



**Integrated  
Circuit  
Systems, Inc.**

## ICS9250-22

### Frequency Generator for P IV™

#### Recommended Application:

P IV Chipset Support

#### Output Features:

- 4 Differential CPU Clock Pairs @ 3.3V
- 2 - 3V MREF clocks for memory reference seeds, (separate single ended but 180 degrees out of phase)
- 4 - 66MHz reference output
- 10 - 3V 33MHz PCI clocks
- 2 - 48MHz clocks
- 2 - 14.318 reference output

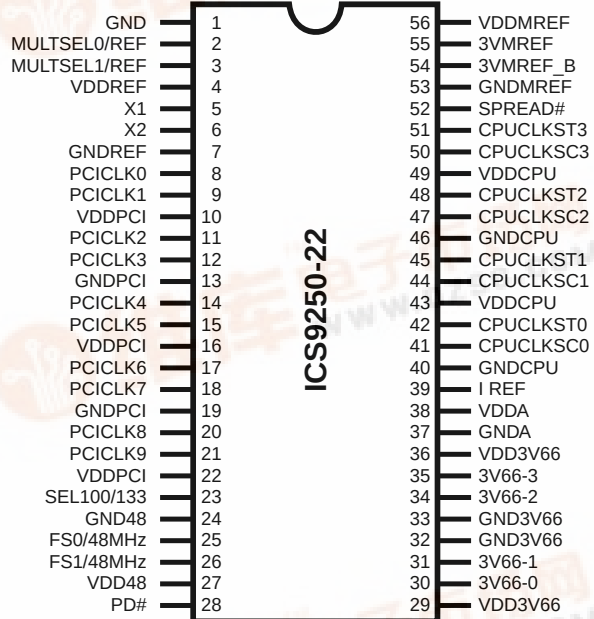
#### Features:

- Support power management: Power Down Mode
- Supports Spread Spectrum modulation: 0 to -0.5% down spread.
- Uses external 14.318MHz crystal
- Select logic for Differential Swing Control, Test mode, Tristate, Power down, Spread Spectrum, limited frequency select, selective clock enable.
- External resistor for current reference
- FS pins for frequency select

#### Key Specifications:

- 3V66 Output jitter <300ps
- CPU Output Jitter <200ps
- MREF Output jitter <250ps

#### Pin Configuration



#### 56-Pin 300mil SSOP & TSSOP

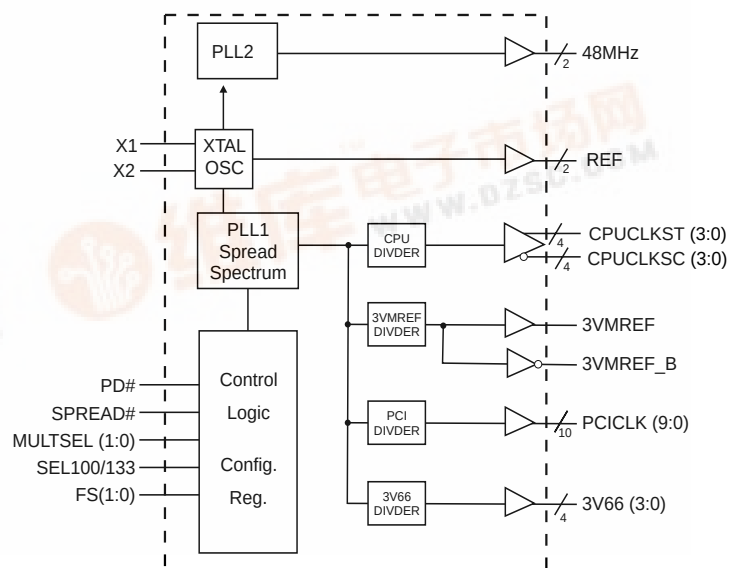
#### Functionality

| SEL133/<br>100 | FS0 | FS1 | Function             |
|----------------|-----|-----|----------------------|
| 0              | 0   | 0   | Active 100MHz        |
| 0              | 0   | 1   | (Reserved)           |
| 0              | 1   | 0   | (Reserved)           |
| 0              | 1   | 1   | Tristate all outputs |
| 1              | 0   | 0   | Active 133MHz        |
| 1              | 0   | 1   | (Reserved)           |
| 1              | 1   | 0   | (Reserved)           |
| 1              | 1   | 1   | Test Mode            |

#### Power Groups

VDDREF, GNDREF = REF, X1, X2  
 VDDPCI, GNDPCI = PCICLK  
 VDD48, GND48 = 48MHz, PLL2  
 VDD3V66, GND3V66 = 3V66  
 VDDCPU, GNDCPU = CPUCLK  
 VDDMREF, GNDMREF = 3VMREF, 3VMREF\_B  
 VDDA = VDD (core supply voltage 3.3V)  
 GNDA = Ground for core supply

#### Block Diagram



# ICS9250-22



## General Description

The **ICS9250-22** is a single chip clock solution.

Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-22 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

## Pin Configuration

| PIN NUMBER                                | PIN NAME          | TYPE              | DESCRIPTION                                                                                                                                                              |
|-------------------------------------------|-------------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 7, 13, 19, 24, 32, 33, 37, 40, 46, 53  | GND               | PWR               | Ground pins for 3.3V supply                                                                                                                                              |
| 3, 2                                      | REF/MULTSEL (1:0) | IN                | MULTSEL0 and MULTSEL1 inputs are sensed on power-up and then internally latched prior to the pin being used for output on 3V 14.318MHz clocks.                           |
| 4, 10, 16, 22, 27, 29, 36, 38, 43, 49, 56 | VDD               | PWR               | 3.3V power supply                                                                                                                                                        |
| 5                                         | X1                | X2 Crystal Input  | 14.318MHz Crystal input                                                                                                                                                  |
| 6                                         | X2                | X1 Crystal Output | 14.318MHz Crystal output                                                                                                                                                 |
| 21, 20, 18, 17, 15, 14, 12, 11, 9, 8      | PCICLK (9:0)      | OUT               | PCI clock outputs                                                                                                                                                        |
| 23                                        | SEL100/133        | IN                | CPU Frequency Select. Low=100MHz, High=133MHz                                                                                                                            |
| 26, 25                                    | FS (1:0)          | IN                | Frequency select pins                                                                                                                                                    |
|                                           | 48MHz             | OUT               | 48MHz clock output                                                                                                                                                       |
| 28                                        | PD#               | IN                | Invokes power-down mode. Active Low.                                                                                                                                     |
| 35, 34, 31, 30                            | 3V66 (3:0)        | OUT               | 66MHz reference clocks                                                                                                                                                   |
| 39                                        | I REF             | OUT               | This pin establishes the reference current for the CPUCLK pairs. This pin takes a fixed precision resistor tied to ground in order to establish the appropriate current. |
| 51, 48, 45, 42                            | CPUCLKST (3:0)    | OUT               | "True" clocks of differential pair CPU outputs. These are switched current outputs and external resistors are required for voltage bias.                                 |
| 50, 47, 44, 41                            | CPUCLKSC (3:0)    | OUT               | "Complementary" clocks of differential pair CPU outputs. These are switched current outputs and external resistors are required for voltage bias.                        |
| 52                                        | SPREAD#           | IN                | Invokes Spread Spectrum functionality on the Differential host clocks, MRef/MRef_b clocks, 66MHz clocks, and 33MHz PCI clocks. Active Low                                |
| 54                                        | 3VMREF_B          | OUT               | 3V reference to memory clock driver (out of phase with 3Vmref)                                                                                                           |
| 55                                        | 3VMREF            | OUT               | 3V reference to memory clock driver                                                                                                                                      |



## ICS9250-22

### Truth Table

| SEL<br>133/100 | FS0 | FS1 | CPU      | MRef     | 3V66     | PCI      | 48MHz    | REF       |
|----------------|-----|-----|----------|----------|----------|----------|----------|-----------|
| 0              | 0   | 0   | 100MHz   | 50MHz    | 66MHz    | 33MHz    | 48MHz    | 14.318MHz |
| 0              | 0   | 1   | N/A      | N/A      | N/A      | N/A      | N/A      | N/A       |
| 0              | 1   | 0   | N/A      | N/A      | N/A      | N/A      | N/A      | N/A       |
| 0              | 1   | 1   | Tristate | Tristate | Tristate | Tristate | Tristate | Tristate  |
| 1              | 0   | 0   | 133MHz   | 66MHz    | 66MHz    | 33MHz    | 48MHz    | 14.318MHz |
| 1              | 0   | 1   | N/A      | N/A      | N/A      | N/A      | N/A      | N/A       |
| 1              | 1   | 0   | N/A      | N/A      | N/A      | N/A      | N/A      | N/A       |
| 1              | 1   | 1   | TCLK/2   | TCLK/4   | TCLK     | TCLK/6   |          | TCLK      |

### Group Offset Limits

| Group       | Offset                    | Measurement Loads<br>(lumped) | Measure Points |
|-------------|---------------------------|-------------------------------|----------------|
| CPU to 3V66 | No Requirement            |                               |                |
| CPU to PCI  |                           |                               |                |
| 3V66 to PCI | 1.5 - 3.5ns<br>3V66 leads | 30pF                          | 1.5V           |

# ICS9250-22



## CPUCLK Buffer Configuration

|             | Conditions            | Configuration                                          | Load                                      | Min            | Max            |
|-------------|-----------------------|--------------------------------------------------------|-------------------------------------------|----------------|----------------|
| <b>Iout</b> | Vdd = nominal (3.30V) | All combinations of M0, M1 and Rr shown in table below | Nominal test load for given configuration | -7% I nominal  | +7% I nominal  |
| <b>Iout</b> | Vdd = 3.30 ± 5%       | All combinations of M0, M1 and Rr shown in table below | Nominal test load for given configuration | -12% I nominal | +12% I nominal |

## CPUCLK Swing Select Functions

| MULTSEL0 | MULTSEL1 | Board Target Trace/Term Z | Reference R, Iref= Vdd/(3*Rr) | Output Current | Voh @ Z, Iref=2.32mA |
|----------|----------|---------------------------|-------------------------------|----------------|----------------------|
| 0        | 0        | 60 ohms                   | Rr = 475 1%<br>Iref = 2.32mA  | Ioh = 5*Iref   | 0.71V @ 60           |
| 0        | 0        | 50 ohms                   | Rr = 475 1%<br>Iref = 2.32mA  | Ioh = 5*Iref   | 0.59V @ 50           |
| 0        | 1        | 60 ohms                   | Rr = 475 1%<br>Iref = 2.32mA  | Ioh = 6*Iref   | 0.85V /2 60          |
| 0        | 1        | 50 ohms                   | Rr = 475 1%<br>Iref = 2.32mA  | Ioh = 6*Iref   | 0.71V @ 50           |
| 1        | 0        | 60 ohms                   | Rr = 475 1%<br>Iref = 2.32mA  | Ioh = 4*Iref   | 0.56V @ 60           |
| 1        | 0        | 50 ohms                   | Rr = 475 1%<br>Iref = 2.32mA  | Ioh = 4*Iref   | 0.47V @ 50           |
| 1        | 1        | 60 ohms                   | Rr = 475 1%<br>Iref = 2.32mA  | Ioh = 7*Iref   | 0.99V @ 60           |
| 1        | 1        | 50 ohms                   | Rr = 475 1%<br>Iref = 2.32mA  | Ioh = 7*Iref   | 0.82V @ 50           |
| 0        | 0        | 30 (DC equiv)             | Rr = 221 1%<br>Iref = 5mA     | Ioh = 5*Iref   | 0.75V @ 30           |
| 0        | 0        | 25 (DC equiv)             | Rr = 221 1%<br>Iref = 5mA     | Ioh = 5*Iref   | 0.62V @ 20           |
| 0        | 1        | 30 (DC equiv)             | Rr = 221 1%<br>Iref = 5mA     | Ioh = 6*Iref   | 0.90V @ 30           |
| 0        | 1        | 25 (DC equiv)             | Rr = 221 1%<br>Iref = 5mA     | Ioh = 6*Iref   | 0.75V @ 20           |
| 1        | 0        | 30 (DC equiv)             | Rr = 221 1%<br>Iref = 5mA     | Ioh = 4*Iref   | 0.60 @ 20            |
| 1        | 0        | 25 (DC equiv)             | Rr = 221 1%<br>Iref = 5mA     | Ioh = 4*Iref   | 0.5V @ 20            |
| 1        | 1        | 30 (DC equiv)             | Rr = 221 1%<br>Iref = 5mA     | Ioh = 7*Iref   | 1.05V @ 30           |
| 1        | 1        | 25 (DC equiv)             | Rr = 221 1%<br>Iref = 5mA     | Ioh = 7*Iref   | 0.84V @ 20           |



## Absolute Maximum Ratings

Supply Voltage ..... 5.5 V  
Logic Inputs ..... GND -0.5 V to  $V_{DD} + 0.5$  V  
Ambient Operating Temperature ..... 0°C to +70°C  
Case Temperature ..... 115°C  
Storage Temperature ..... -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = 3.3$  V +/-5%

| PARAMETER                      | SYMBOL             | CONDITIONS                                       | MIN            | TYP    | MAX            | UNITS         |
|--------------------------------|--------------------|--------------------------------------------------|----------------|--------|----------------|---------------|
| Input High Voltage             | $V_{IH}$           |                                                  | 2              |        | $V_{DD} + 0.3$ | V             |
| Input Low Voltage              | $V_{IL}$           |                                                  | $V_{SS} - 0.3$ |        | 0.8            | V             |
| Input High Current             | $I_{IH}$           | $V_{IN} = V_{DD}$                                | -5             |        | 5              | $\mu\text{A}$ |
| Input Low Current              | $I_{IL1}$          | $V_{IN} = 0$ V; Inputs with no pull-up resistors | -5             |        |                | $\mu\text{A}$ |
|                                | $I_{IL2}$          | $V_{IN} = 0$ V; Inputs with pull-up resistors    | -200           |        |                |               |
| Operating Supply Current       | $I_{DD3.3OP}$      | $C_L = 0$ pF; Select @ 100 MHz                   |                | 130    | 250            | mA            |
| Powerdown Current              | $I_{DD3.3PD}$      | $C_L = 0$ pF; Input address to VDD or GND        |                | 35     | 60             | mA            |
| Input Frequency                | $F_i$              | $V_{DD} = 3.3$ V                                 |                | 14.318 |                | MHz           |
| Pin Inductance                 | $L_{pin}$          |                                                  |                |        | 7              | nH            |
| Input Capacitance <sup>1</sup> | $C_{IN}$           | Logic Inputs                                     |                |        | 5              | pF            |
|                                | $C_{OUT}$          | Output pin capacitance                           |                |        | 6              | pF            |
|                                | $C_{INX}$          | X1 & X2 pins                                     | 27             |        | 45             | pF            |
| Transition time <sup>1</sup>   | $T_{trans}$        | To 1st crossing of target frequency              |                |        | 3              | ms            |
| Settling time <sup>1</sup>     | $T_s$              | From 1st crossing to 1% target frequency         |                |        | 3              | ms            |
| Clk Stabilization <sup>1</sup> | $T_{STAB}$         | From $V_{DD} = 3.3$ V to 1% target frequency     |                |        | 3              | ms            |
| Delay <sup>1</sup>             | $t_{PZH}, t_{PZL}$ | Output enable delay (all outputs)                | 1              |        | 10             | ns            |
|                                | $t_{PHZ}, t_{PLZ}$ | Output disable delay (all outputs)               | 1              |        | 10             | ns            |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

# ICS9250-22



## Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

| PARAMETER           | SYMBOL          | CONDITIONS                                                  | MIN | TYP | MAX | UNITS    |
|---------------------|-----------------|-------------------------------------------------------------|-----|-----|-----|----------|
| Output Impedance    | $R_{DSP2B}^1$   | $V_O = V_{DD} \cdot (0.5)$                                  |     | 714 |     | $\Omega$ |
| Output Impedance    | $R_{DSN2B}^1$   | $V_O = V_{DD} \cdot (0.5)$                                  |     | 714 |     | $\Omega$ |
| Output High Voltage | $V_{OH2B}$      | $I_{OH} = -1\text{ mA}$                                     | 2   |     |     | V        |
| Output Low Voltage  | $V_{OL2B}$      | $I_{OL} = 1\text{ mA}$                                      |     |     | 0.4 | V        |
| Output High Current | $I_{OH2B}^2$    | $V_{OH@MIN} = 1.0\text{ V}$ , $V_{OH@MAX} = 2.375\text{ V}$ | -27 |     | -27 | mA       |
| Output Low Current  | $I_{OL2B}^2$    | $V_{OL@MIN} = 1.2\text{ V}$ , $V_{OL@MAX} = 0.3\text{ V}$   | 27  |     | 30  | mA       |
| Rise Time           | $t_{r2B}^1$     | $V_{OL} = 20\%$ , $V_{OH} = 80\%$                           | 175 | 500 | 700 | ps       |
| Fall Time           | $t_{f2B}^1$     | $V_{OH} = 80\%$ , $V_{OL} = 20\%$                           | 175 | 500 | 700 | ps       |
| Duty Cycle          | $d_{t2B}^1$     | $V_T = 50\%$                                                | 45  | 51  | 55  | %        |
| Skew                | $t_{sk2B}^1$    | $V_T = 50\%$                                                |     | 110 | 150 | ps       |
| Jitter              | $t_{jyc-cyc}^1$ | $V_T = 50\%$                                                |     | 110 | 200 | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup> $I_{OWT}$  can be varied and is selectable thru the MULTSEL pin.

## Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}30\text{ pF}$  (unless otherwise specified)

| PARAMETER           | SYMBOL          | CONDITIONS                                                  | MIN | TYP | MAX  | UNITS    |
|---------------------|-----------------|-------------------------------------------------------------|-----|-----|------|----------|
| Output Frequency    | $F_{O1}$        |                                                             |     |     |      | MHz      |
| Output Impedance    | $R_{DSP1}^1$    | $V_O = V_{DD} \cdot (0.5)$                                  | 12  | 33  | 55   | $\Omega$ |
| Output High Voltage | $V_{OH}^1$      | $I_{OH} = -1\text{ mA}$                                     | 2.4 |     |      | V        |
| Output Low Voltage  | $V_{OL}^1$      | $I_{OL} = 1\text{ mA}$                                      |     |     | 0.55 | V        |
| Output High Current | $I_{OH}^1$      | $V_{OH@MIN} = 1.0\text{ V}$ , $V_{OH@MAX} = 3.135\text{ V}$ | -33 |     | -33  | mA       |
| Output Low Current  | $I_{OL}^1$      | $V_{OL@MIN} = 1.95\text{ V}$ , $V_{OL@MAX} = 0.4\text{ V}$  | 30  |     | 38   | mA       |
| Rise Time           | $t_{r1}^1$      | $V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$           | 0.5 | 1.4 | 2    | ns       |
| Fall Time           | $t_{f1}^1$      | $V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$           | 0.5 | 1.4 | 2    | ns       |
| Duty Cycle          | $d_{t1}^1$      | $V_T = 1.5\text{ V}$                                        | 45  | 51  | 55   | %        |
| Skew                | $t_{sk1}^1$     | $V_T = 1.5\text{ V}$                                        |     | 270 | 500  | ps       |
| Jitter              | $t_{jyc-cyc}^1$ | $V_T = 1.5\text{ V}$                                        |     | 115 | 500  | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## ICS9250-22

### Electrical Characteristics - MREF/MREF\_B

T<sub>A</sub> = 0 - 70°C; VDD=3.3V +/-5%; C<sub>L</sub> = 10-20 pF (unless otherwise specified)

| PARAMETER           | SYMBOL                            | CONDITIONS                                                 | MIN | TYP | MAX  | UNITS |
|---------------------|-----------------------------------|------------------------------------------------------------|-----|-----|------|-------|
| Output Frequency    | F <sub>O1</sub>                   |                                                            |     |     |      | MHz   |
| Output Impedance    | R <sub>DSP1</sub> <sup>1</sup>    | V <sub>O</sub> = V <sub>DD</sub> *(0.5)                    | 12  | 33  | 55   | Ω     |
| Output High Voltage | V <sub>OH</sub> <sup>1</sup>      | I <sub>OH</sub> = -1 mA                                    | 2.4 |     |      | V     |
| Output Low Voltage  | V <sub>OL</sub> <sup>1</sup>      | I <sub>OL</sub> = 1 mA                                     |     |     | 0.55 | V     |
| Output High Current | I <sub>OH</sub> <sup>1</sup>      | V <sub>OH@MIN</sub> = 1.0 V, V <sub>OH@MAX</sub> = 3.135 V | -33 |     | -33  | mA    |
| Output Low Current  | I <sub>OL</sub> <sup>1</sup>      | V <sub>OL@MIN</sub> = 1.95 V, V <sub>OL@MAX</sub> = 0.4 V  | 30  |     | 38   | mA    |
| Rise Time           | t <sub>r1</sub> <sup>1</sup>      | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V           | 0.4 | 1.4 | 1.6  | ns    |
| Fall Time           | t <sub>f1</sub> <sup>1</sup>      | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V           | 0.4 | 1.4 | 1.6  | ns    |
| Duty Cycle          | d <sub>tl</sub> <sup>1</sup>      | V <sub>T</sub> = 1.5 V                                     | 45  | 51  | 55   | %     |
| Skew                | t <sub>sk1</sub> <sup>1</sup>     | V <sub>T</sub> = 1.5 V                                     |     | 80  | 100  | ps    |
| Jitter              | t <sub>jcy-cyc</sub> <sup>1</sup> | V <sub>T</sub> = 1.5 V                                     |     | 105 | 250  | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - REF

T<sub>A</sub> = 0 - 70°C; VDD=3.3V +/-5%; C<sub>L</sub> = 10-20 pF (unless otherwise specified)

| PARAMETER           | SYMBOL                            | CONDITIONS                                                 | MIN | TYP | MAX  | UNITS |
|---------------------|-----------------------------------|------------------------------------------------------------|-----|-----|------|-------|
| Output Frequency    | F <sub>O1</sub>                   |                                                            |     |     |      | MHz   |
| Output Impedance    | R <sub>DSP1</sub> <sup>1</sup>    | V <sub>O</sub> = V <sub>DD</sub> *(0.5)                    | 20  | 48  | 60   | Ω     |
| Output High Voltage | V <sub>OH</sub> <sup>1</sup>      | I <sub>OH</sub> = -1 mA                                    | 2.4 |     |      | V     |
| Output Low Voltage  | V <sub>OL</sub> <sup>1</sup>      | I <sub>OL</sub> = 1 mA                                     |     |     | 0.4  | V     |
| Output High Current | I <sub>OH</sub> <sup>1</sup>      | V <sub>OH@MIN</sub> = 1.0 V, V <sub>OH@MAX</sub> = 3.135 V | -29 |     | -23  | mA    |
| Output Low Current  | I <sub>OL</sub> <sup>1</sup>      | V <sub>OL@MIN</sub> = 1.95 V, V <sub>OL@MAX</sub> = 0.4 V  | 29  |     | 27   | mA    |
| Rise Time           | t <sub>r1</sub> <sup>1</sup>      | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V           | 1   | 2   | 4    | ns    |
| Fall Time           | t <sub>f1</sub> <sup>1</sup>      | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V           | 1   | 2   | 4    | ns    |
| Duty Cycle          | d <sub>tl</sub> <sup>1</sup>      | V <sub>T</sub> = 1.5 V                                     | 45  | 50  | 55   | %     |
| Skew                | t <sub>sk1</sub> <sup>1</sup>     | V <sub>T</sub> = 1.5 V                                     |     |     | N/A  | ps    |
| Jitter              | t <sub>jcy-cyc</sub> <sup>1</sup> | V <sub>T</sub> = 1.5 V                                     |     | 205 | 1000 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

# ICS9250-22



## Electrical Characteristics - 3V66

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD}=3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}30\text{ pF}$  (unless otherwise specified)

| PARAMETER           | SYMBOL          | CONDITIONS                                                  | MIN | TYP | MAX  | UNITS    |
|---------------------|-----------------|-------------------------------------------------------------|-----|-----|------|----------|
| Output Frequency    | $F_{OI}$        |                                                             |     |     |      | MHz      |
| Output Impedance    | $R_{DSP1}^1$    | $V_O = V_{DD}*(0.5)$                                        | 12  | 33  | 55   | $\Omega$ |
| Output High Voltage | $V_{OH}^1$      | $I_{OH} = -1\text{ mA}$                                     | 2.4 |     |      | V        |
| Output Low Voltage  | $V_{OL}^1$      | $I_{OL} = 1\text{ mA}$                                      |     |     | 0.55 | V        |
| Output High Current | $I_{OH}^1$      | $V_{OH@MIN} = 1.0\text{ V}$ , $V_{OH@MAX} = 3.135\text{ V}$ | -33 |     | -33  | mA       |
| Output Low Current  | $I_{OL}^1$      | $V_{OL@MIN} = 1.95\text{ V}$ , $V_{OL@MAX} = 0.4\text{ V}$  | 30  |     | 38   | mA       |
| Rise Time           | $t_{r1}^1$      | $V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$           | 0.5 | 1.3 | 2    | ns       |
| Fall Time           | $t_{f1}^1$      | $V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$           | 0.5 | 1.3 | 2    | ns       |
| Duty Cycle          | $d_{t1}^1$      | $V_T = 1.5\text{ V}$                                        | 45  | 51  | 55   | %        |
| Skew                | $t_{sk1}^1$     | $V_T = 1.5\text{ V}$                                        |     | 85  | 250  | ps       |
| Jitter              | $t_{jyc-cyc}^1$ | $V_T = 1.5\text{ V}$                                        |     | 80  | 300  | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - 48MHz

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD}=3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

| PARAMETER           | SYMBOL          | CONDITIONS                                                  | MIN | TYP | MAX | UNITS    |
|---------------------|-----------------|-------------------------------------------------------------|-----|-----|-----|----------|
| Output Frequency    | $F_{OI}$        |                                                             |     |     |     | MHz      |
| Output Impedance    | $R_{DSP1}^1$    | $V_O = V_{DD}*(0.5)$                                        | 20  | 48  | 60  | $\Omega$ |
| Output High Voltage | $V_{OH}^1$      | $I_{OH} = -1\text{ mA}$                                     | 2.4 |     |     | V        |
| Output Low Voltage  | $V_{OL}^1$      | $I_{OL} = 1\text{ mA}$                                      |     |     | 0.4 | V        |
| Output High Current | $I_{OH}^1$      | $V_{OH@MIN} = 1.0\text{ V}$ , $V_{OH@MAX} = 3.135\text{ V}$ | -29 |     | -23 | mA       |
| Output Low Current  | $I_{OL}^1$      | $V_{OL@MIN} = 1.95\text{ V}$ , $V_{OL@MAX} = 0.4\text{ V}$  | 29  |     | 27  | mA       |
| Rise Time           | $t_{r1}^1$      | $V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$           | 1   | 2   | 4   | ns       |
| Fall Time           | $t_{f1}^1$      | $V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$           | 1   | 2   | 4   | ns       |
| Duty Cycle          | $d_{t1}^1$      | $V_T = 1.5\text{ V}$                                        | 45  | 54  | 55  | %        |
| Skew                | $t_{sk1}^1$     | $V_T = 1.5\text{ V}$                                        |     |     | N/A | ps       |
| Jitter              | $t_{jyc-cyc}^1$ | $V_T = 1.5\text{ V}$                                        |     | 120 | 350 | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

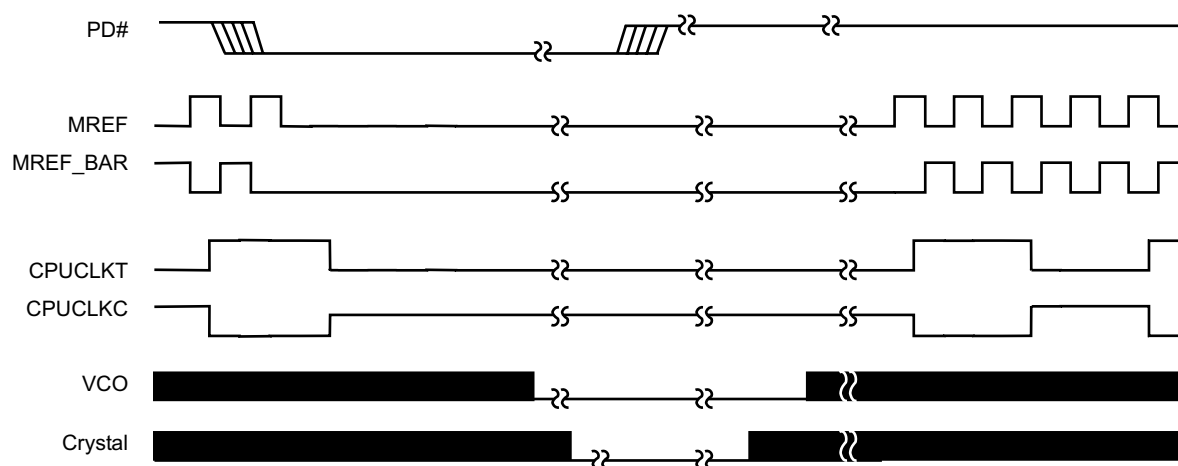




## PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

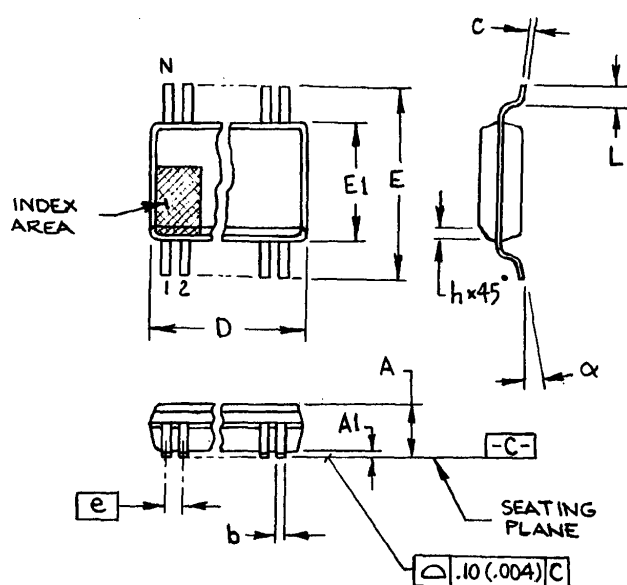
Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below.



### Notes:

1. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock.

# ICS9250-22



300 mil SSOP

| SYMBOL   | In Millimeters<br>COMMON DIMENSIONS |        | In Inches<br>COMMON DIMENSIONS |       |
|----------|-------------------------------------|--------|--------------------------------|-------|
|          | MIN                                 | MAX    | MIN                            | MAX   |
| A        | 2.413                               | 2.794  | .095                           | .110  |
| A1       | 0.203                               | 0.406  | .008                           | .016  |
| b        | 0.203                               | 0.343  | .008                           | .0135 |
| c        | 0.127                               | 0.254  | .005                           | .010  |
| D        | SEE VARIATIONS                      |        | SEE VARIATIONS                 |       |
| E        | 10.033                              | 10.668 | .395                           | .420  |
| E1       | 7.391                               | 7.595  | .291                           | .299  |
| e        | 0.635 BASIC                         |        | 0.025 BASIC                    |       |
| h        | 0.381                               | 0.635  | .015                           | .025  |
| L        | 0.508                               | 1.016  | .020                           | .040  |
| N        | SEE VARIATIONS                      |        | SEE VARIATIONS                 |       |
| $\alpha$ | 0°                                  | 8°     | 0°                             | 8°    |

## VARIATIONS

| N  | D mm.  |        | D (inch) |      |
|----|--------|--------|----------|------|
|    | MIN    | MAX    | MIN      | MAX  |
| 56 | 18.288 | 18.542 | .720     | .730 |

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## Ordering Information

ICS9250yF-22-T

Example:

ICS XXXX y F - PPP - T

Designation for tape and reel packaging

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type  
F=SSOP

Revision Designator (will not correlate with datasheet revision)

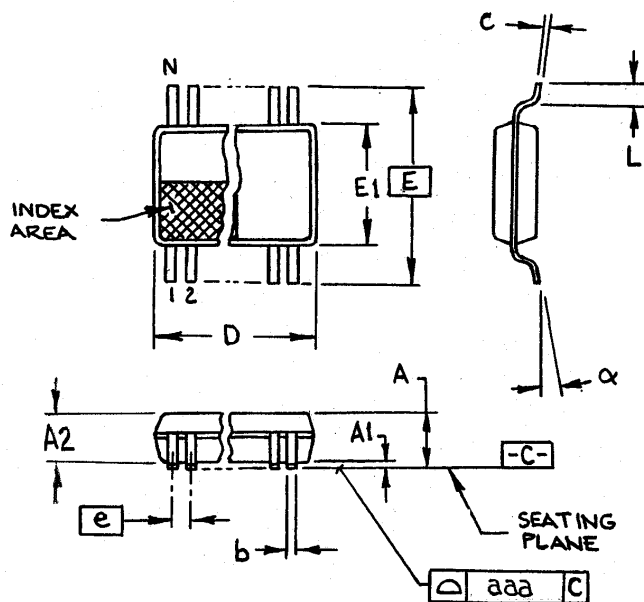
Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV = Standard Device



# ICS9250-22



6.10 mm. Body, 0.50 mm. pitch TSSOP  
(240 mil) (0.020 mil)

| SYMBOL   | In Millimeters<br>COMMON DIMENSIONS |      | In Inches<br>COMMON DIMENSIONS |      |
|----------|-------------------------------------|------|--------------------------------|------|
|          | MIN                                 | MAX  | MIN                            | MAX  |
| A        | -                                   | 1.20 | -                              | .047 |
| A1       | 0.05                                | 0.15 | .002                           | .006 |
| A2       | 0.80                                | 1.05 | .032                           | .041 |
| b        | 0.17                                | 0.27 | .007                           | .011 |
| c        | 0.09                                | 0.20 | .0035                          | .008 |
| D        | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| E        | 8.10 BASIC                          |      | 0.319                          |      |
| E1       | 6.00                                | 6.20 | .236                           | .244 |
| e        | 0.50 BASIC                          |      | 0.020 BASIC                    |      |
| L        | 0.45                                | 0.75 | .018                           | .30  |
| N        | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| $\alpha$ | 0°                                  | 8°   | 0°                             | 8°   |
| aaa      | -                                   | 0.10 | -                              | .004 |

## VARIATIONS

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 56 | 13.90 | 14.10 | .547     | .555 |

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## Ordering Information

ICS9250yG-22-T

Example:

ICS XXXX y G - PPP - T

- Designation for tape and reel packaging
- Pattern Number (2 or 3 digit number for parts with ROM code patterns)
- Package Type  
G=TSSOP
- Revision Designator (will not correlate with datasheet revision)
- Device Type (consists of 3 or 4 digit numbers)
- Prefix  
ICS, AV = Standard Device