

Preliminary

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M5Y816WG -70HI, -85HI**8388608-BIT (524288-WORD BY 16-BIT) CMOS STATIC RAM**

Those are summarized in the part name table below.

DESCRIPTION

The M5M5Y816 is a family of low voltage 8-Mbit static RAMs organized as 524288-words by 16-bit, fabricated by Mitsubishi's high-performance 0.18μm CMOS technology.

The M5M5Y816 is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5Y816WG is packaged in a CSP (chip scale package), with the outline of 7.5mm x 8.5mm, ball matrix of 6 x 8 (48ball) and ball pitch of 0.75mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

FEATURES

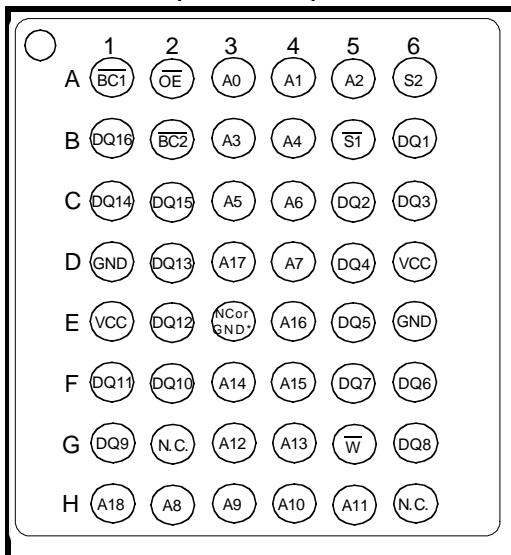
- Single 1.65~2.3V power supply
- Small stand-by current: 0.5μA (2.0V, typ.)
- No clocks, No refresh
- Data retention supply voltage =1.3V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by S1, S2, BC1 and BC2
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Process technology: 0.18μm CMOS
- Package: 48ball 7.5mm x 8.5mm CSP

Version, Operating temperature	Part name	Power Supply	Access time max.	Stand-by current (μA)						Activ e current Icc1 (2.3V, max)	
				* Typical		Ratings (max.)					
				25°C	40°C	25°C	40°C	70°C	85°C		
I-version -40 ~ +85°C	M5M5Y816WG -70HI	1.65 ~ 2.3V	70ns	0.5	1	2	4	15	30	30mA (10MHz) 3mA (1MHz)	
	M5M5Y816WG -85HI	1.65 ~ 2.3V	85ns								

* Typical parameter indicates the value for the center of distribution at 2.0V, and not 100% tested.

PIN CONFIGURATION

(TOP VIEW)



Pin	Function
A0 ~ A18	Address input
DQ1 ~ DQ16	Data input / output
S1	Chip select input 1
S2	Chip select input 2
W	Write control input
OE	Output enable input
BC1	Lower Byte (DQ1 ~ 8)
BC2	Upper Byte (DQ9 ~ 16)
Vcc	Power supply
GND	Ground supply

Outline: 48F7Q

NC: No Connection

*Don't connect E3 ball to voltage level more than 0V



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FUNCTION

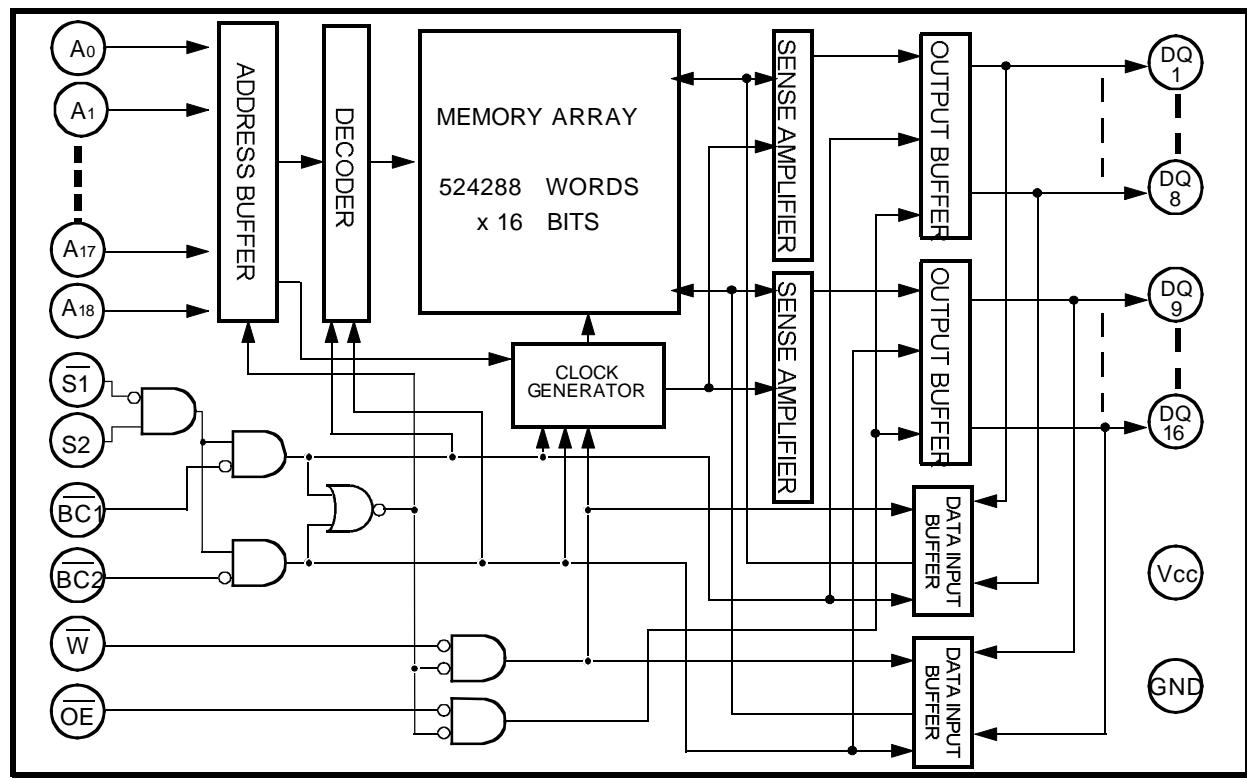
The M5M5Y816WG is organized as 524288-words by 16-bit. These devices operate on a single +1.65~2.3V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs $\overline{BC1}$, $\overline{BC2}$, $\overline{S1}$, $S2$, \overline{W} and \overline{OE} . Each mode is summarized in the function table.

A write operation is executed whenever the low level \overline{W} overlaps with the low level $\overline{BC1}$ and/or $\overline{BC2}$ and the low level $\overline{S1}$ and the high level $S2$. The address(A0~A18) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{BC1}$ and/or $\overline{BC2}$ and $S1$ and $S2$ are in an active state($S1=L, S2=H$).

When setting $BC1$ at the high level and other pins are in an active stage, upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting $BC2$ at a high level and other pins are in an active stage, lower-byte are in a selectable mode and upper-byte are in a non-selectable mode.

BLOCK DIAGRAM

When setting $\overline{BC1}$ and $\overline{BC2}$ at a high level or $\overline{S1}$ at a high level or $S2$ at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $BC1$, $BC2$ and $\overline{S1}$, $S2$.

The power supply current is reduced as low as $0.5\mu A$ ($25^\circ C$, typical), and the memory data can be held at +1.3V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	$S2$	$\overline{BC1}$	$\overline{BC2}$	\overline{W}	\overline{OE}	Mode	DQ1~8	DQ9~16	Icc
H	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
L	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
H	H	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	X	H	H	X	X	Non selection	High-Z	High-Z	Standby
L	H	L	H	L	X	Write	Din	High-Z	Active
L	H	L	H	L	X	Read	Dout	High-Z	Active
L	H	L	H	H	—	—	High-Z	High-Z	Active
L	H	H	L	X	—	Write	High-Z	Din	Active
L	H	H	L	L	X	Read	High-Z	Dout	Active
L	H	H	L	H	H	—	High-Z	High-Z	Active
L	H	L	L	X	—	Write	Din	Din	Active
L	H	L	L	H	L	Read	Dout	Dout	Active
L	H	L	L	H	H	—	High-Z	High-Z	Active



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings		Units
V _{cc}	Supply voltage	With respect to GND	-0.5*	~ +2.7	V
V _I	Input voltage	With respect to GND	-0.2*	~ V _{cc} + 0.2 (max. 2.7V)	
V _O	Output voltage	With respect to GND	0	~ V _{cc}	
P _d	Power dissipation	T _a =25°C	700		mW
T _a	Operating temperature	I-v ersion	- 40	~ +85	°C
T _{stg}	Storage temperature		- 65	~ +150	°C

* -0.7V in case of AC (Pulse width \leq 30ns)**DC ELECTRICAL CHARACTERISTICS**(V_{cc}=1.65~ 2.3V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
V _{IH}	High-level input voltage		0.7 x V _{cc}		V _{cc} +0.2	V
V _{IL}	Low-level input voltage		-0.2 *		0.4	
V _{OH}	High-level output voltage	I _{OH} = -0.1mA	1.3			
V _{OL}	Low-level output voltage	I _{OL} =0.1mA			0.2	
I _I	Input leakage current	V _I =0 ~ V _{cc}			±1	μA
I _O	Output leakage current	BC1 and BC2=V _{IH} or S1=V _{IH} or S2=V _{IL} or OE=V _{IH} , V _I /O=0 ~ V _{cc}			±1	
I _{cc1}	Active supply current (AC,MOS level)	BC1 and BC2 \leq 0.2V, S1 \leq 0.2V, S2 \geq V _{cc} -0.2V other inputs \leq 0.2V or \geq V _{cc} -0.2V Output - open (duty 100%)	f= 10MHz	-	20	30
			f= 1MHz	-	1.5	3
I _{cc2}	Active supply current (AC,TTL level)	BC1 and BC2=V _{IL} , S1=V _{IL} , S2=V _{IH} other pins =V _{IH} or V _{IL} Output - open (duty 100%)	f= 10MHz	-	20	30
			f= 1MHz	-	1.5	3
I _{cc3}	Stand by supply current (AC,MOS level)	(1) S1 \geq V _{cc} - 0.2V, S2 \geq V _{cc} - 0.2V, other inputs = 0 ~ V _{cc} (2) S2 \leq 0.2V, other inputs = 0 ~ V _{cc} (3) BC1 and BC2 \geq V _{cc} - 0.2V S1 \leq 0.2V, S2 \geq V _{cc} - 0.2V other inputs = 0 ~ V _{cc}	~ +25°C	-	0.5	2
			~ +40°C	-	1	4
			~ +70°C	-	-	15
			~ +85°C	-	-	30
I _{cc4}	Stand by supply current (AC,TTL level)	BC1 and BC2=V _{IH} or S1=V _{IH} or S2=V _{IL} Other inputs= 0 ~ V _{cc}		-	-	0.5

* -0.7V in case of AC (Pulse width \leq 30ns)

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

Note 2: Typical parameter indicates the value for the center of distribution at 2.0V, and not 100% tested.

CAPACITANCE(V_{cc}=1.65 ~ 2.3V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			10	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	



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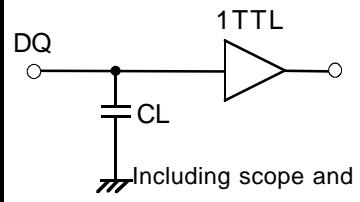
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AC ELECTRICAL CHARACTERISTICS (V_{CC}=1.65 ~ 2.3V, unless otherwise noted)**(1) TEST CONDITIONS**

Supply voltage	1.65~2.3V
Input pulse	V _{IH} =0.7 x V _{CC} +0.2V, V _{IL} =0.2V
Input rise time and fall time	5ns
Reference level	V _{OH} =V _{OL} =0.9V Transition is measured ±200mV from steady state voltage.(for t _{en} , t _{dis})
Output loads	Fig.1, CL=30pF CL=5pF (for t _{en} , t _{dis})

**(2) READ CYCLE**

Symbol	Parameter	Limits				Units	
		70HI		85HI			
		Min	Max	Min	Max		
t _{CR}	Read cycle time	70		85		ns	
t _{a(A)}	Address access time		70		85	ns	
t _{a(S1)}	Chip select 1 access time		70		85	ns	
t _{a(S2)}	Chip select 2 access time		70		85	ns	
t _{a(BC1)}	Byte control 1 access time		70		85	ns	
t _{a(BC2)}	Byte control 2 access time		70		85	ns	
t _{a(OE)}	Output enable access time		35		45	ns	
t _{dis(S1)}	Output disable time after S1 high		25		30	ns	
t _{dis(S2)}	Output disable time after S2 low		25		30	ns	
t _{dis(BC1)}	Output disable time after BC1 high		25		30	ns	
t _{dis(BC2)}	Output disable time after BC2 high		25		30	ns	
t _{dis(OE)}	Output disable time after OE high		25		30	ns	
t _{en(S1)}	Output enable time after S1 low	10		10		ns	
t _{en(S2)}	Output enable time after S2 high	10		10		ns	
t _{en(BC1)}	Output enable time after BC1 low	10		10		ns	
t _{en(BC2)}	Output enable time after BC2 low	10		10		ns	
t _{en(OE)}	Output enable time after OE low	5		5		ns	
t _{v(A)}	Data valid time after address	10		10		ns	

(3) WRITE CYCLE

Symbol	Parameter	Limits				Units	
		70HI		85HI			
		Min	Max	Min	Max		
t _{cw}	Write cycle time	70		85		ns	
t _{w(W)}	Write pulse width	55		60		ns	
t _{su(A)}	Address setup time	0		0		ns	
t _{su(A-WH)}	Address setup time with respect to W	65		70		ns	
t _{su(BC1)}	Byte control 1 setup time	65		70		ns	
t _{su(BC2)}	Byte control 2 setup time	65		70		ns	
t _{su(S1)}	Chip select 1 setup time	65		70		ns	
t _{su(S2)}	Chip select 2 setup time	65		70		ns	
t _{su(D)}	Data setup time	30		35		ns	
t _{h(D)}	Data hold time	0		0		ns	
t _{rec(W)}	Write recovery time	0		0		ns	
t _{dis(W)}	Output disable time from W low		25		30	ns	
t _{dis(OE)}	Output disable time from OE high		25		30	ns	
t _{en(W)}	Output enable time from W high	5		5		ns	
t _{en(OE)}	Output enable time from OE low	5		5		ns	



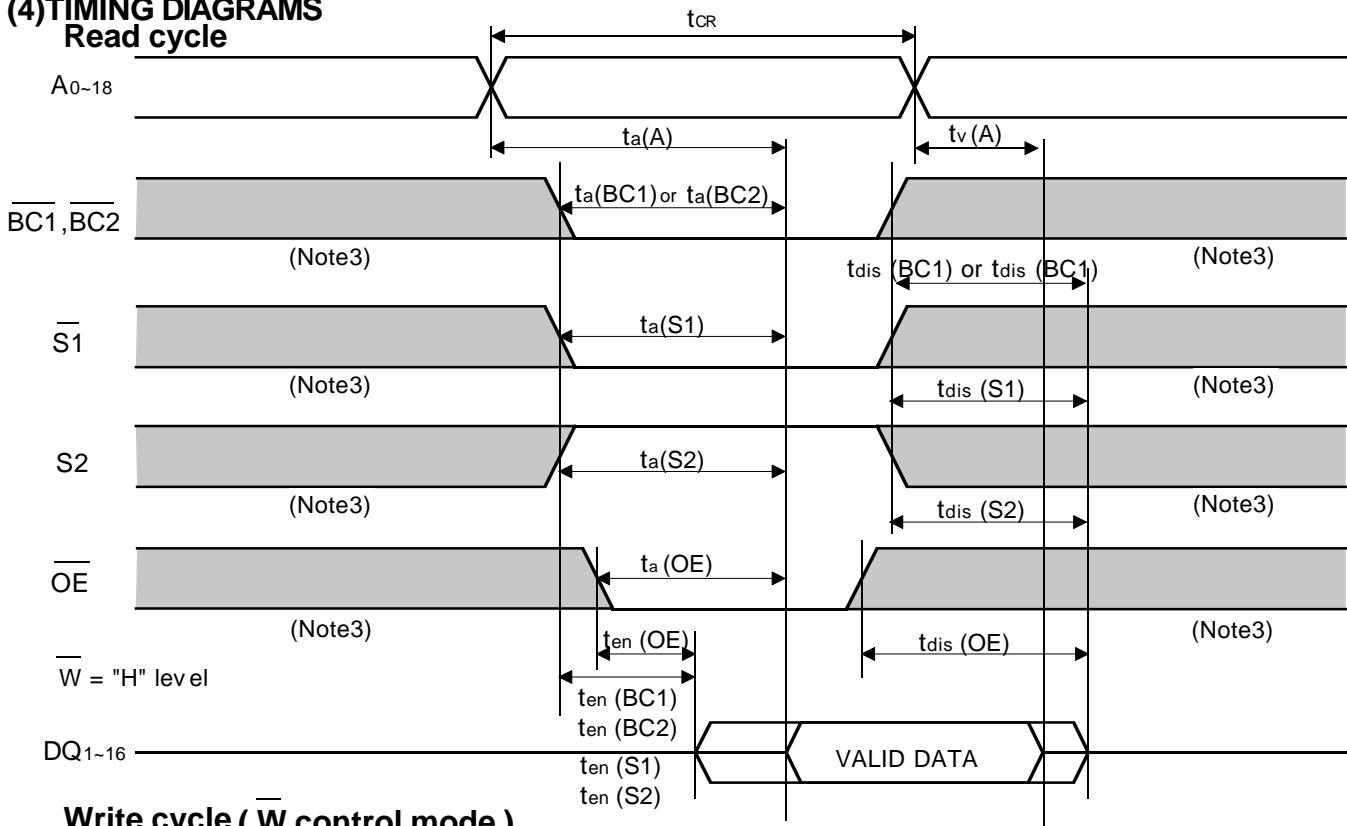
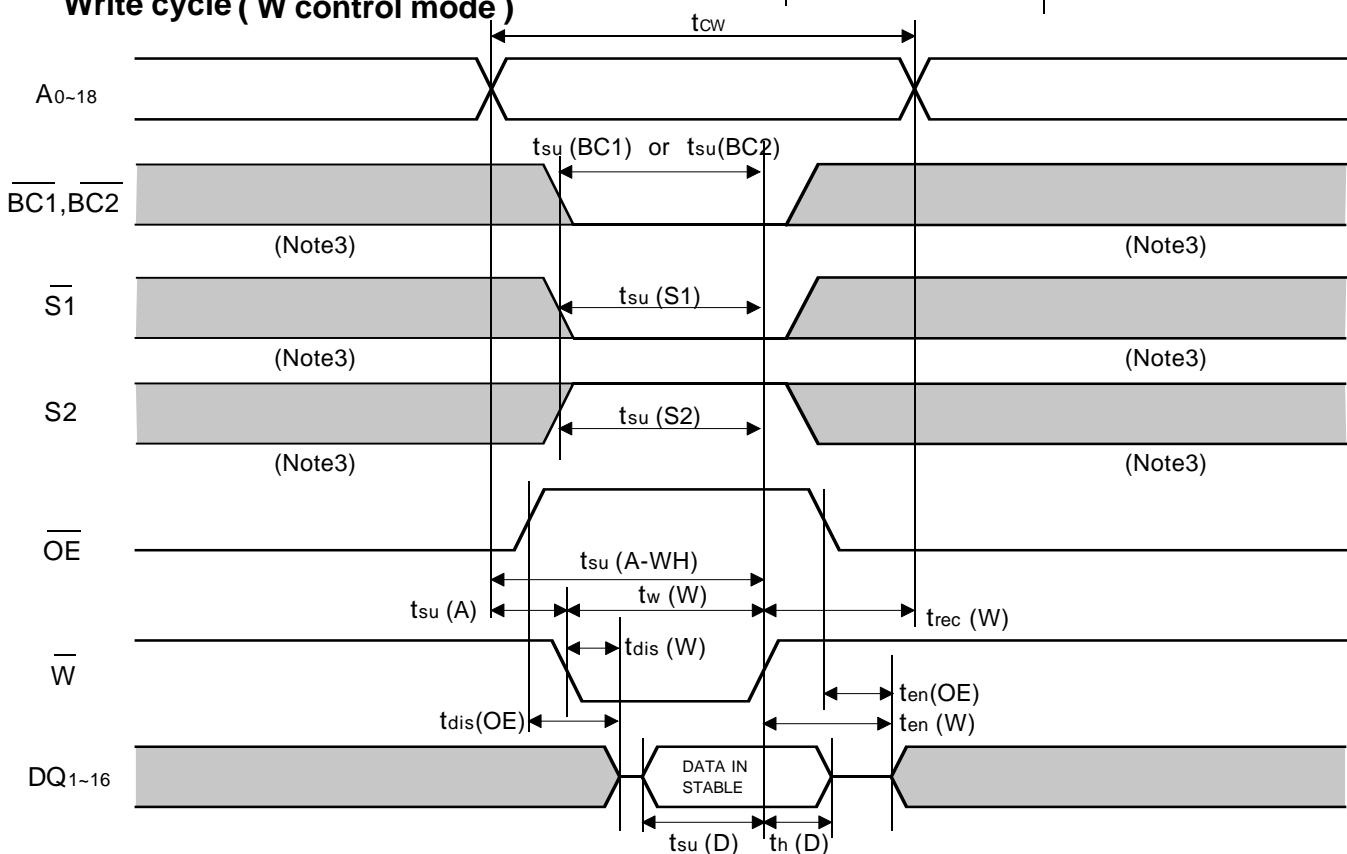
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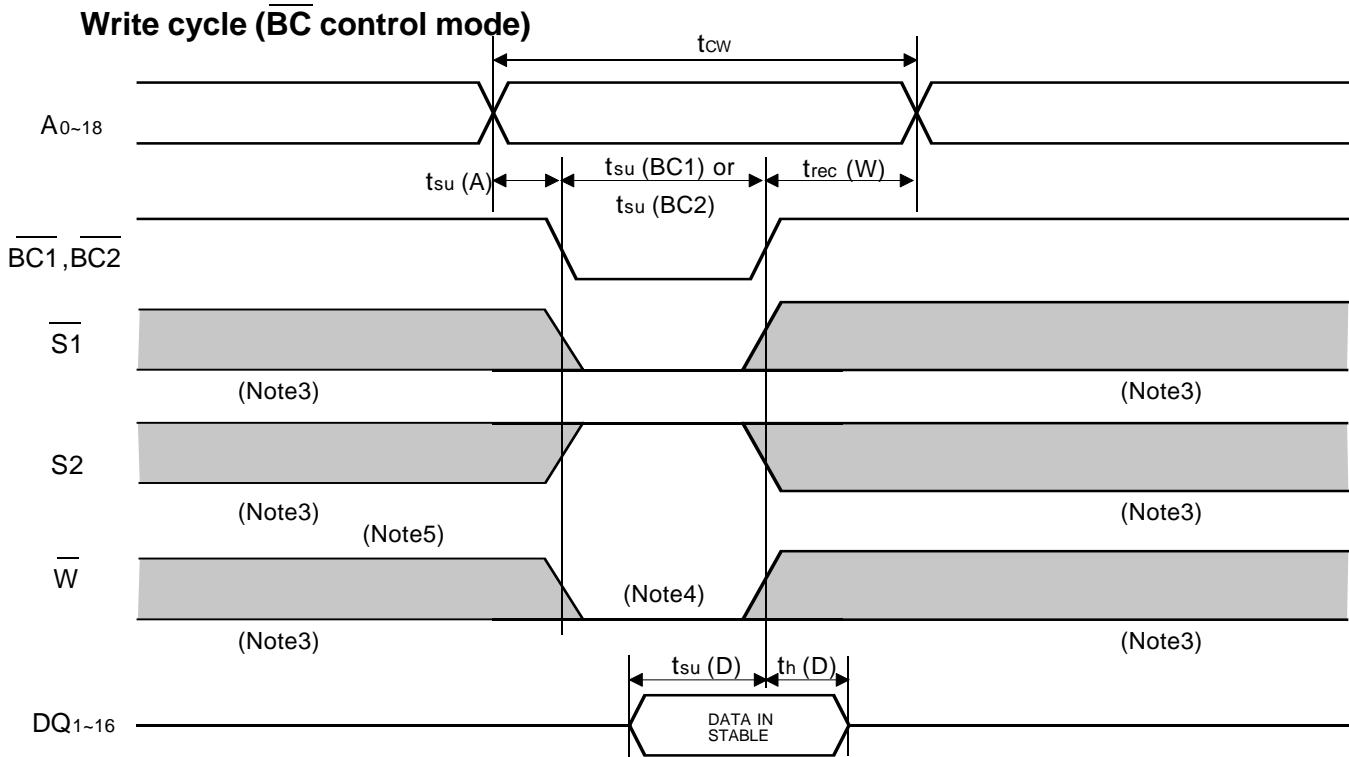
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(4) TIMING DIAGRAMS**Read cycle****Write cycle (W control mode)**

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Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during $\overline{S1}$ low, S2 high overlaps $\overline{BC1}$ and/or $\overline{BC2}$ low and \overline{W} low.

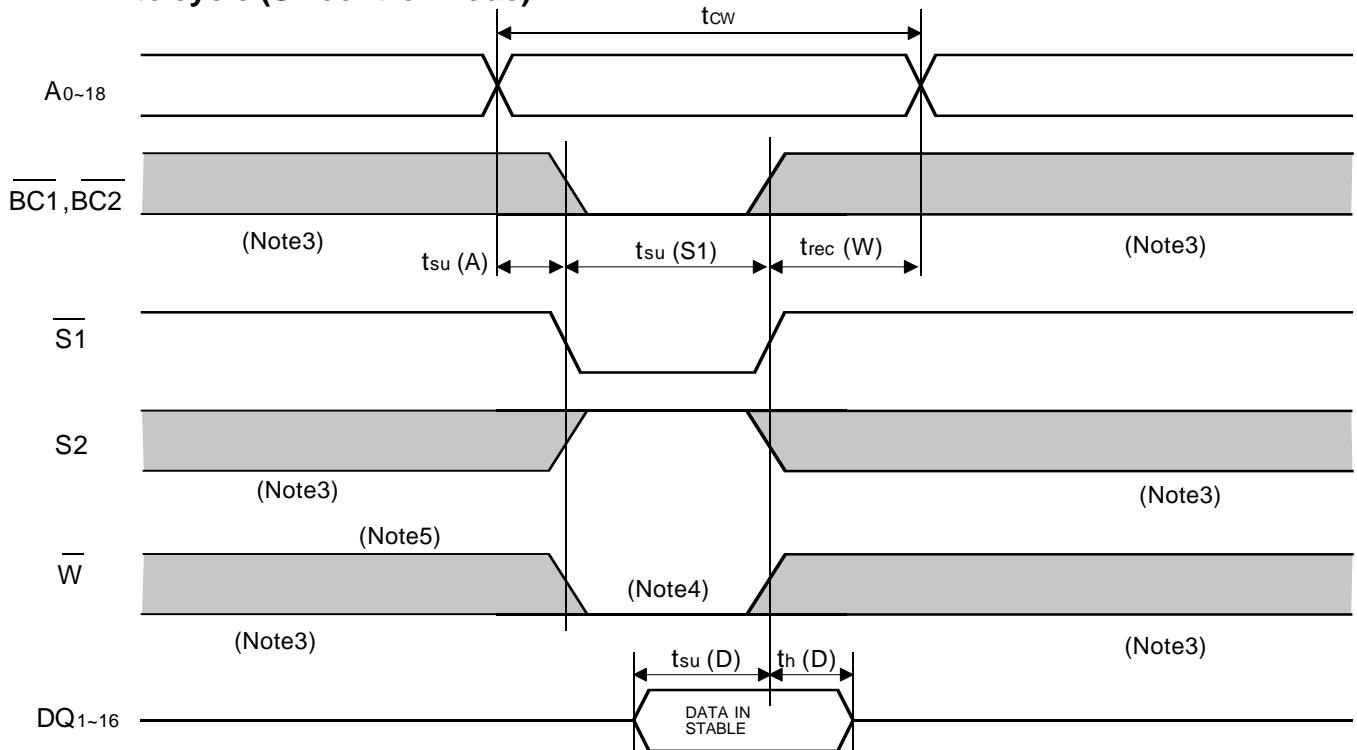
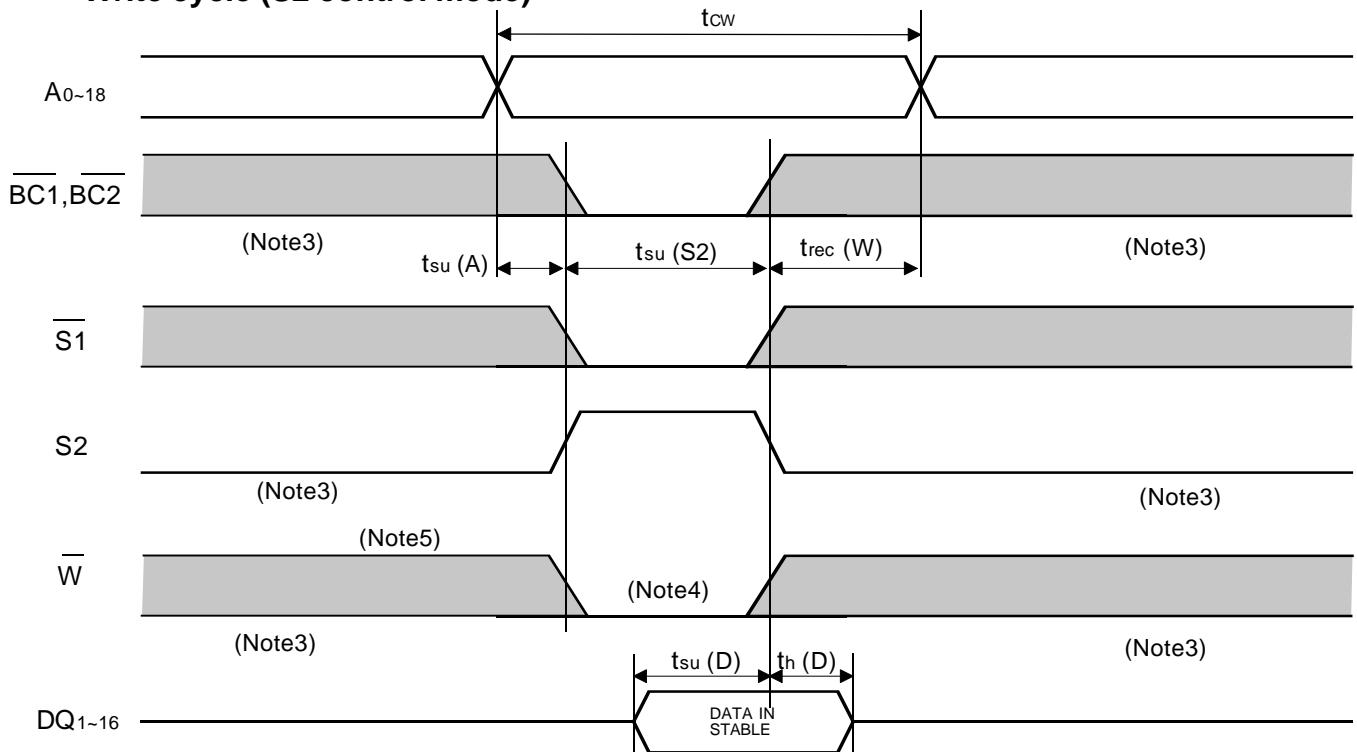
Note 5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of $\overline{BC1}$ and/or $\overline{BC2}$ or the falling edge of $\overline{S1}$ or rising edge of S2, the outputs are maintained in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.



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M5M5Y816WG -70HI, -85HI**8388608-BIT (524288-WORD BY 16-BIT) CMOS STATIC RAM****Write cycle (S1 control mode)****Write cycle (S2 control mode)**

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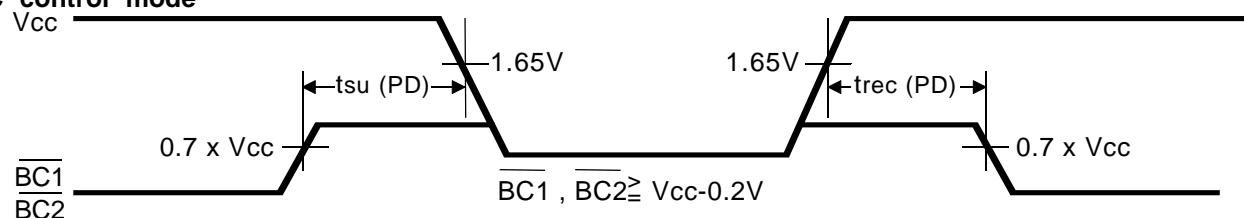
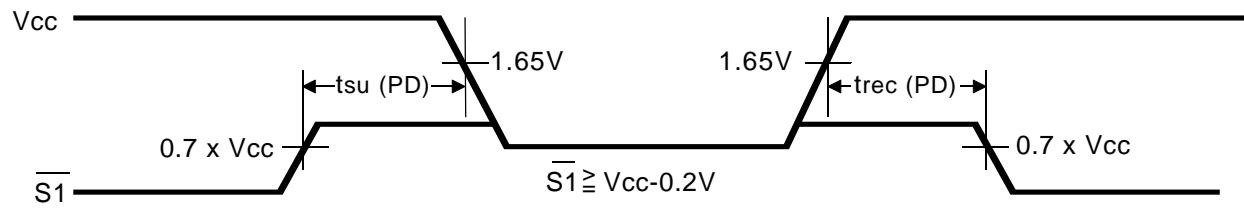
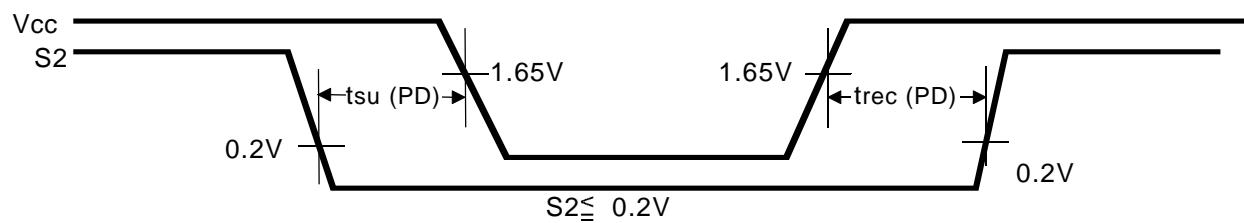
POWER DOWN CHARACTERISTICS**(1) ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test conditions	Limits			Units	
			Min	Typ	Max		
V _{cc} (PD)	Power down supply voltage		1.3			V	
V _I (BC)	Byte control input $\overline{BC1}$ & $\overline{BC2}$	1.65V \leq V _{cc} (PD)	0.7xV _{cc}			V	
		1.3V \leq V _{cc} (PD) \leq 1.65V			V _{cc} (PD)		
V _I (S1)	Chip select input $\overline{S1}$	1.65V \leq V _{cc} (PD)	0.7xV _{cc}			V	
		1.3V \leq V _{cc} (PD) \leq 1.65V			V _{cc} (PD)		
V _I (S2)	Chip select input S2				0.2	V	
I _{cc} (PD)	Power down supply current	$V_{cc}=1.3V$ (1) $\overline{S1} \geq V_{cc} - 0.2V$, other inputs = 0 ~ V _{cc} (2) $S2 \leq 0.2V$, other inputs = 0 ~ V _{cc} (3) $\overline{BC1}$ and $\overline{BC2} \geq V_{cc} - 0.2V$ $\overline{S1} \leq 0.2V$, $S2 \geq V_{cc} - 0.2V$ other inputs = 0 ~ V _{cc}	~ +25°C	-	0.1	1.5	μA
			~ +40°C	-	0.2	3	
			~ +70°C	-	-	10	
			~ +85°C	-	-	20	

Note 2: Typical parameter of I_{cc}(PD) indicates the value for the center of distribution at 1.3V, and not 100% tested.

(2) TIMING REQUIREMENTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM**BC control mode****S1 control mode****S2 control mode**

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Revision History

Ver. 0.0 / May.07.2001 Initial

Ver. 0.1 / May.22.2001 Change of package name 48FJA ---> 48F7Q <Page1>



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