DATA SHEET

MOS INTEGRATED CIRCUIT

μPD4564323 for Rev. E

64M-bit Synchronous DRAM
4-bank, LVTTL

Description

The μPD4564323 is a high-speed 67,108,864-bit synchronous dynamic random-access memory, organized as 524,288 words × 32 bits × 4 banks.

The synchronous DRAMs achieved high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAMs are compatible with Low Voltage TTL (LVTTL).

These products are packaged in 86-pin TSOP (II).

Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- ×32 organization
- Byte control by DQM0, DQM1, DQM2 and DQM3
- Programmable Wrap sequence (Sequential / Interleave)
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable /CAS latency (2 and 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- Single 3.3 V ± 0.3 V power supply
- LVTTL compatible inputs and outputs
- 4,096 refresh cycles / 64 ms
- Burst termination by Burst stop command and Precharge command

Document No. M14376EJ2V0DS00 (2nd edition)
Date Published December 1999 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

★ Ordering Information

Part number	Organization (word × bit × bank)	Clock frequency MHz (MAX.)	Package
μPD4564323G5-A60-9JH	512K × 32 × 4	166	86-pin Plastic TSOP (II) (10.16 mm (400))
μPD4564323G5-A70-9JH		143	
μPD4564323G5-A80-9JH		125	
μPD4564323G5-A10-9JH		100	
μPD4564323G5-A10B-9JH		100	

★ **Part Number**

μPD4564323G5 - A60

- NEC Memory: μPD
- Synchronous DRAM: 45
- Memory Density: 64
  - 64 : 64M bits
- Organization: 32
  - 32 : x32
- Number of Banks & Interface: 3
  - 3 : 4Bank, LVTTL
- Package: G5
  - G5 : TSOP(II)
- Low Voltage: A
  - A : 3.3 ± 0.3 V
- Minimum Cycle Time: 60
  - 60 : 6 ns (166MHz)
  - 70 : 7 ns (143MHz)
  - 80 : 8 ns (125MHz)
  - 10 : 10 ns (100MHz)
  - 10B : 10 ns (100MHz)

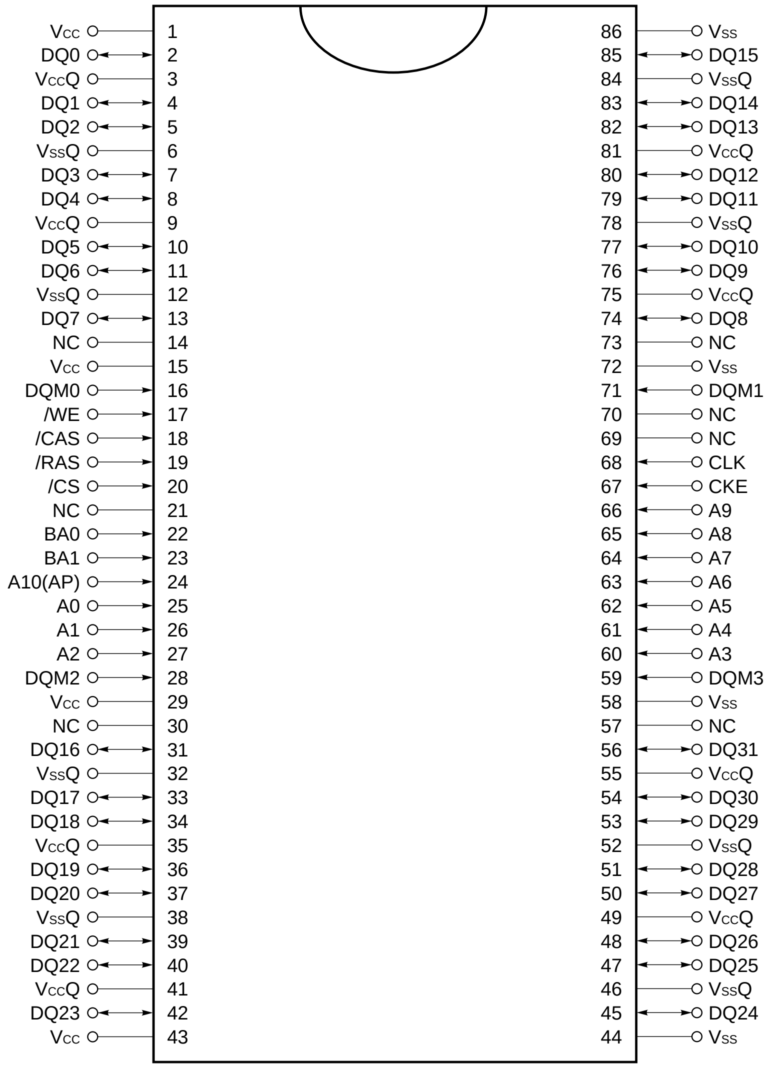
Pin Configuration

/xxx indicates active low signal.

[μPD4564323]

86-pin Plastic TSOP (II) (10.16 mm (400))

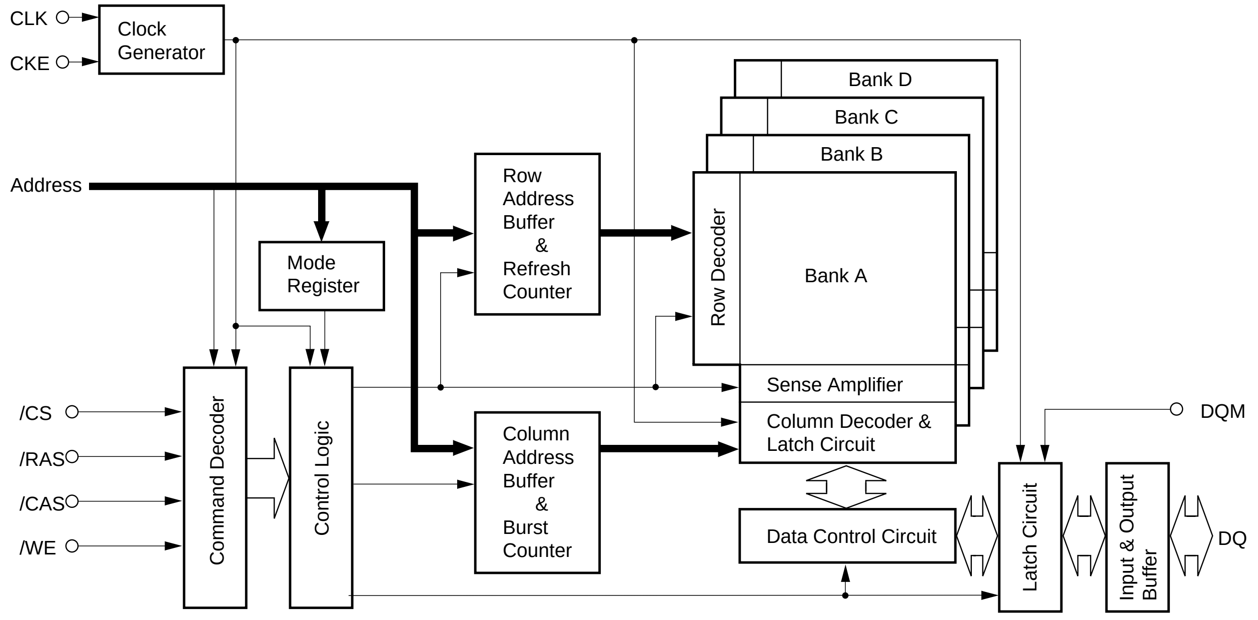
512K words × 32 bits × 4 banks



A0 to A10 [Note]	: Address inputs
BA0, BA1	: Bank select
DQ0 to DQ31	: Data inputs / outputs
CLK	: Clock input
CKE	: Clock enable
/CS	: Chip select
/RAS	: Row address strobe
/CAS	: Column address strobe
/WE	: Write enable
DQM0 to DQM3	: DQ mask enable
VCC	: Supply voltage
VSS	: Ground
VCCQ	: Supply voltage for DQ
VSSQ	: Ground for DQ
NC	: No connection

Note A0 to A10 : Row address inputs
A0 to A7 : Column address inputs

Block Diagram



CONTENTS

1. Input / Output Pin Function

Pin name	Input / Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the μPD4564323 suspends operation. When the μPD4564323 is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.
/CS	Input	/CS low starts the command input cycle. When /CS is high, commands are ignored but operations continue.
/RAS, /CAS, /WE	Input	/RAS, /CAS and /WE have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
A0 - A10	Input	Row Address is determined by A0 - A10 at the CLK (clock) rising edge in the active command cycle. Column Address is determined by A0 - A7 at the CLK rising edge in the read or write command cycle. A10 defines the precharge mode. When A10 is high in the precharge command cycle, all banks are precharged; when A10 is low, only the bank selected by BA0 and BA1 is precharged. When A10 is high in read or write command cycle, the precharge starts automatically after the burst access.
BA0, BA1	Input	BA0 and BA1 are the bank select signal. In command cycle, BA0 and BA1 low select bank A, BA0 low and BA1 high select bank C, BA0 high and BA1 low select bank B and then BA0 and BA1 high select bank D.
DQM0 - DQM3	Input	DQM controls I/O buffers. DQM0 controls DQ0 - DQ7, DQM1 controls DQ8 - DQ15, DQM2 controls DQ16 - DQ23, DQM3 controls DQ24 - DQ31. In read mode, DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ31	Input / Output	DQ pins have the same function as I/O pins on a conventional DRAM.
V_{CC}, V_{SS}, $V_{CC}Q$, $V_{SS}Q$	(Power supply)	V_{CC} and V_{SS} are power supply pins for internal circuits. $V_{CC}Q$ and $V_{SS}Q$ are power supply pins for the output buffers.

2. Commands

Mode register set command

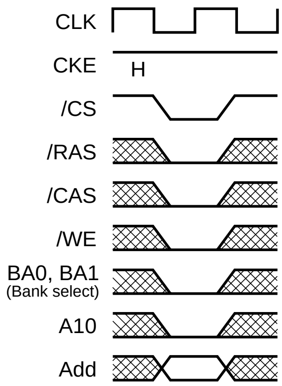
(/CS, /RAS, /CAS, /WE = Low)

The μPD4564323 has a mode register that defines how the device operates. In this command, A0 through A10, BA0 and BA1 are the data input pins. After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when all banks are in idle state.

During 2 CLK (t_{RSC}) following this command, the μPD4564323 cannot accept any other commands.

Fig.1 Mode register set command



Activate command

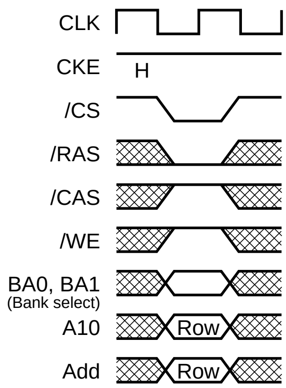
(/CS, /RAS = Low, /CAS, /WE = High)

The μPD4564323 has four banks, each with 4,096 rows.

This command activates the bank selected by BA0 and BA1 and a row address selected by A0 through A10.

This command corresponds to a conventional DRAM's /RAS falling.

Fig.2 Row address strobe and bank activate command



Precharge command

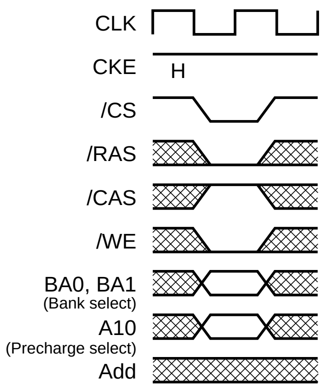
(/CS, /RAS, /WE = Low, /CAS = High)

This command begins precharge operation of the bank selected by BA0 and BA1. When A10 is High, all banks are precharged, regardless of BA0 and BA1. When A10 is Low, only the bank selected by BA0 and BA1 is precharged.

After this command, the μPD4564323 can't accept the activate command to the precharging bank during t_{RP} (precharge to activate command period).

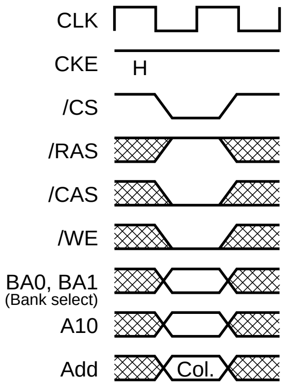
This command corresponds to a conventional DRAM's /RAS rising.

Fig.3 Precharge command



Write command

Fig.4 Column address and write command

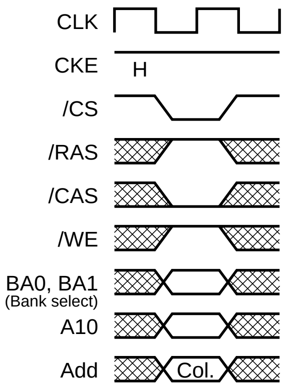


(/CS, /CAS, /WE = Low, /RAS = High)

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.

Read command

Fig.5 Column address and read command

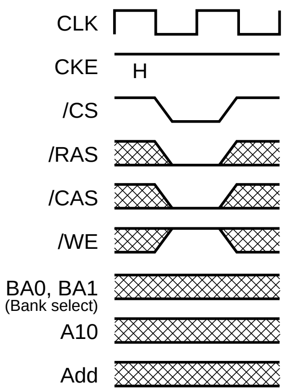


(/CS, /CAS = Low, /RAS, /WE = High)

Read data is available after /CAS latency requirements have been met. This command sets the burst start address given by the column address.

CBR (auto) refresh command

Fig.6 CBR (auto) refresh command



(/CS, /RAS, /CAS = Low, /WE, CKE = High)

This command is a request to begin the CBR (auto) refresh operation. The refresh address is generated internally.

Before executing CBR (auto) refresh, all banks must be precharged.

After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command.

During t_{RC} period (from refresh command to refresh or activate command), the μPD4564323 cannot accept any other command.

Self refresh entry command

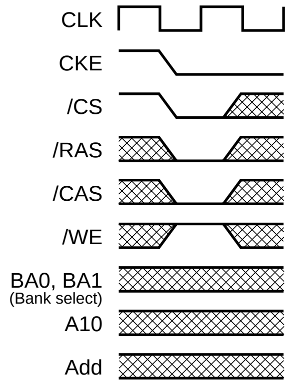
(/CS, /RAS, /CAS, CKE = Low, /WE = High)

After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the μPD4564323 exits the self refresh mode.

During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.

Before executing self refresh, all banks must be precharged.

Fig.7 Self refresh entry command

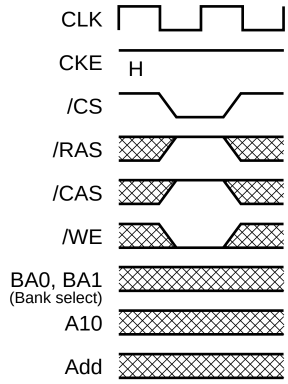


Burst stop command

(/CS, /WE = Low, /RAS, /CAS = High)

This command can stop the current burst operation.

Fig.8 Burst stop command in Full Page Mode

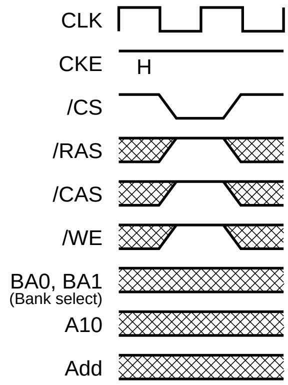


No operation

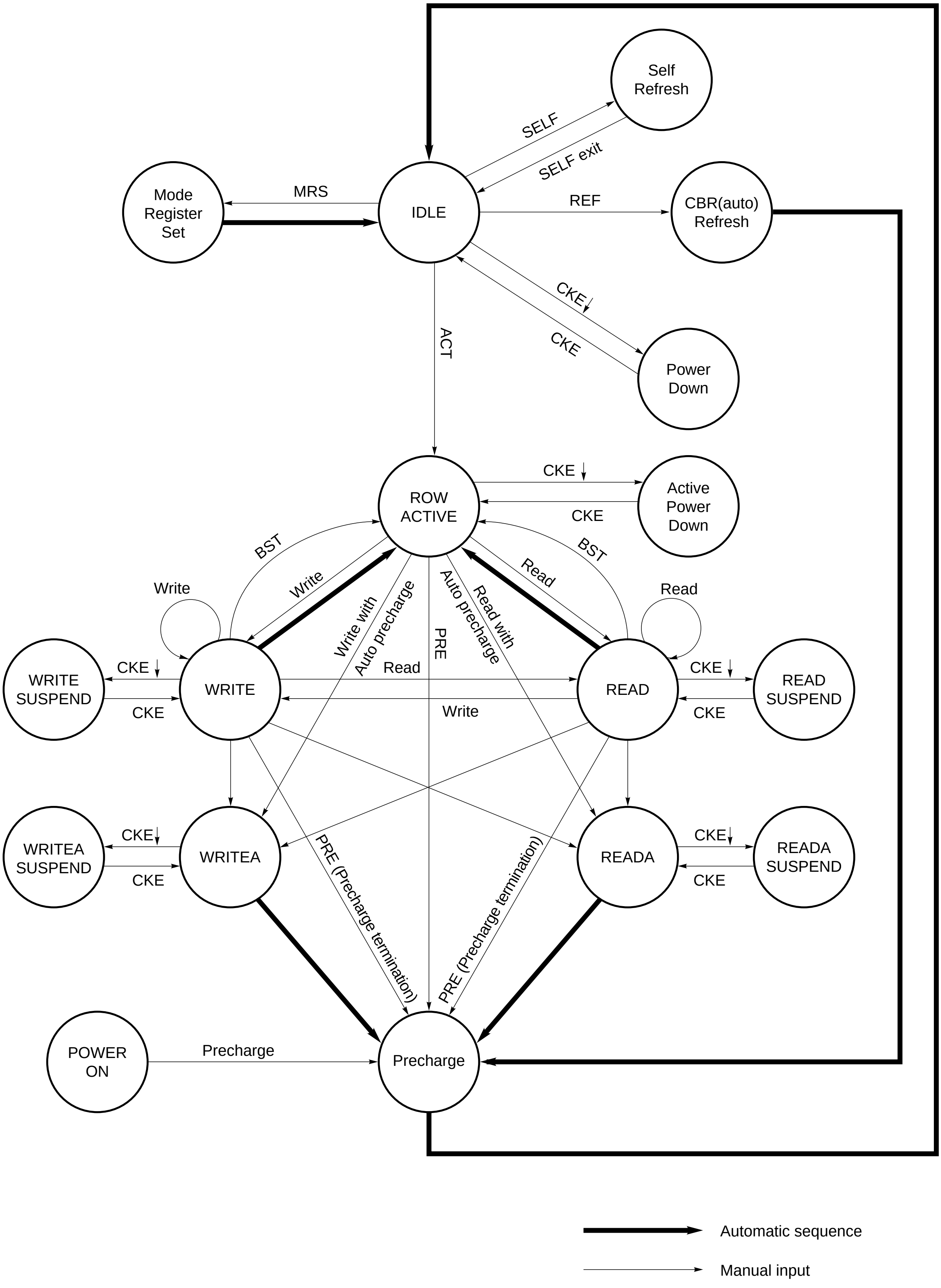
(/CS = Low, /RAS, /CAS, /WE = High)

This command is not an execution command. No operations begin or terminate by this command.

Fig.9 No operation



3. Simplified State Diagram



4. Truth Table

4.1 Command Truth Table

Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A9 - A0
		n – 1	n							
Device deselect	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Burst stop	BST	H	×	L	H	H	L	×	×	×
Read	READ	H	×	L	H	L	H	V	L	V
Read with auto precharge	READA	H	×	L	H	L	H	V	H	V
Write	WRIT	H	×	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	×	L	H	L	L	V	H	V
Bank activate	ACT	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge all banks	PALL	H	×	L	L	H	L	×	H	×
Mode register set	MRS	H	×	L	L	L	L	L	L	V

Remark H = High level, L = Low level, × = High or Low level (Don't care), V = Valid data input

4.2 DQM Truth Table

Function	Symbol	CKE		DQM			
		n-1	n	0	1	2	3
Data write/output enable	ENB	H	×	L			
Data mask/output disable	MASK	H	×	H			
DQ0 - DQ7 write enable/output enable	ENB0	H	×	L	×	×	×
DQ8 - DQ15 write enable/output enable	ENB1	H	×	×	L	×	×
DQ16 - DQ23 write enable/output enable	ENB2	H	×	×	×	L	×
DQ24 - DQ31 write enable/output enable	ENB3	H	×	×	×	×	L
DQ0 - DQ7 write inhibit/output disable	MASK0	H	×	H	×	×	×
DQ8 - DQ15 write inhibit/output disable	MASK1	H	×	×	H	×	×
DQ16 - DQ23 write inhibit/output disable	MASK2	H	×	×	×	H	×
DQ24 - DQ31 write inhibit/output disable	MASK3	H	×	×	×	×	H

Remark H = High level, L = Low level, × = High or Low level (Don't care)

4.3 CKE Truth Table

Current state	Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	Address
			n – 1	n					
Activating	Clock suspend mode entry		H	L	×	×	×	×	×
Any	Clock suspend		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	H	×	×	×	×	×
Idle	CBR (auto) refresh command	REF	H	H	L	L	L	H	×
Idle	Self refresh entry	SELF	H	L	L	L	L	H	×
Self refresh	Self refresh exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Idle	Power down entry		H	L	×	×	×	×	×
Power down	Power down exit		L	H	H	×	×	×	×
			L	H	L	H	H	H	×

Remark H = High level, L = Low level, × = High or Low level (Don't care)

4.4 Operative Command Table [Note1]

(1/3)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Idle	H	×	×	×	×	DESL	Nop or power down	2
	L	H	H	×	×	NOP or BST	Nop or power down	2
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	×	REF/SELF	CBR (auto) refresh or self refresh	4
	L	L	L	L	Op-Code	MRS	Mode register accessing	
Row active	H	×	×	×	×	DESL	Nop	
	L	H	H	×	×	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read : Determine AP	5
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write : Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Precharge	6
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end → Row active	
	L	H	H	H	×	NOP	Continue burst to end → Row active	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, new read : Determine AP	7
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, start write : Determine AP	7, 8
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, precharging	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP	7, 8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP	7
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, precharging	9
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/3)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Read with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Precharging	
	L	H	H	H	×	NOP	Continue burst to end → Precharging	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Precharging	H	×	×	×	×	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	×	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop → Enter bank active after t_{RCD}	
	L	H	H	H	×	NOP	Nop → Enter bank active after t_{RCD}	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3, 10
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(3/3)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Write recovering	H	×	×	×	×	DESL	Nop → Enter row active after t_{DPL}	
	L	H	H	H	×	NOP	Nop → Enter row active after t_{DPL}	
	L	H	H	L	×	BST	Nop → Enter row active after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	Start read, Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering with auto precharge	H	×	×	×	×	DESL	Nop → Enter precharge after t_{DPL}	
	L	H	H	H	×	NOP	Nop → Enter precharge after t_{DPL}	
	L	H	H	L	×	BST	Nop → Enter precharge after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3, 8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	H	×	×	×	×	DESL	Nop → Enter idle after t_{RC}	
	L	H	H	×	×	NOP/BST	Nop → Enter idle after t_{RC}	
	L	H	L	×	×	READ/WRIT	ILLEGAL	
	L	L	H	×	×	ACT/PRE/PALL	ILLEGAL	
	L	L	L	×	×	REF/SELF/MRS	ILLEGAL	
Mode register accessing	H	×	×	×	×	DESL	Nop → Enter idle after t_{RSC}	
	L	H	H	H	×	NOP	Nop → Enter idle after t_{RSC}	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	×	×	READ/WRIT	ILLEGAL	
	L	L	×	×	×	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

Notes 1. All entries assume that CKE was active (High level) during the preceding clock cycle.

2. If all banks are idle, and CKE is inactive (Low level), μPD4564323 will enter Power down mode. All input buffers except CKE will be disabled.

3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

4. If all banks are idle, and CKE is inactive (Low level), μPD4564323 will enter Self refresh mode. All input buffers except CKE will be disabled.

5. Illegal if t_{RCD} is not satisfied.

6. Illegal if t_{RAS} is not satisfied.

7. Must satisfy burst interrupt condition.

8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.

9. Must mask preceding data which don't satisfy t_{DPL}.

10. Illegal if t_{RRD} is not satisfied.

Remark H = High level, L = Low level, × = High or Low level (Don't care), V = Valid data

4.5 Command Truth Table for CKE

Current State	CKE		/CS	/RAS	/CAS	/WE	Address	Action	Notes
	n – 1	n							
Self refresh	H	×	×	×	×	×	×	INVALID, CLK (n-1) would exit self refresh	
	L	H	H	×	×	×	×	Self refresh recovery	
	L	H	L	H	H	×	×	Self refresh recovery	
	L	H	L	H	L	×	×	ILLEGAL	
	L	H	L	L	×	×	×	ILLEGAL	
	L	L	×	×	×	×	×	Maintain self refresh	
Self refresh recovery	H	H	H	×	×	×	×	Idle after t_{RC}	
	H	H	L	H	H	×	×	Idle after t_{RC}	
	H	H	L	H	L	×	×	ILLEGAL	
	H	H	L	L	×	×	×	ILLEGAL	
	H	L	H	×	×	×	×	ILLEGAL	
	H	L	L	H	H	×	×	ILLEGAL	
	H	L	L	H	L	×	×	ILLEGAL	
	H	L	L	L	×	×	×	ILLEGAL	
Power down	H	×	×	×	×	×		INVALID, CLK (n – 1) would exit power down	
	L	H	H	×	×	×	×	EXIT power down → Idle	
	L	H	L	H	H	H	×		
	L	L	×	×	×	×	×	Maintain power down mode	
All banks idle	H	H	H	×	×	×		Refer to operations in Operative Command Table	
	H	H	L	H	×	×		Refer to operations in Operative Command Table	
	H	H	L	L	H	×		Refer to operations in Operative Command Table	
	H	H	L	L	L	H	×	CBR (auto) refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	×	×	×		Refer to operations in Operative Command Table	
	H	L	L	H	×	×		Refer to operations in Operative Command Table	
	H	L	L	L	H	×		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	×	Self refresh	1
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	×	×	×	×	×	×	Power down	1
Row active	H	×	×	×	×	×	×	Refer to operations in Operative Command Table	
	L	×	×	×	×	×	×	Power down	1
Any state other than listed above	H	H	×	×	×	×		Refer to operations in Operative Command Table	
	H	L	×	×	×	×	×	Begin clock suspend next cycle	2
	L	H	×	×	×	×	×	Exit clock suspend next cycle	
	L	L	×	×	×	×	×	Maintain clock suspend	

Notes 1. Self refresh can be entered only from the all banks idle state. Power down can be entered only from all banks idle or row active state.

2. Must be legal command as defined in Operative Command Table.

Remark H = High level, L = Low level, × = High or Low level (Don't care)

5. Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 100 μs or longer pause must precede any signal toggling.

(2) After the pause, all banks must be precharged using the Precharge command (The Precharge all banks command is convenient).

(3) Once the precharge is completed and the minimum t_{RP} is satisfied, the mode register can be programmed. After the mode register set cycle, t_{RSC} (2 CLK minimum) pause must be satisfied as well.

(4) Two or more CBR (Auto) refresh must be performed.

Remarks **1.** The sequence of Mode register programming and Refresh above may be transposed.
2. CKE and DQM must be held high until the Precharge command is issued to ensure data-bus Hi-Z.

6. Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits A10 through A0, BA0 and BA1 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options	:	A10 through A7, BA0, BA1
/CAS latency	:	A6 through A4
Wrap type	:	A3
Burst length	:	A2 through A0

Following mode register programming, no command can be issued before at least 2 CLK have elapsed.

/CAS Latency

/CAS latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available.

The value is determined by the frequency of the clock and the speed grade of the device. **13.3 Relationship between Frequency and Latency** shows the relationship of /CAS latency to the clock period and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become Hi-Z.

The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. **7.1 Burst Length and Sequence** shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequence supports the full page length.

7. Mode Register

BA1	BA0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	1								JEDEC Standard Test Set (refresh counter test)

BA1	BA0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
x	x	x	1	0	0	LTMODE			WT	BL			Burst Read and Single Write (for Write Through Cache)

BA1	BA0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
				1	0								Use in future

BA1	BA0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
x	x	x	x	1	1	V	V	V	V	V	V	V	Vender Specific

V = Valid
x = Don' t care

BA1	BA0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	LTMODE			WT	BL			Mode Register Set

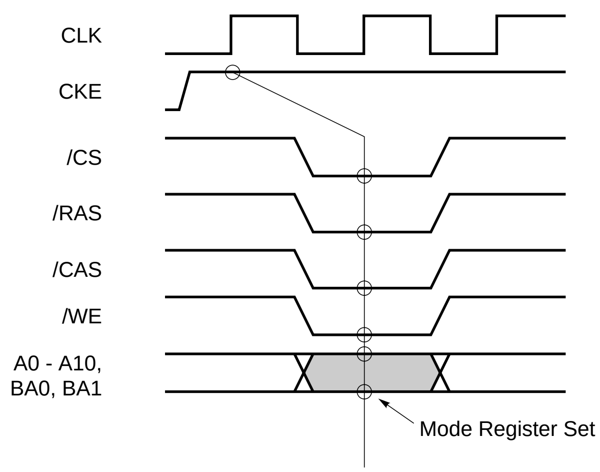
Burst length	Bits2-0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type		
	0	Sequential
	1	Interleave

Latency mode	Bits6-4	/CAS latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R : Reserved

Mode Register Set Timing



7.1 Burst Length and Sequence

[Burst of Two]

Starting address (column address A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

Starting address (column address A1 - A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting address (column address A2 - A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of sequential addressing, with the length being 256.

8. Address Bits of Bank-Select and Precharge

Row (Activate command)

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	BA0	BA1

BA1	BA0	Result
0	0	**Select Bank A “Activate” command**
0	1	**Select Bank B “Activate” command**
1	0	**Select Bank C “Activate” command**
1	1	**Select Bank D “Activate” command**

(Precharge command)

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	BA0	BA1

A10	BA1	BA0	Result
0	0	0	**Precharge Bank A**
0	0	1	**Precharge Bank B**
0	1	0	**Precharge Bank C**
0	1	1	**Precharge Bank D**
1	x	x	**Precharge All Banks**

x : Don’t care

Col. (/CAS strobes)

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	BA0	BA1

0	**disables Auto-Precharge (End of Burst)**
1	**enables Auto-Precharge (End of Burst)**

BA1	BA0	Result
0	0	**enables Read/Write commands for Bank A**
0	1	**enables Read/Write commands for Bank B**
1	0	**enables Read/Write commands for Bank C**
1	1	**enables Read/Write commands for Bank D**

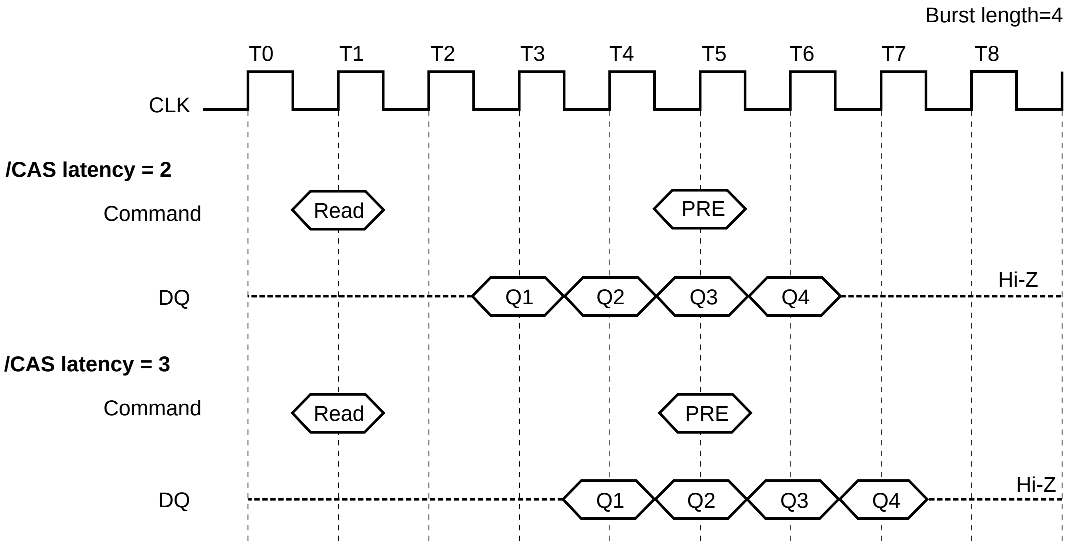
9. Precharge

The precharge command can be issued anytime after $t_{RAS\ (MIN.)}$ is satisfied.

Soon after the precharge command is issued, precharge operation performed and the synchronous DRAM enters the idle state after t_{RP} is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.

It is depending on the /CAS latency and clock cycle time.



(t_{RAS} must be satisfied)

In order to write all data to the memory cell correctly, the asynchronous parameter "t_{DPL}" must be satisfied. The $t_{DPL(MIN.)}$ specification defines the earliest time that a precharge command can be issued. Minimum number of clocks is calculated by dividing $t_{DPL(MIN.)}$ with clock cycle time.

In summary, the precharge command can be issued relative to reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

/CAS latency	Read	Write
2	–1	+$t_{DPL\ (MIN.)}$
3	–2	+$t_{DPL\ (MIN.)}$

10. Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the Read or Write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically.

The t_{RAS} must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.

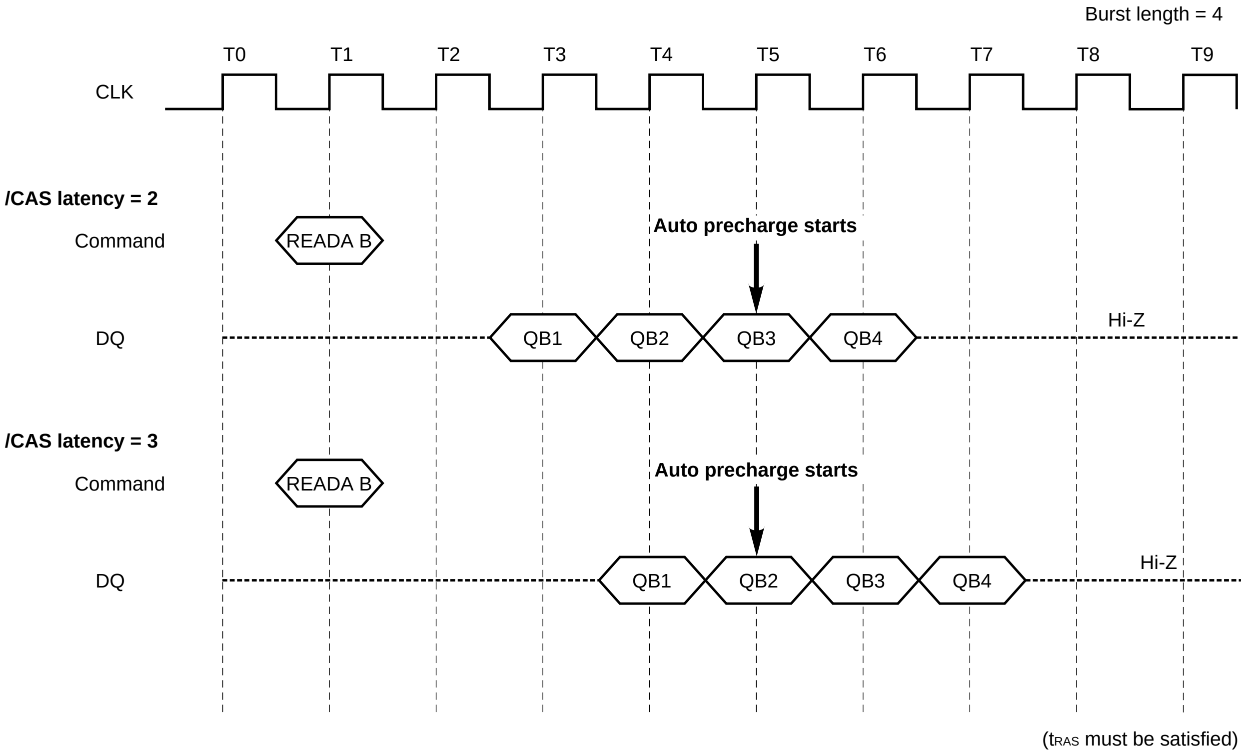
In read cycle, once auto precharge has started, an activate command to the bank can be issued after t_{RP} has been satisfied.

In write cycle, the t_{DAL} must be satisfied to issue the next activate command to the bank being precharged.

The timing that begins the auto precharge cycle depends on both the /CAS latency programmed into the mode register and whether read or write cycle.

10.1 Read with Auto Precharge

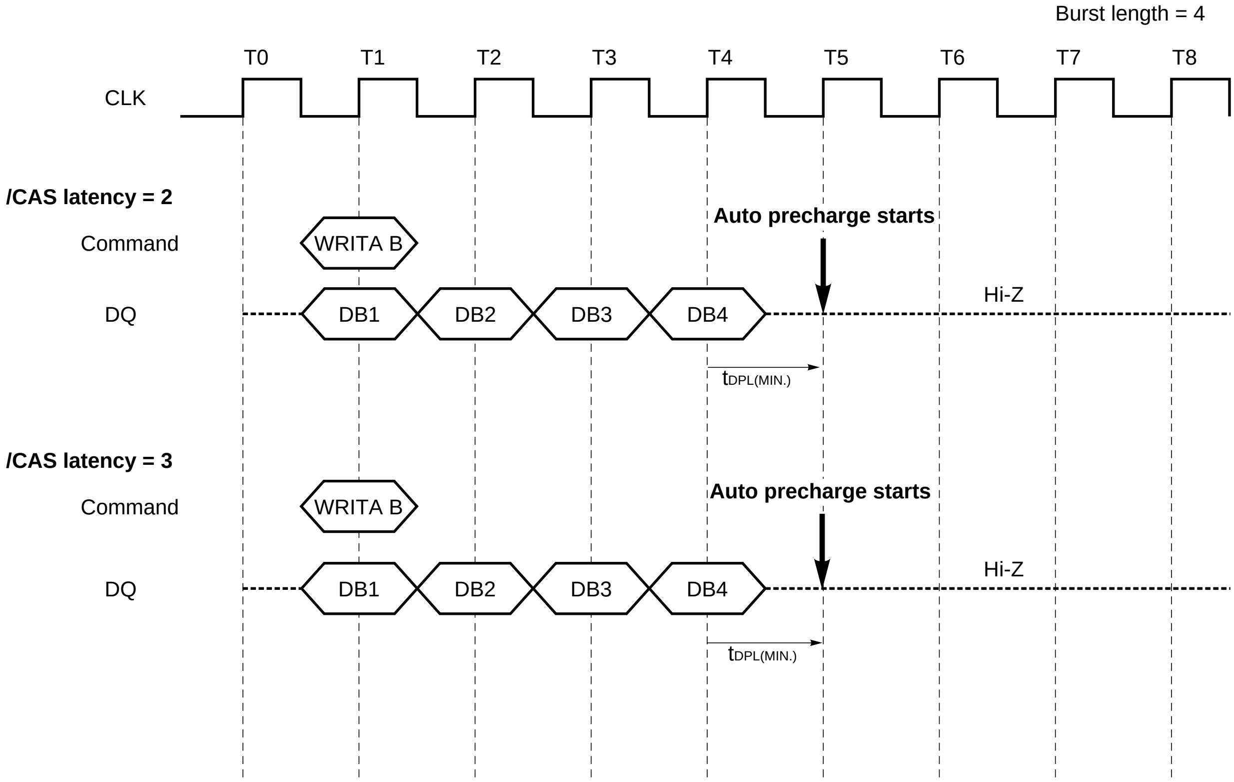
During a read cycle, the auto precharge begins one clock earlier (/CAS latency of 2) or two clocks earlier (/CAS latency of 3) the last data word output.



Remark READA means Read with Auto precharge

10.2 Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing that is equal to the value of the $t_{DPL\ (MIN.)}$ after the last data word input to the device.



(t_{RAS} must be satisfied)

Remark WRITA means Write with Auto Precharge

In summary, the auto precharge begins relative to a reference clock that indicates the last data word is valid.
In the table below, minus means clocks before the reference; plus means after the reference.

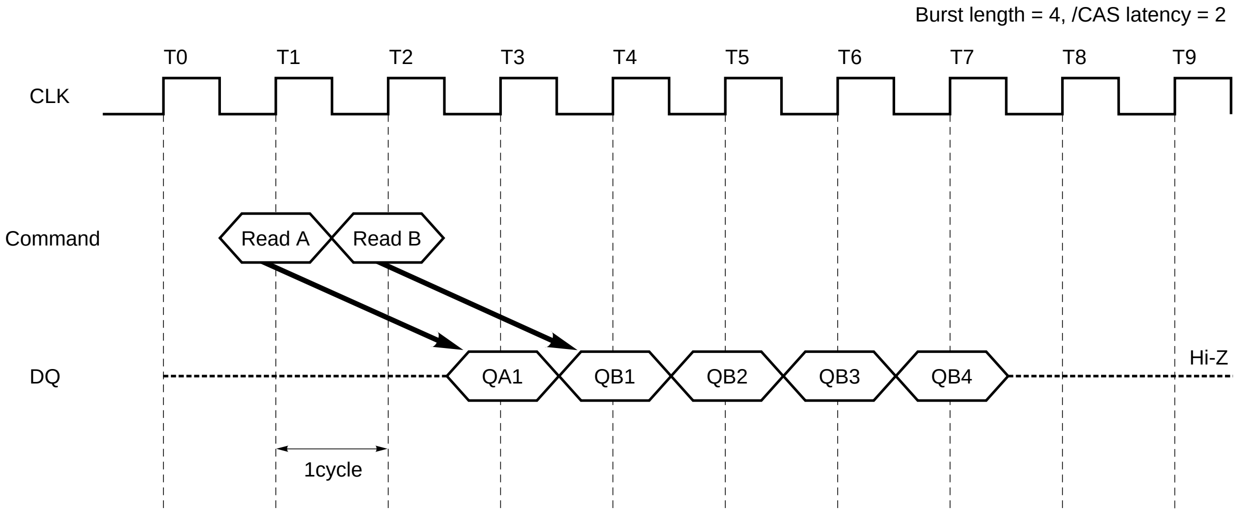
/CAS latency	Read	Write
2	–1	$+t_{DPL\ (MIN.)}$
3	–2	$+t_{DPL\ (MIN.)}$

11. Read / Write Command Interval

11.1 Read to Read Command Interval

During a read cycle, when new Read command is issued, it will be effective after /CAS latency, even if the previous read operation does not completed. READ will be interrupted by another READ.

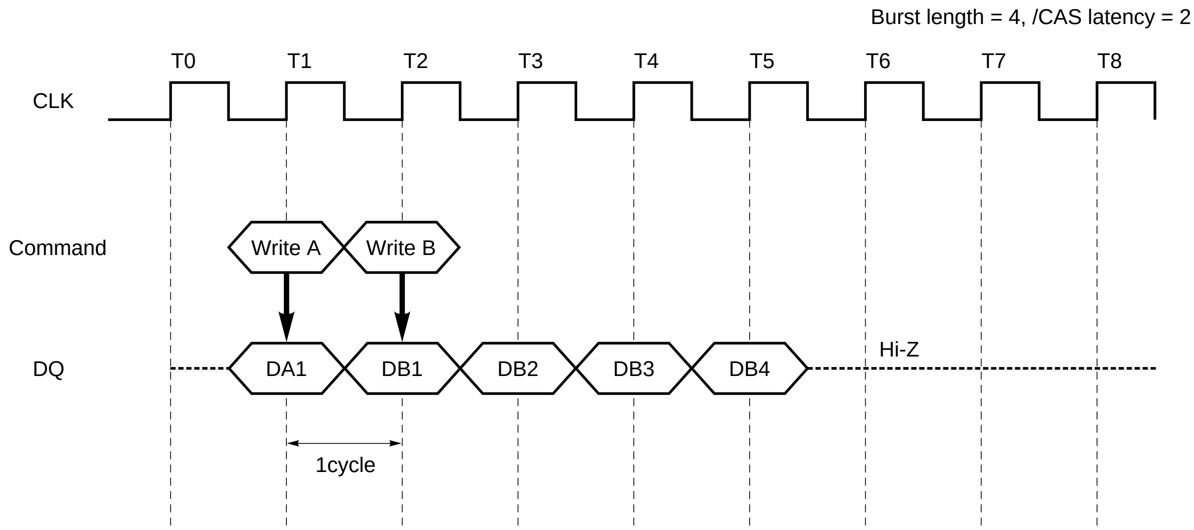
The interval between the commands is 1 cycle minimum. Each Read command can be issued in every clock without any restriction.



11.2 Write to Write Command Interval

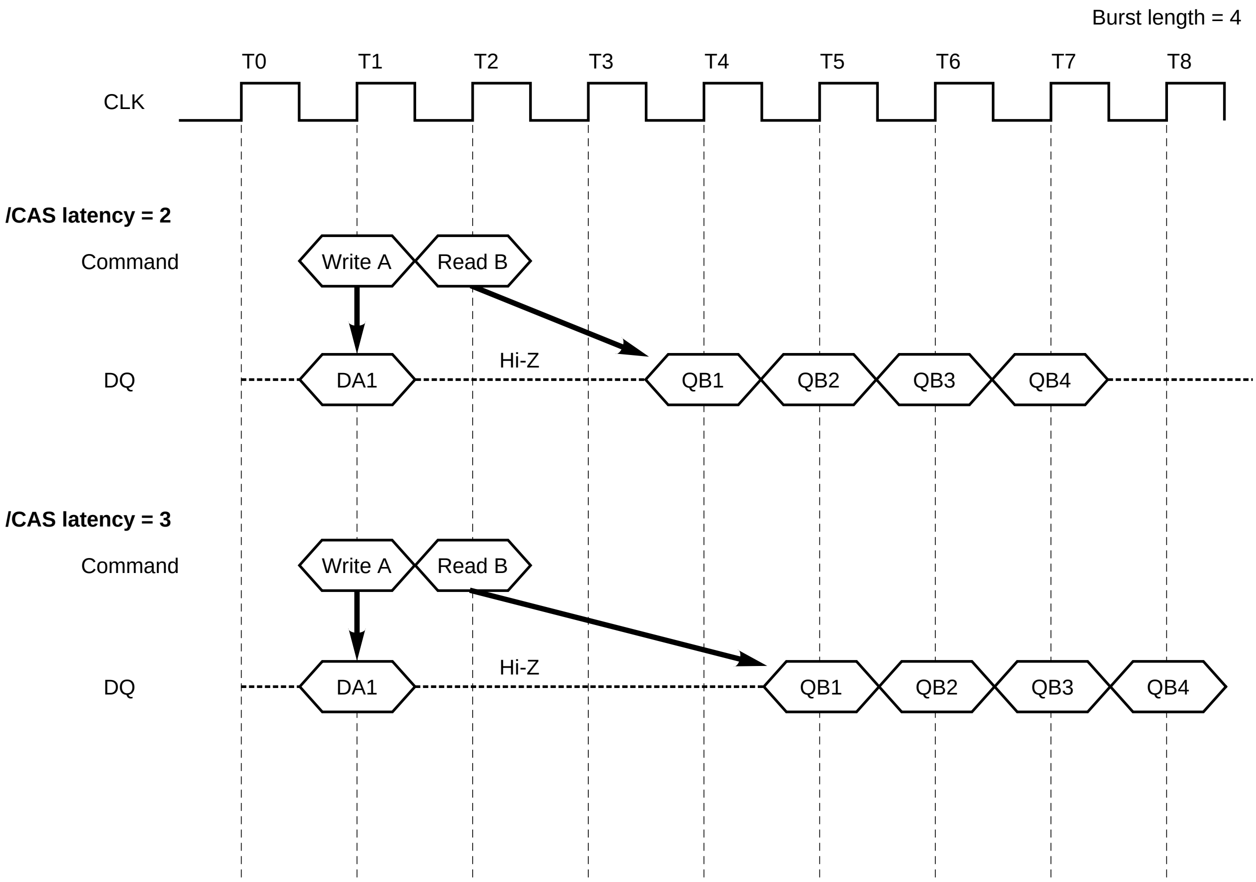
During a write cycle, when a new Write command is issued, the previous burst will terminate and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE.

The interval between the commands is minimum 1 cycle. Each Write command can be issued in every clock without any restriction.



11.3 Write to Read Command Interval

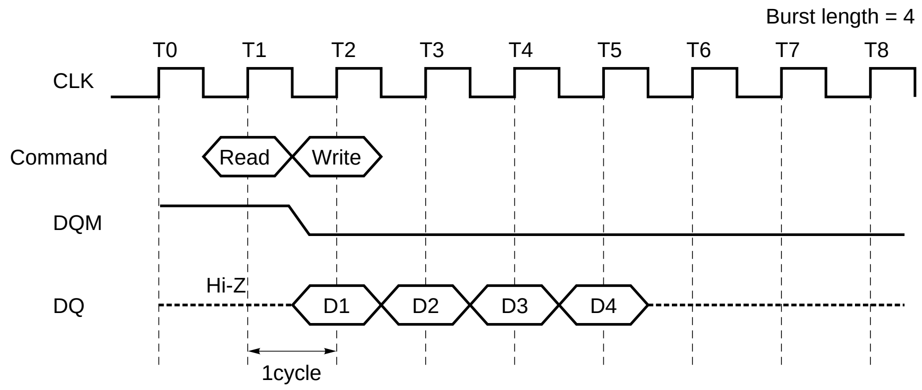
Write command and Read command interval is also 1 cycle.
Only the write data before Read command will be written.
The data bus must be Hi-Z at least one cycle prior to the first DOUT.



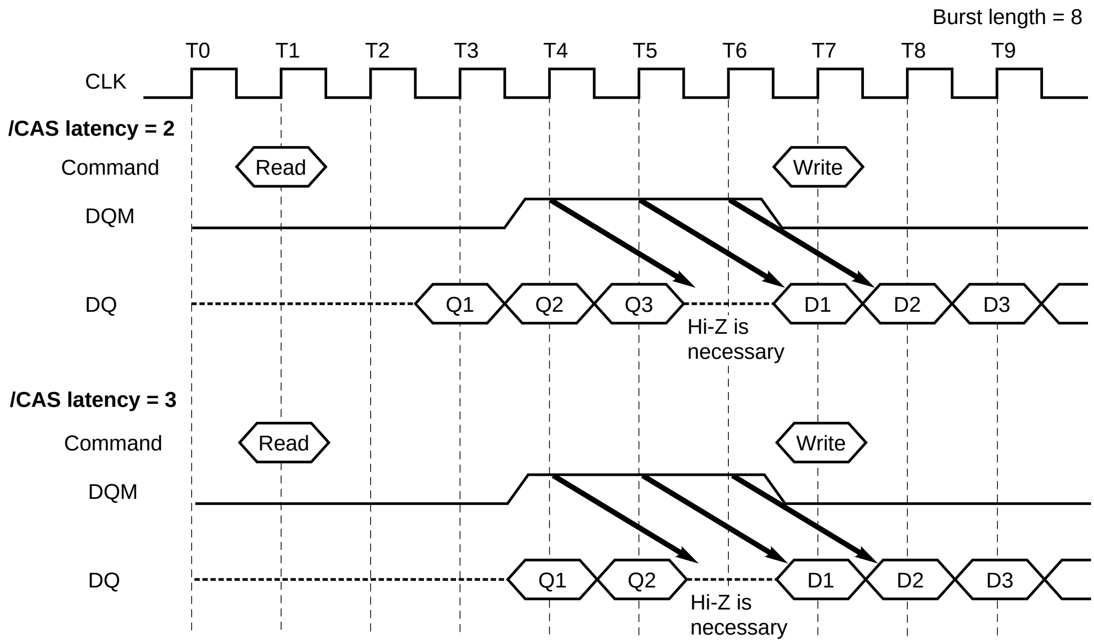
11.4 Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE.

The Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The Data bus must be Hi-Z using DQM before WRITE.



READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.

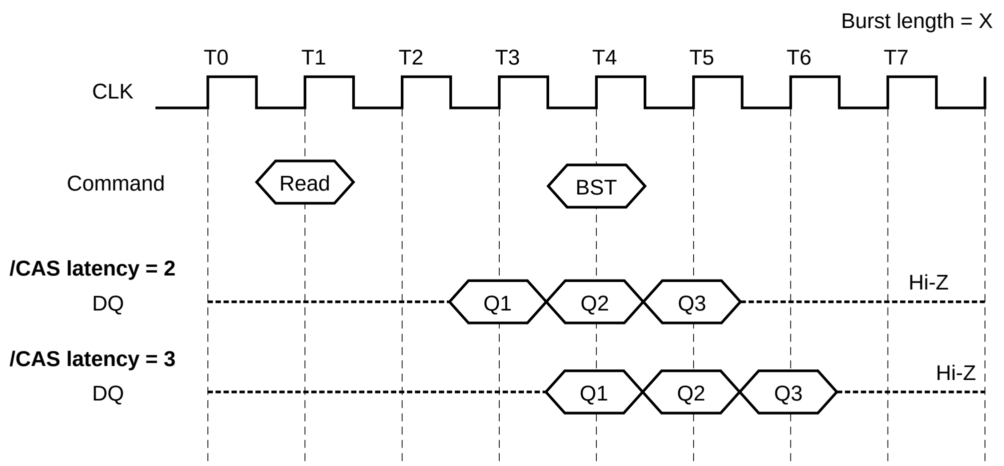


12. Burst Termination

There are two methods to terminate a burst operation other than using a Read or a Write command. One is the burst stop command and the other is the precharge command.

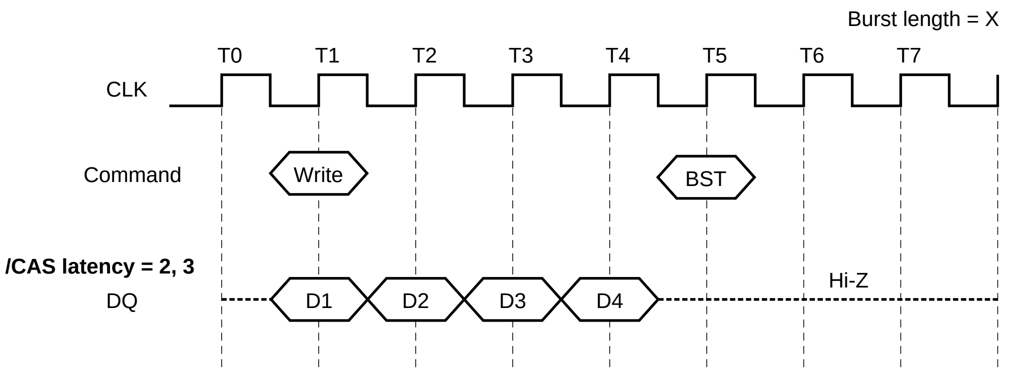
12.1 Burst Stop Command

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to Hi-Z after the /CAS latency from the burst stop command.



Remark BST: Burst stop command

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to Hi-Z at the same clock with the burst stop command.



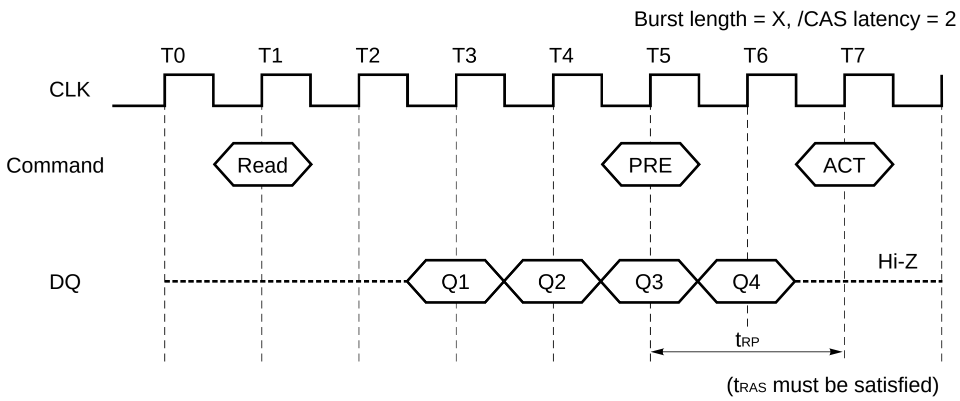
Remark BST: Burst stop command

12.2 Precharge Termination

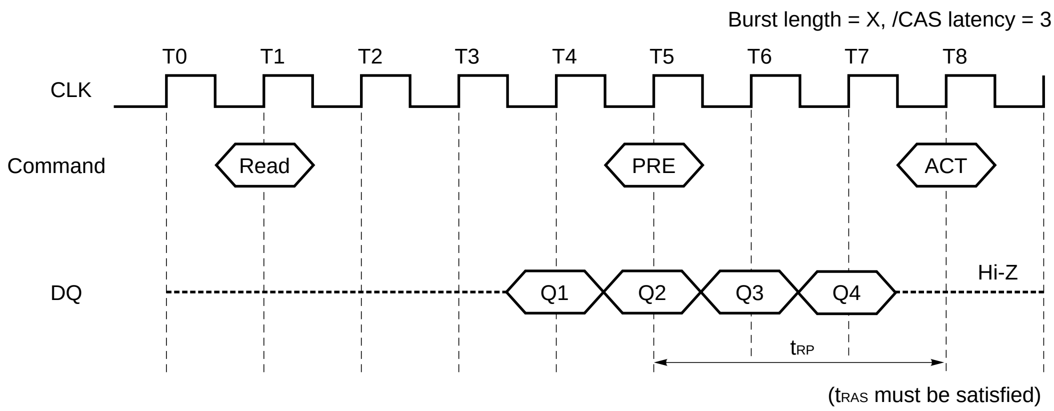
12.2.1 Precharge Termination in READ Cycle

During a read cycle, the burst read operation is terminated by a precharge command.
When the precharge command is issued, the burst read operation is terminated and precharge starts.
The same bank can be activated again after t_{RP} from the precharge command.
To issue a precharge command, t_{RAS} must be satisfied.

When /CAS latency is 2, the read data will remain valid until one clock after the precharge command.



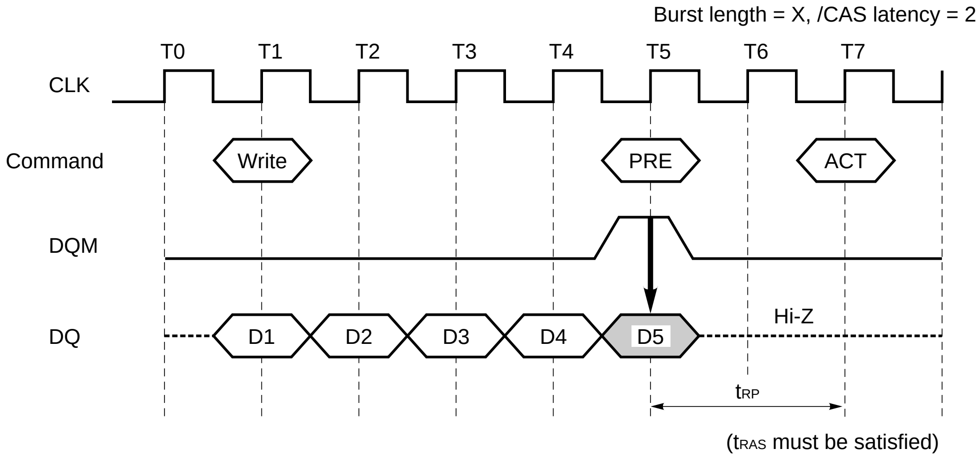
When /CAS latency is 3, the read data will remain valid until two clocks after the precharge command.



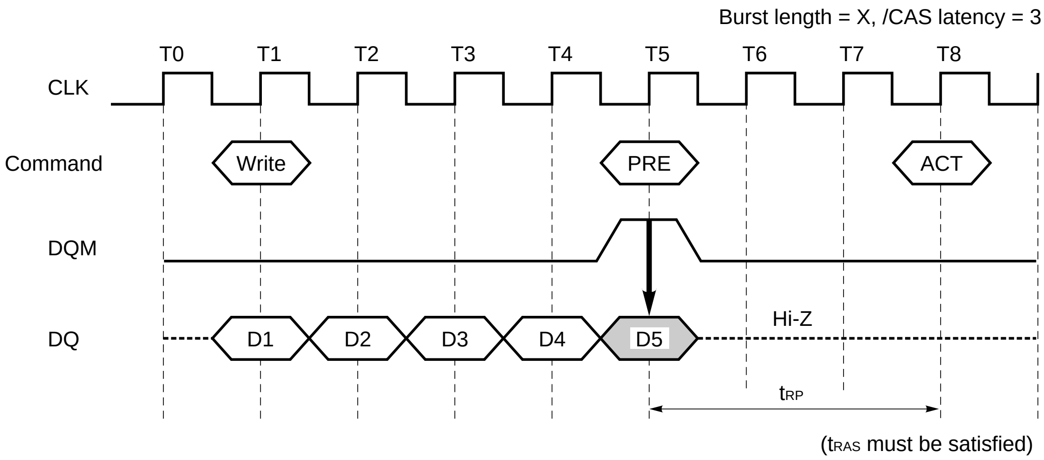
12.2.2 Precharge Termination in WRITE Cycle

During a write cycle, the burst write operation is terminated by a precharge command.
When the precharge command is issued, the burst write operation is terminated and precharge starts.
The same bank can be activated again after t_{RP} from the precharge command.
To issue a precharge command, t_{RAS} must be satisfied.

When /CAS latency is 2, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



When /CAS latency is 3, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



13. Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute **Power on sequence and CBR (auto) Refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}, $V_{CC}Q$		–0.5 to +4.6	V
Voltage on input pin relative to GND	V_T		–0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–55 to + 125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}, $V_{CC}Q$		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3 Note1	V
Low level input voltage	V_{IL}		–0.3 Note 2		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Notes 1. $V_{IH(MAX.)} = V_{CC} + 1.5$ V (Pulse width $\leq$ 5ns)

2. $V_{IL(MIN.)} = -1.5$ V (Pulse width $\leq$ 5ns)

Pin Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, BA0, BA1	2.5		4	pF
	C_{I2}	CLK, CKE, /CS, /RAS, /CAS, /WE, DQM0 - DQM3	2.5		4	
Data input / output capacitance	$C_{I/O}$	DQ0 - DQ31	4		6.5	pF

DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test conditions	/CAS latency	Grade	Maximum	Unit	Notes
Operating current	I_{CC1}	Burst length = 1, $t_{RC} \geq t_{RC(MIN.)}$, I_O = 0 mA, One bank active	CL=2	-A60	150	mA	1
				-A70	140		
				-A80	130		
				-A10	130		
				-A10B	120		
			CL=3	-A60	160		
				-A70	150		
				-A80	140		
				-A10	140		
				-A10B	130		
Precharge standby current in power down mode	$I_{CC2}P$	CKE $\leq V_{IL(MAX.)}$, t_{CK} = 15 ns			1	mA	
	$I_{CC2}PS$	CKE $\leq V_{IL(MAX.)}$, $t_{CK} = \infty$			1		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE $\geq V_{IH(MIN.)}$, t_{CK} = 15 ns, CS $\geq V_{IH(MIN.)}$, Input signals are changed one time during 30 ns			20	mA	
	$I_{CC2}NS$	CKE $\geq V_{IH(MIN.)}$, $t_{CK} = \infty$, Input signals are stable.			6		
Active standby current in power down mode	$I_{CC3}P$	CKE $\leq V_{IL(MAX.)}$, t_{CK} = 15 ns			5	mA	
	$I_{CC3}PS$	CKE $\leq V_{IL(MAX.)}$, $t_{CK} = \infty$			4		
Active standby current in non power down mode	$I_{CC3}N$	CKE $\geq V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS $\geq V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.			30	mA	
	$I_{CC3}NS$	CKE $\geq V_{IH(MIN.)}$, $t_{CK} = \infty$, Input signals are stable.			20		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA, All banks active	CL=2	-A60	170	mA	2
				-A70	170		
				-A80	170		
				-A10	140		
				-A10B	130		
			CL=3	-A60	240		
				-A70	220		
				-A80	190		
				-A10	180		
				-A10B	160		
CBR (auto) refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$	CL=2	-A60	160	mA	3
				-A70	150		
				-A80	150		
				-A10	150		
				-A10B	130		
			CL=3	-A60	170		
				-A70	160		
				-A80	160		
				-A10	160		
				-A10B	140		
★ Self refresh current	I_{CC6}	CKE $\leq$ 0.2 V			1	mA	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

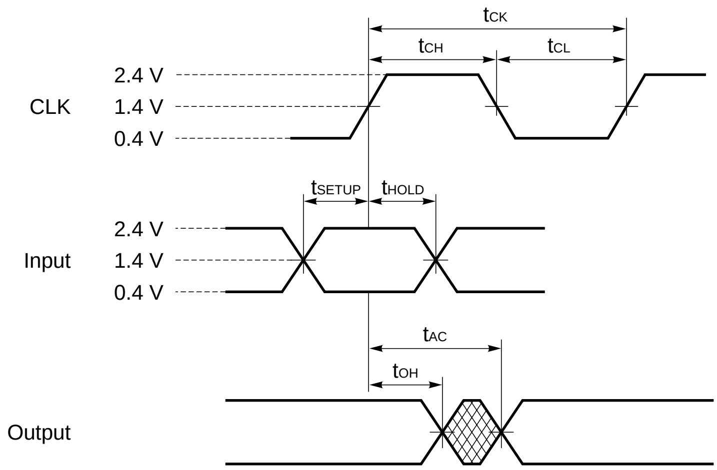
DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit	Notes
Input leakage current	$I_{I(L)}$	$0 \le V_I \le V_{CC}Q$, $V_{CC}Q = V_{CC}$, All other pins not under test = 0 V	–1.0		+1.0	μA	
Output leakage current	$I_{O(L)}$	$0 \le V_O \le V_{CC}Q$, D_{OUT} is disabled	–1.5		+1.5	μA	
High level output voltage	V_{OH}	I_O = – 4 mA	2.4			V	
Low level output voltage	V_{OL}	I_O = + 4 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

★ **Test Conditions**

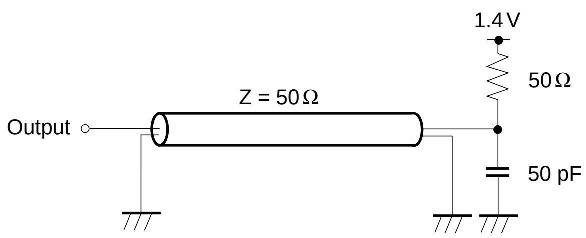
Parameter	Value	Unit	Notes
AC high level input voltage / low level input voltage	2.4 / 0.4	V	
Input timing measurement reference level	1.4	V	
Transition time (Input rise and fall time)	1	ns	
Output timing measurement reference level	1.4	V	



Synchronous Characteristics

Parameter	/CAS latency	Symbol	-A60		-A70		-A80		-A10		-A10B		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	CL = 3	t_{CK3}	6	(166MHz)	7	(143MHz)	8	(125MHz)	10	(100MHz)	10	(100MHz)	ns	
	CL = 2	t_{CK2}	10	(100MHz)	10	(100MHz)	10	(100MHz)	13	(77MHz)	15	(67MHz)	ns	
Access time from CLK	CL = 3	t_{AC3}		5.5		5.5		6		6		7	ns	1
	CL = 2	t_{AC2}		6		6		6		7		8	ns	1
CLK high level width		t_{CH}	2		2		3		3		3.5		ns	
CLK low level width		t_{CL}	2		2		3		3		3.5		ns	
Data-out hold time		t_{OH}	2.5		2.5		3		3		3		ns	1
Data-out low-impedance time		t_{LZ}	0		0		0		0		0		ns	
Data-out high-impedance time	CL = 3	t_{HZ3}	2.5	5.5	2.5	5.5	3	6	3	6	3	7	ns	
	CL = 2	t_{HZ2}	2.5	6	2.5	6	3	6	3	7	3	8	ns	
Data-in setup time		t_{DS}	1.5		1.5		2		2		2.5		ns	
Data-in hold time		t_{DH}	0.8		0.8		1		1		1		ns	
Address setup time		t_{AS}	1.5		1.5		2		2		2.5		ns	
Address hold time		t_{AH}	0.8		0.8		1		1		1		ns	
CKE setup time		t_{CKS}	2		2		2		2		2.5		ns	
CKE hold time		t_{CKH}	1		1		1		1		1		ns	
CKE setup time (Power down exit)		t_{CKSP}	2		2		2		2		2.5		ns	
Command (/CS, /RAS, /CAS, /WE, DQM) setup time		t_{CMS}	1.5		1.5		2		2		2.5		ns	
Command (/CS, /RAS, /CAS, /WE, DQM) hold time		t_{CMH}	0.8		0.8		1		1		1		ns	

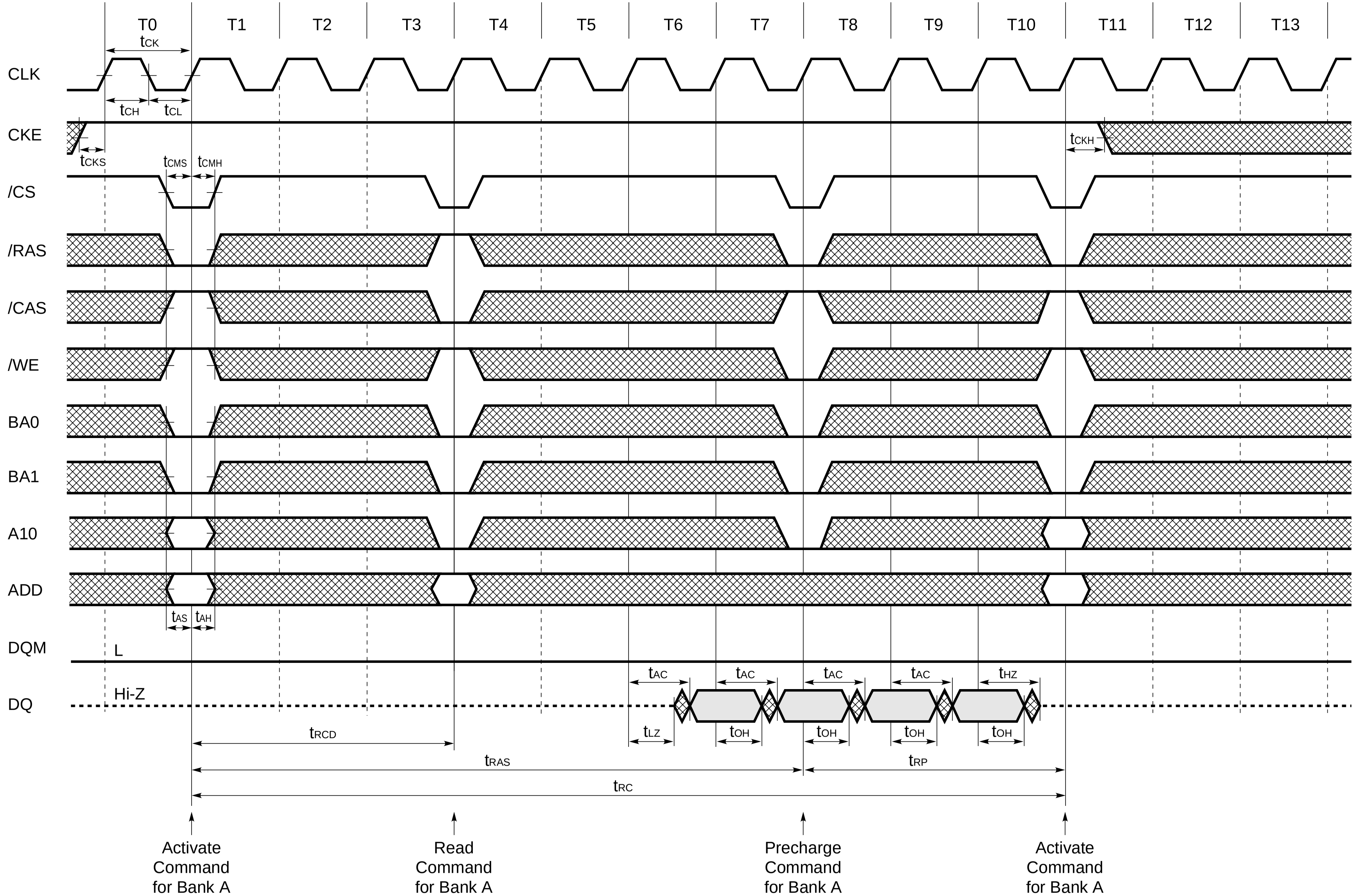
Note 1. Output load



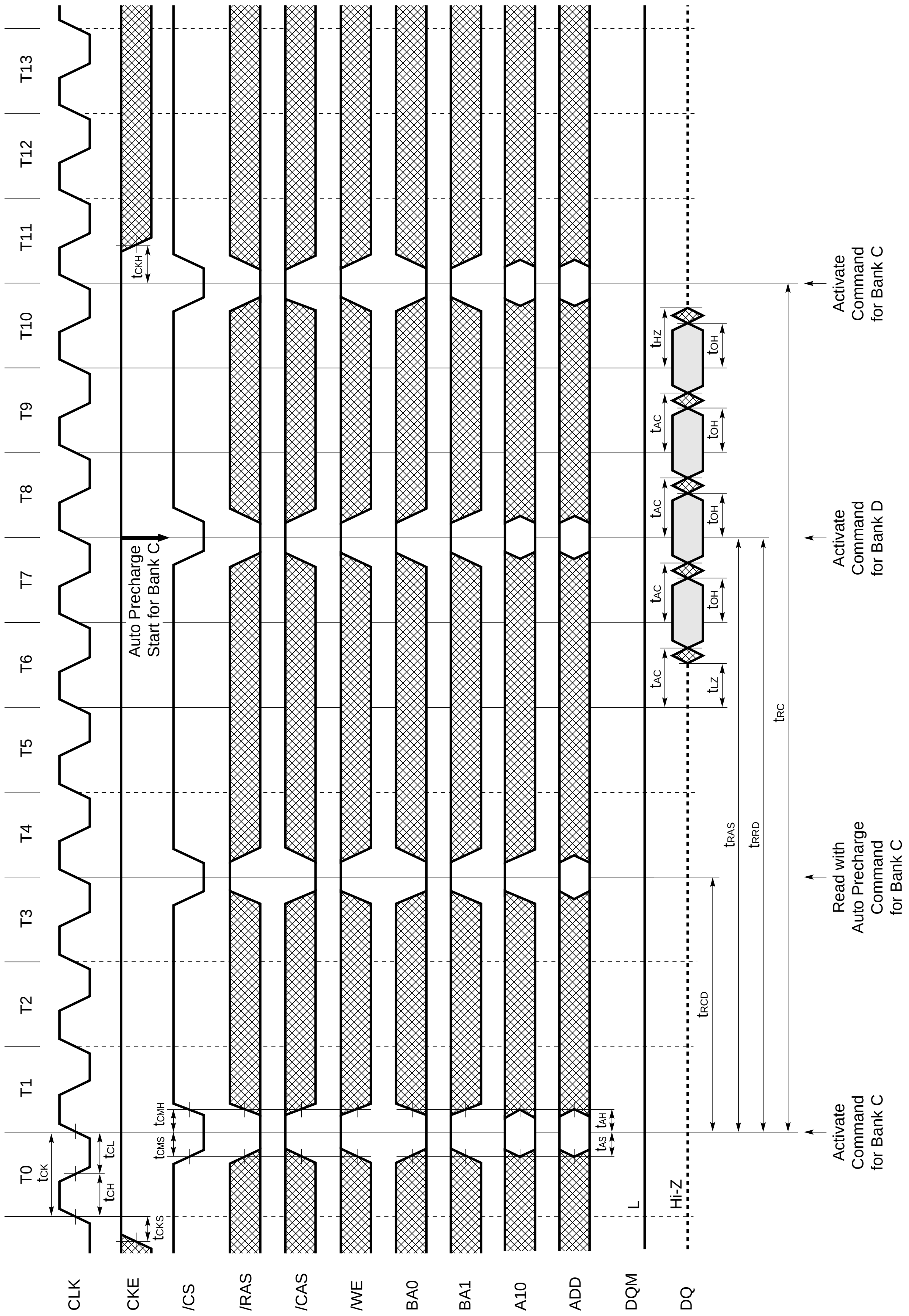
Asynchronous Characteristics

Parameter	/CAS latency	Symbol	-A60		-A70		-A80		-A10		-A10B		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT command period (Operation)		t_{RC}	60		63		70		70		90		ns	
REF to REF/ACT command period (Refresh)		t_{RC1}	66		70		70		70		90		ns	
ACT to PRE command period		t_{RAS}	42	120,000	42	120,000	48	120,000	50	120,000	60	120,000	ns	
PRE to ACT command period		t_{RP}	18		20		20		20		30		ns	
Delay time ACT to READ/WRITE command		t_{RCD}	18		20		20		20		30		ns	
ACT(one) to ACT(another) command period		t_{RRD}	12		14		16		20		20		ns	
Data-in to PRE command period		t_{DPL}	8		8		8		10		10		ns	
Data-in to ACT(REF) command period (Auto precharge)	CL = 3	t_{DAL3}	2CLK+18		2CLK+20		1CLK+20		1CLK+20		1CLK+30		ns	
	CL = 2	t_{DAL2}	1CLK+18		1CLK+20		1CLK+20		1CLK+20		1CLK+30		ns	
Mode register set cycle time		t_{RSC}	2		2		2		2		2		CLK	
Transition time		t_T	0.5	30	0.5	30	0.5	30	1	30	1	30	ns	
Refresh time (4,096 refresh cycles)		t_{REF}		64		64		64		64		64	ms	

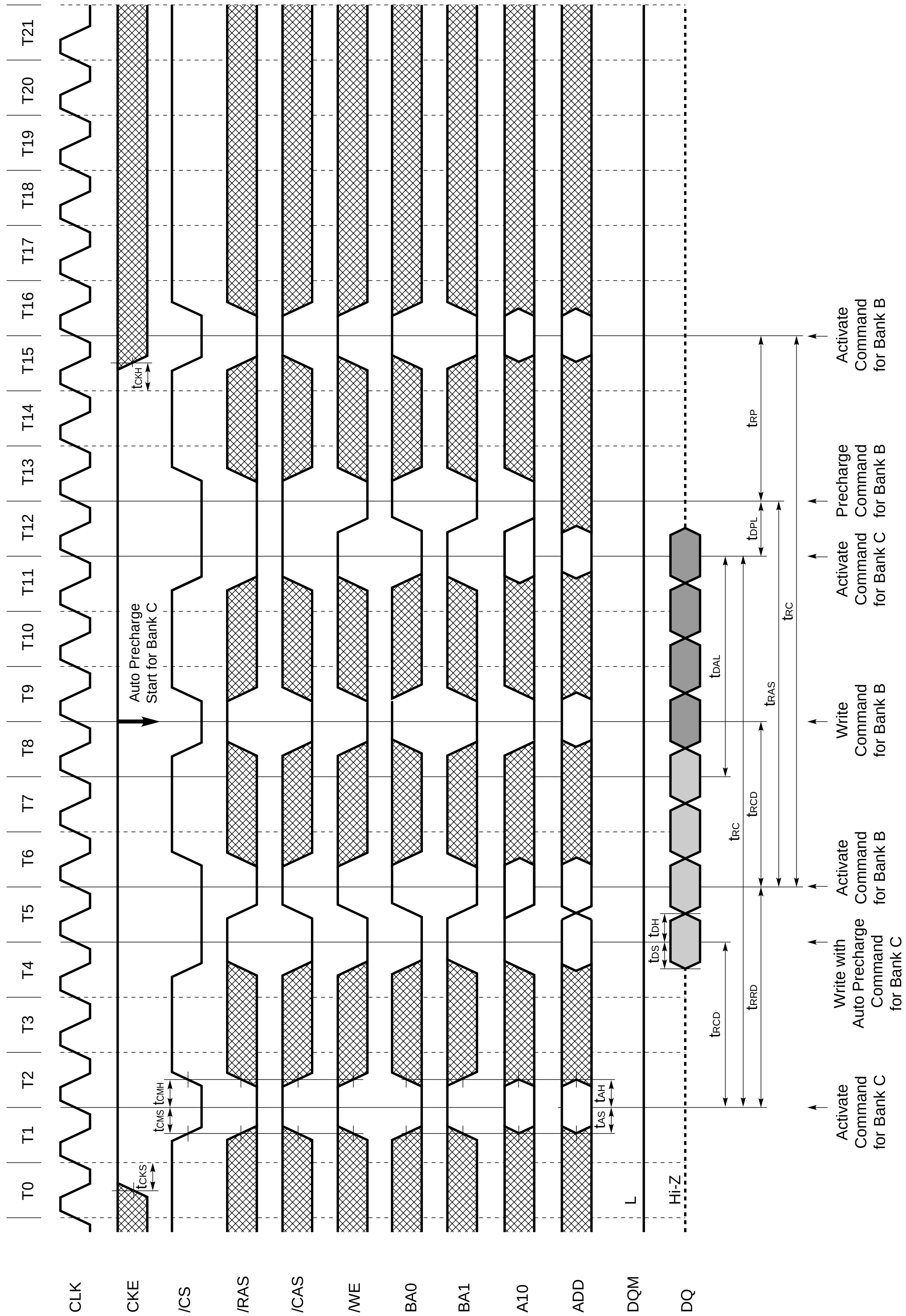
13.1 AC Parameters for Read Timing (Manual Precharge, Burst Length = 4, /CAS Latency = 3)



AC Parameters for Read Timing (Auto Precharge, Burst Length = 4, /CAS Latency = 3)



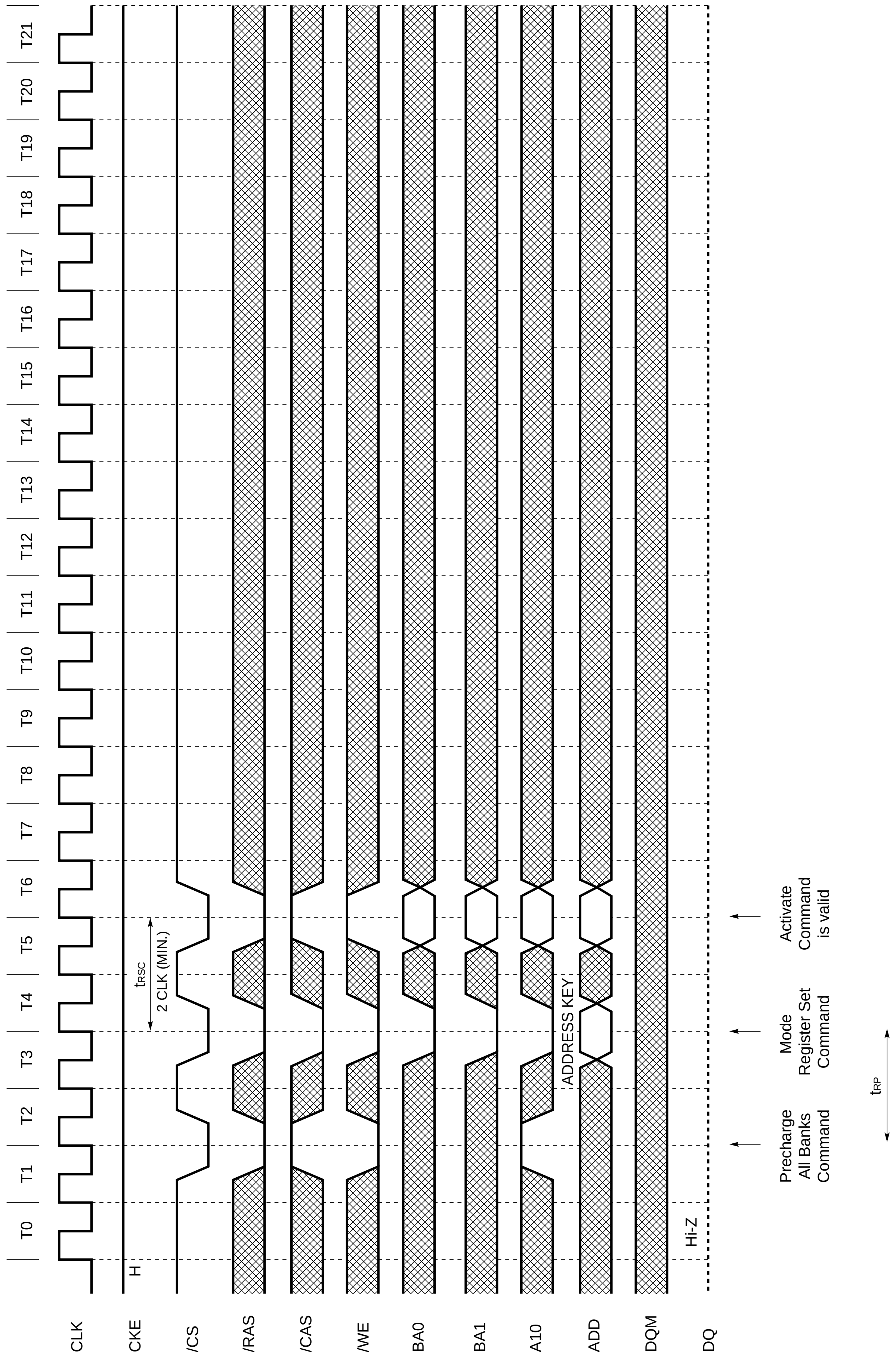
13.2 AC Parameters for Write Timing (Burst Length = 4, /CAS Latency = 3)



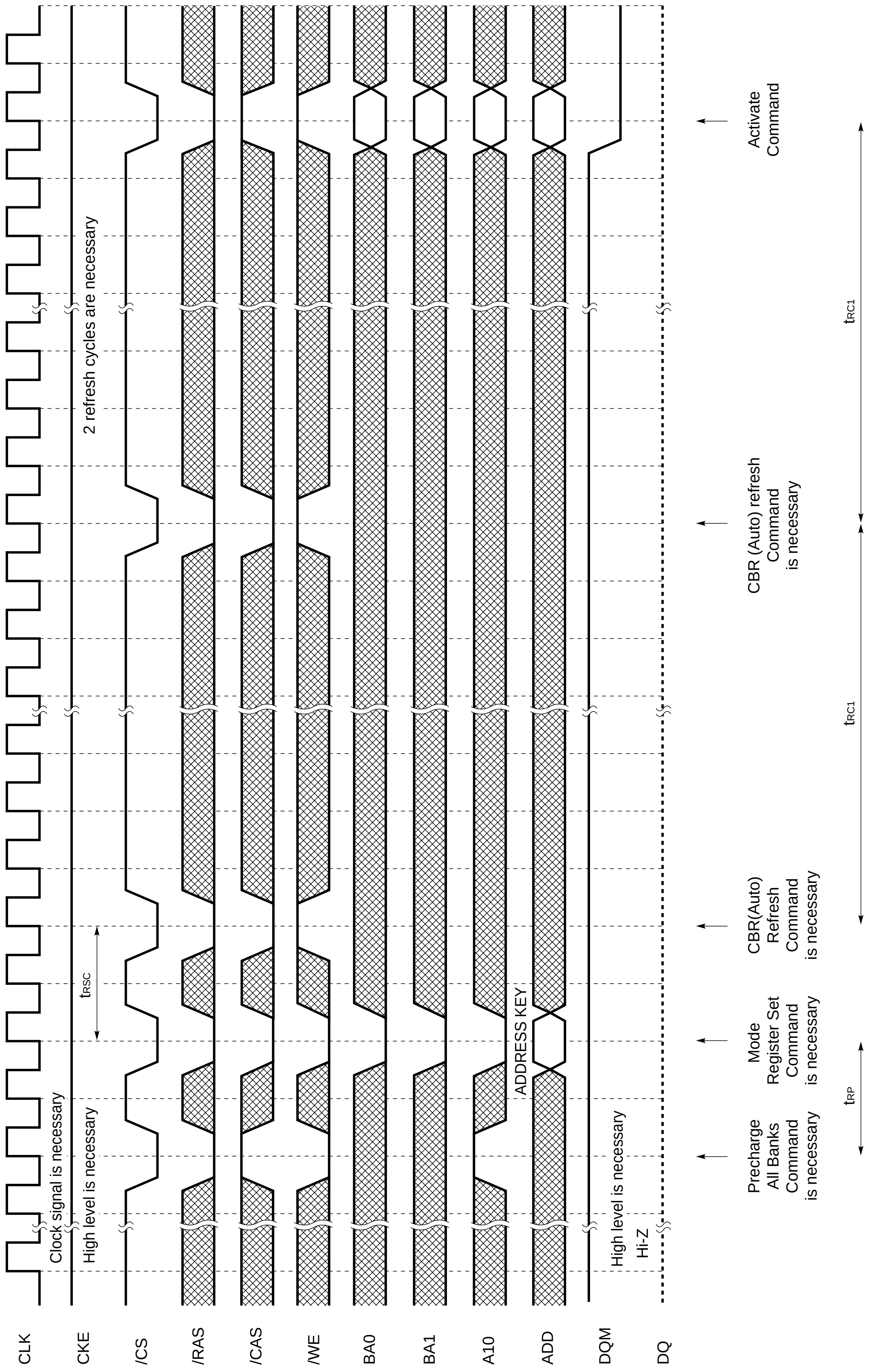
13.3 Relationship between Frequency and Latency

Speed version	-A60		-A70		-A80		-A10		-A10B	
Clock cycle time [ns]	6	10	7	10	8	10	10	13	10	15
Frequency [MHz]	166	100	143	100	125	100	100	77	100	67
/CAS latency	3	2	3	2	3	2	3	2	3	2
[t_{RCD}]	3	2	3	2	3	2	2	2	3	2
/RAS latency (/CAS latency + [t_{RCD}])	6	4	6	4	6	4	5	4	6	4
[t_{RC}]	10	6	9	7	9	7	7	6	9	6
[t_{RC1}]	11	7	10	7	9	7	7	6	9	6
[t_{RAS}]	7	5	6	5	6	5	5	4	6	4
[t_{RRD}]	2	2	2	2	2	2	2	2	2	2
[t_{RP}]	3	2	3	2	3	2	2	2	3	2
[t_{DPL}]	2	1	2	1	1	1	1	1	1	1
[t_{DAL}]	5	3	5	3	4	3	3	3	4	3
[t_{RSC}]	2	2	2	2	2	2	2	2	2	2

13.4 Mode Register Set (Burst Length = 4, /CAS Latency = 2)

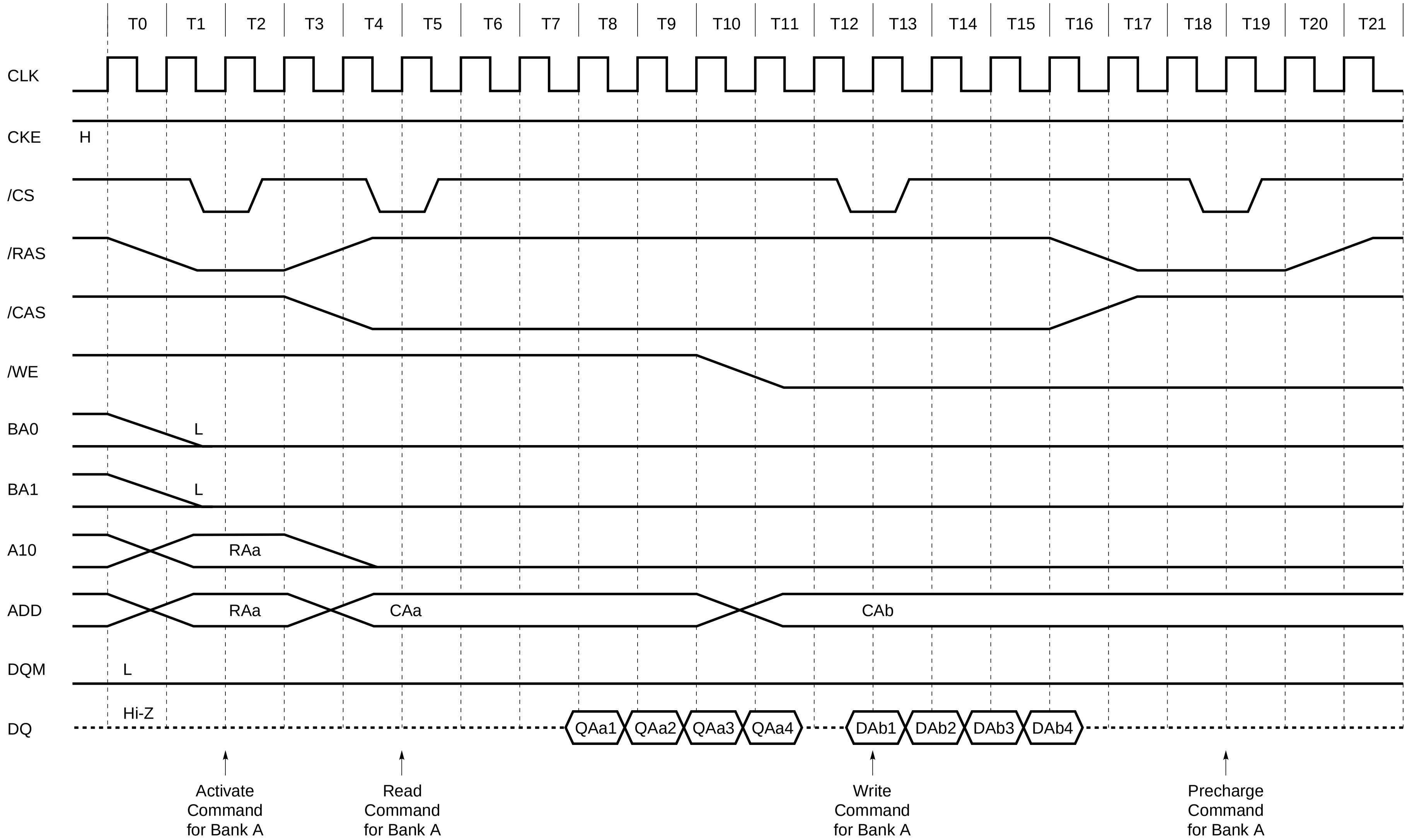


13.5 Power On Sequence and CBR (Auto) Refresh

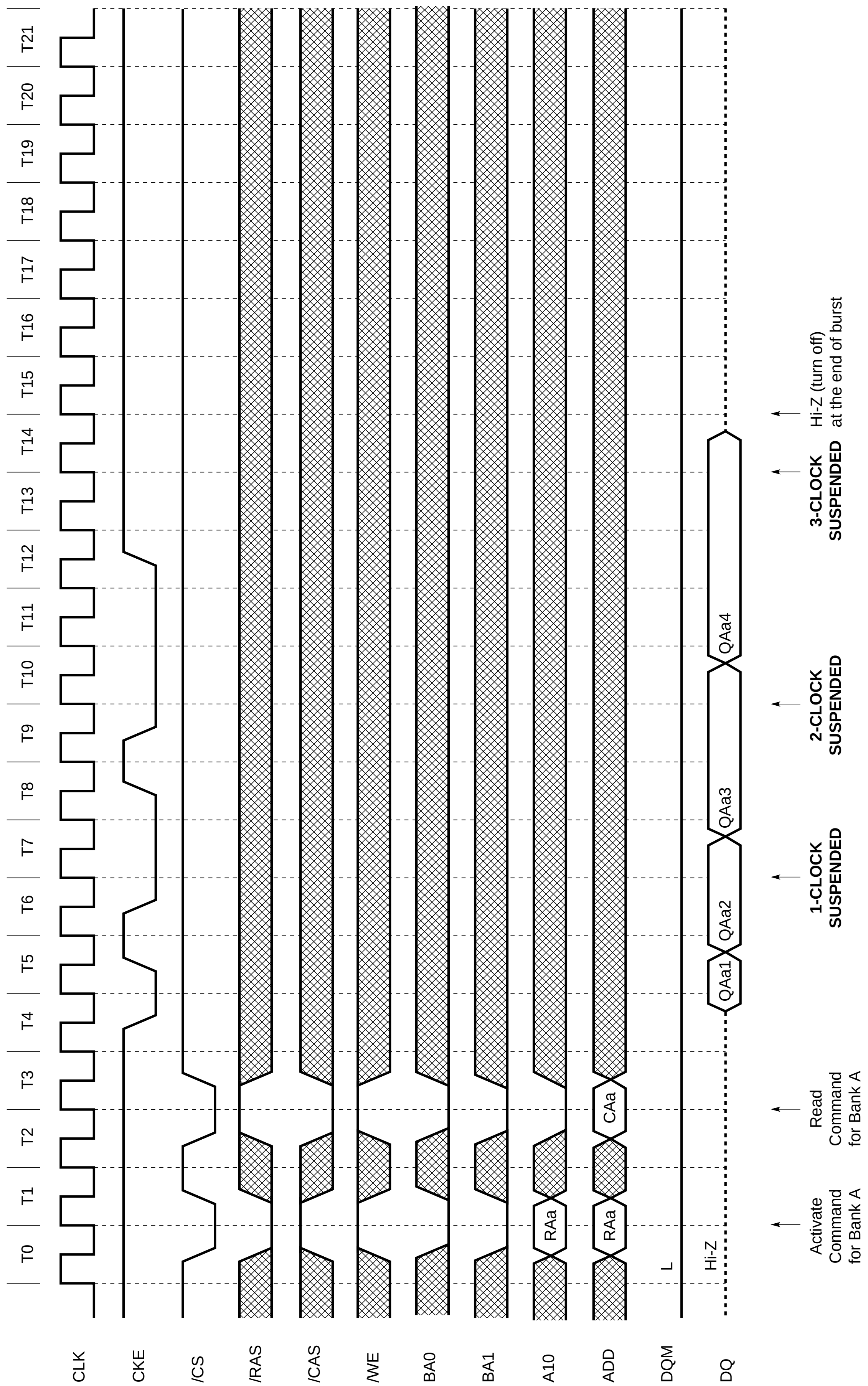


13.6 /CS Function (at 100 MHz, Burst Length = 4, /CAS Latency = 3)

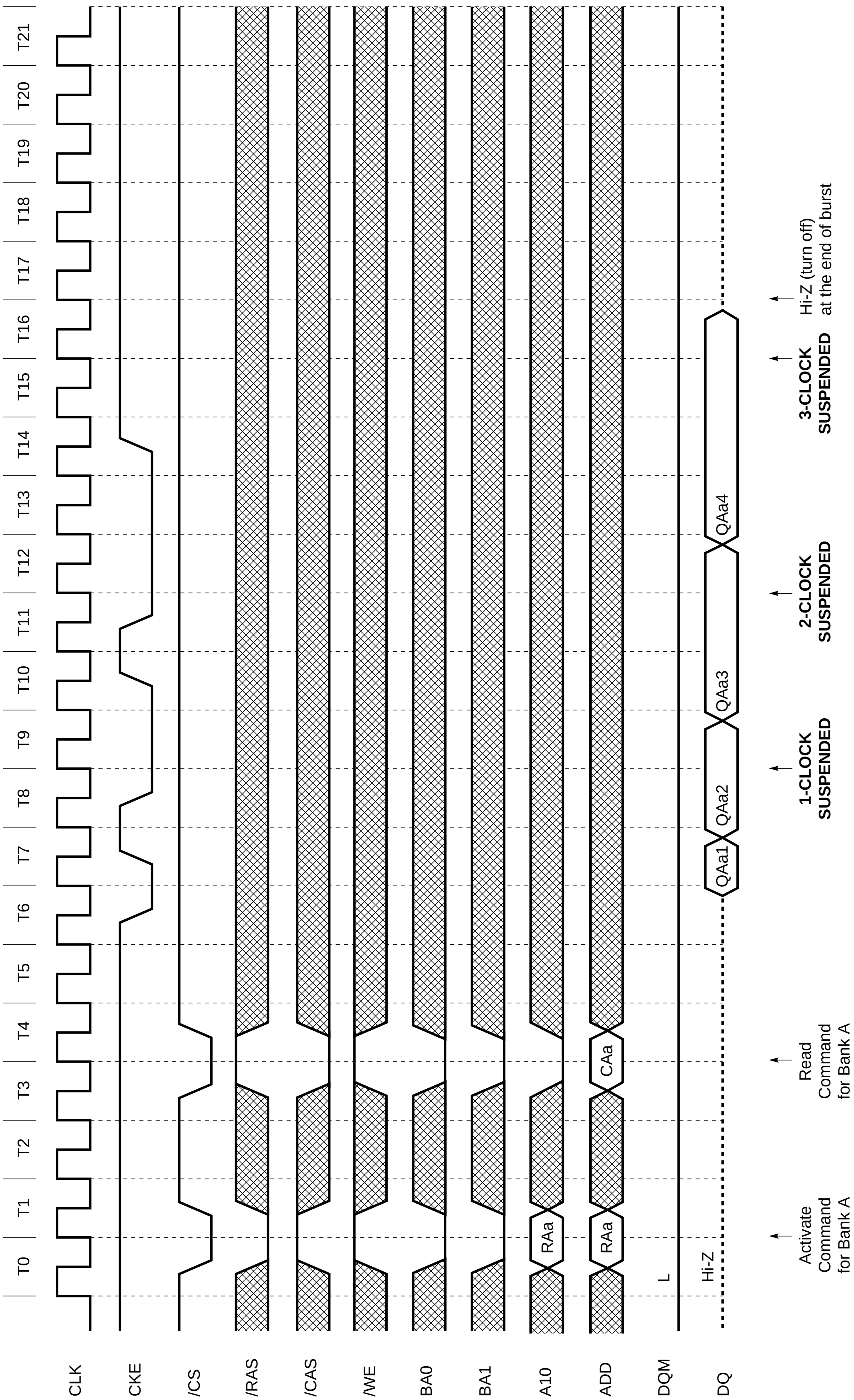
Only /CS signal needs to be issued at minimum rate



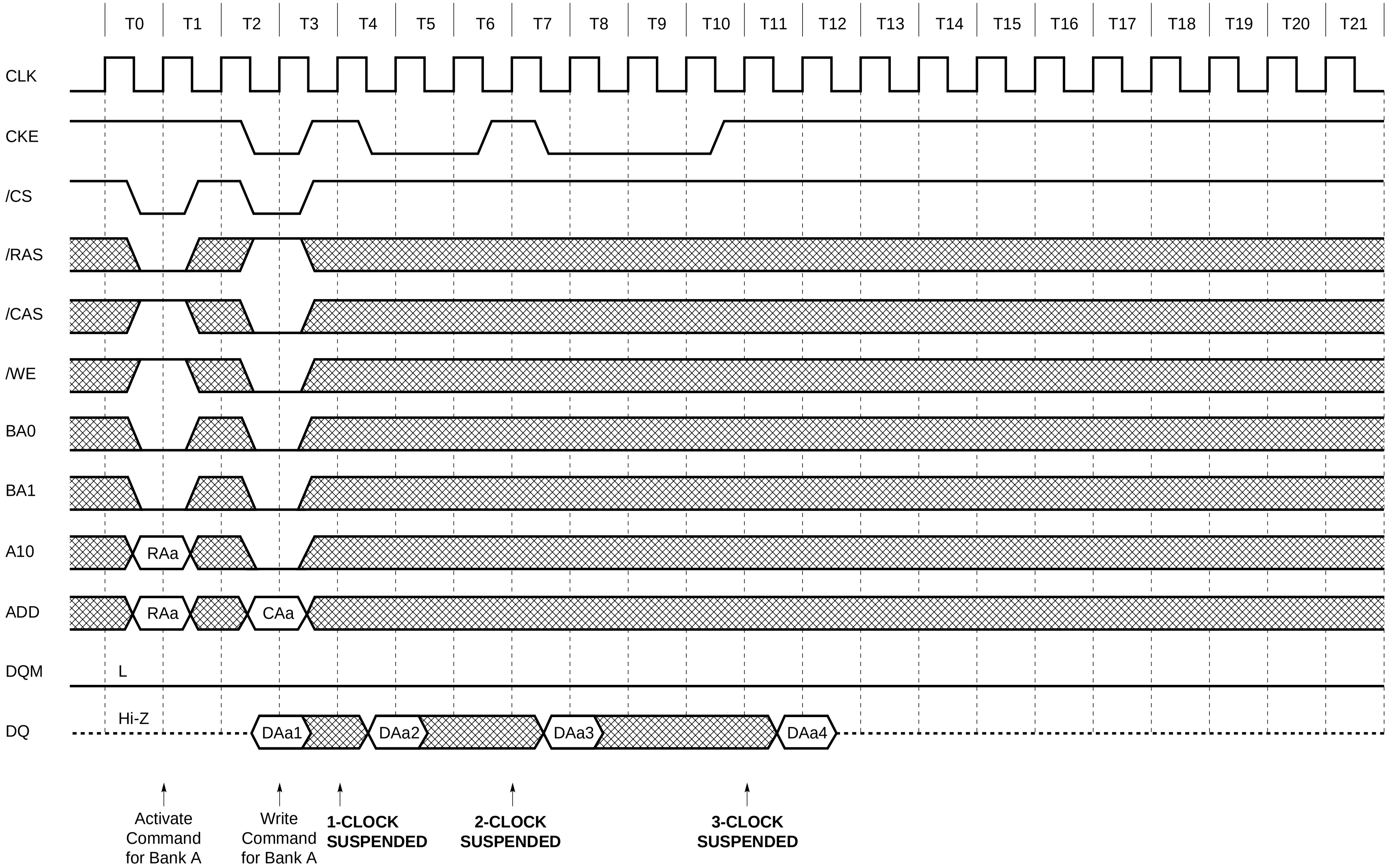
13.7 Clock Suspension during Burst Read (using CKE Function) (1/2) (Burst Length = 4, /CAS Latency = 2)



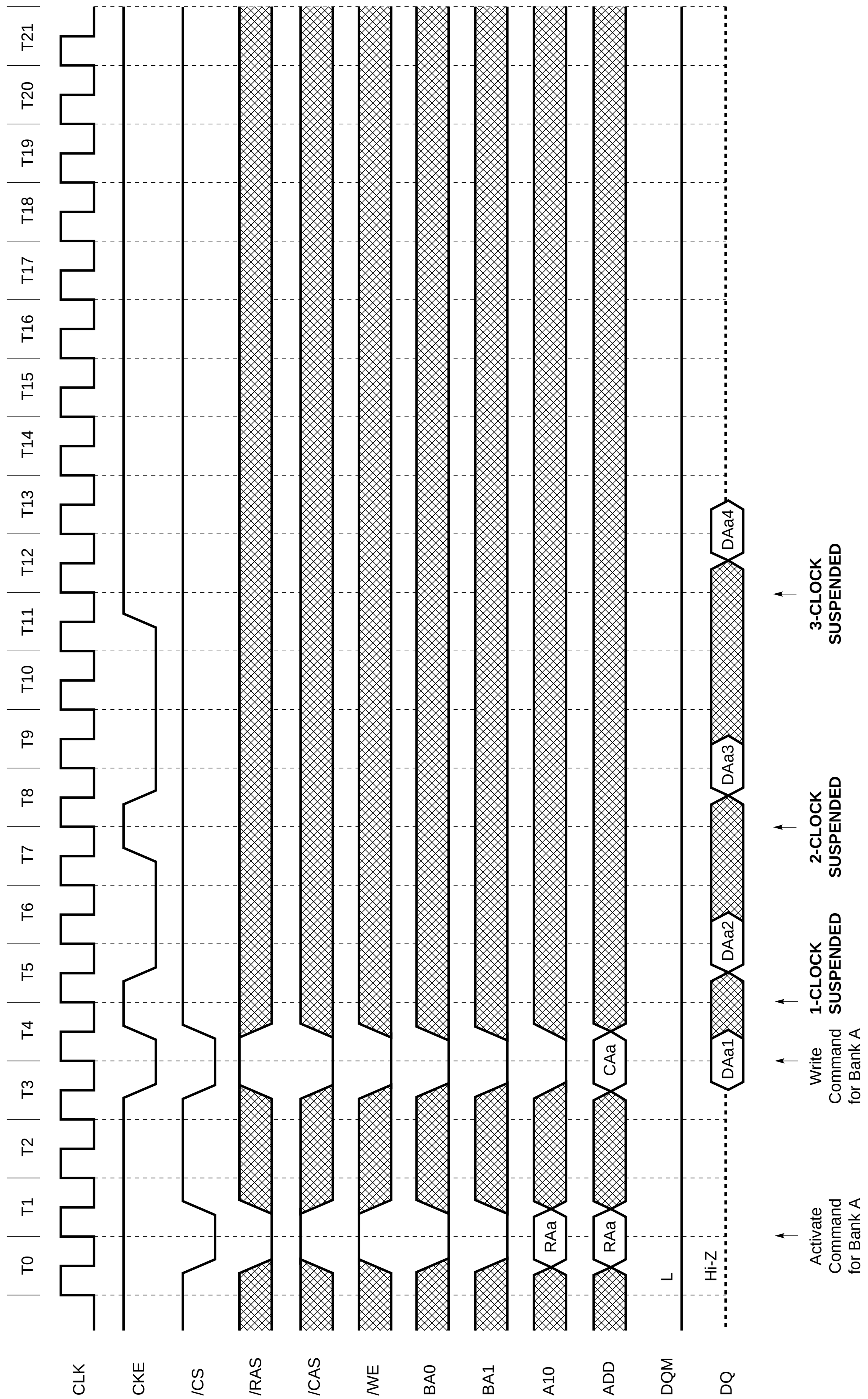
Clock Suspension during Burst Read (using CKE Function) (2/2) (Burst Length = 4, /CAS Latency = 3)



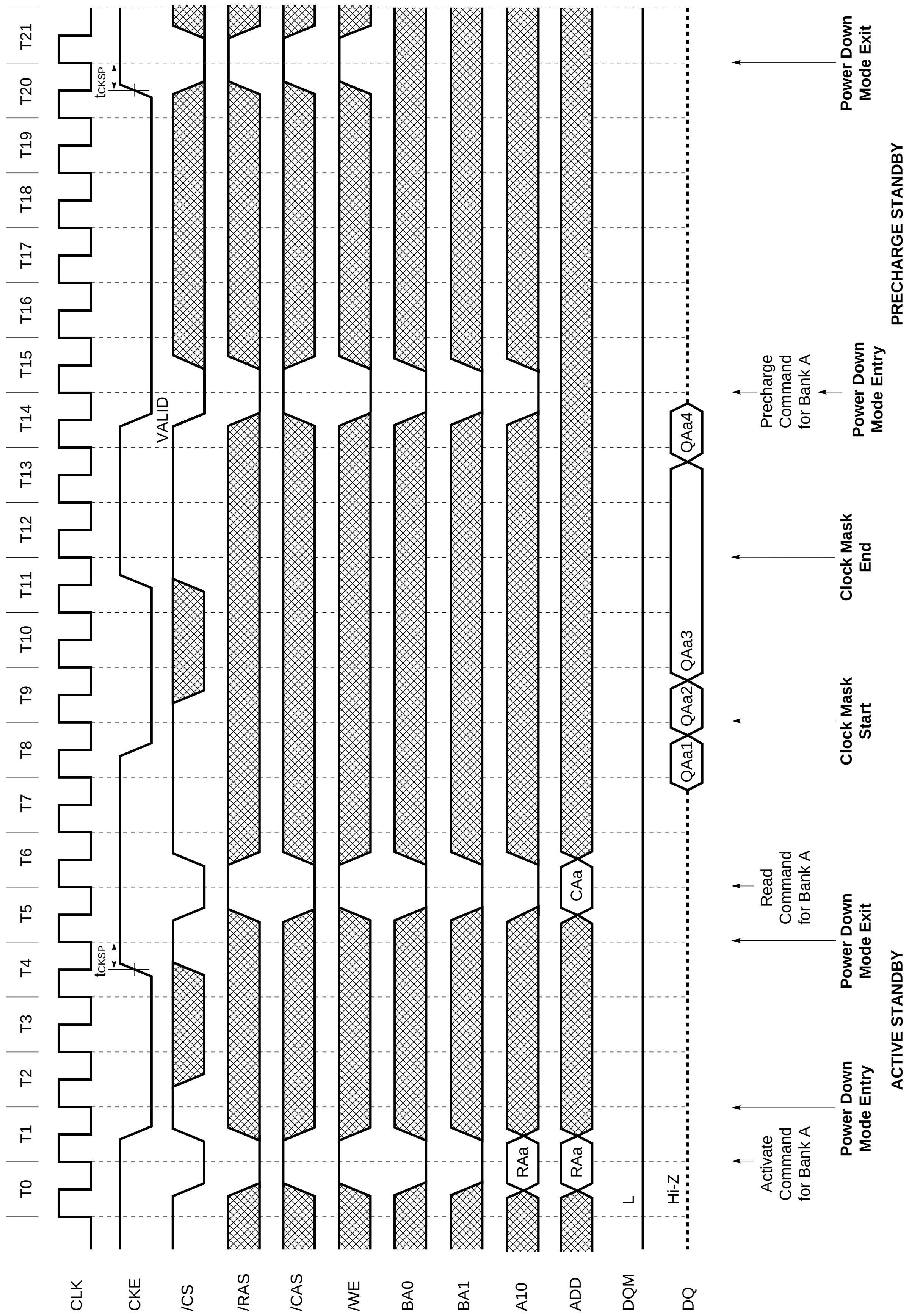
13.8 Clock Suspension during Burst Write (using CKE Function) (1/2) (Burst Length = 4, /CAS Latency = 2)



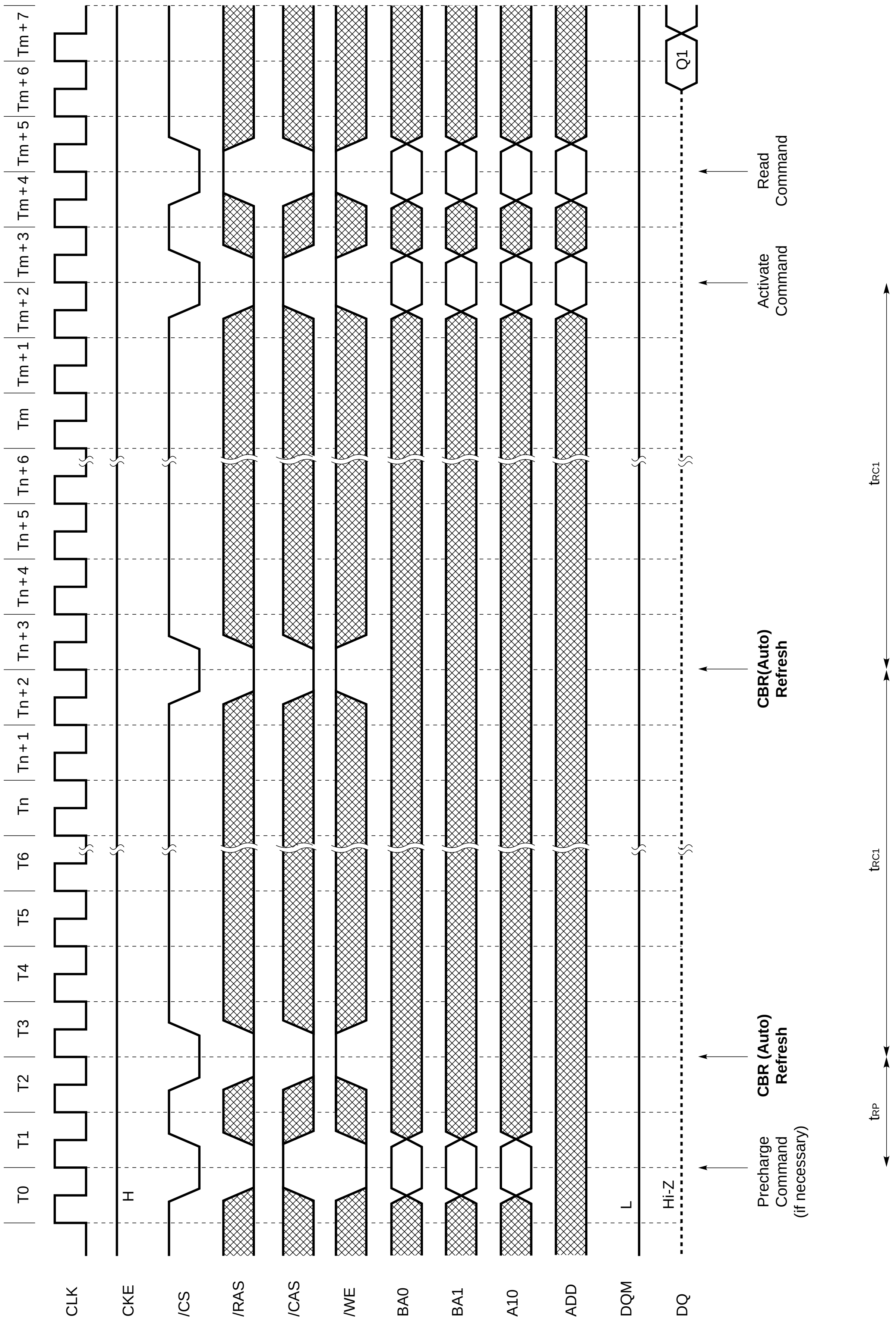
Clock Suspension during Burst Write (using CKE Function) (2/2) (Burst Length = 4, /CAS Latency = 3)



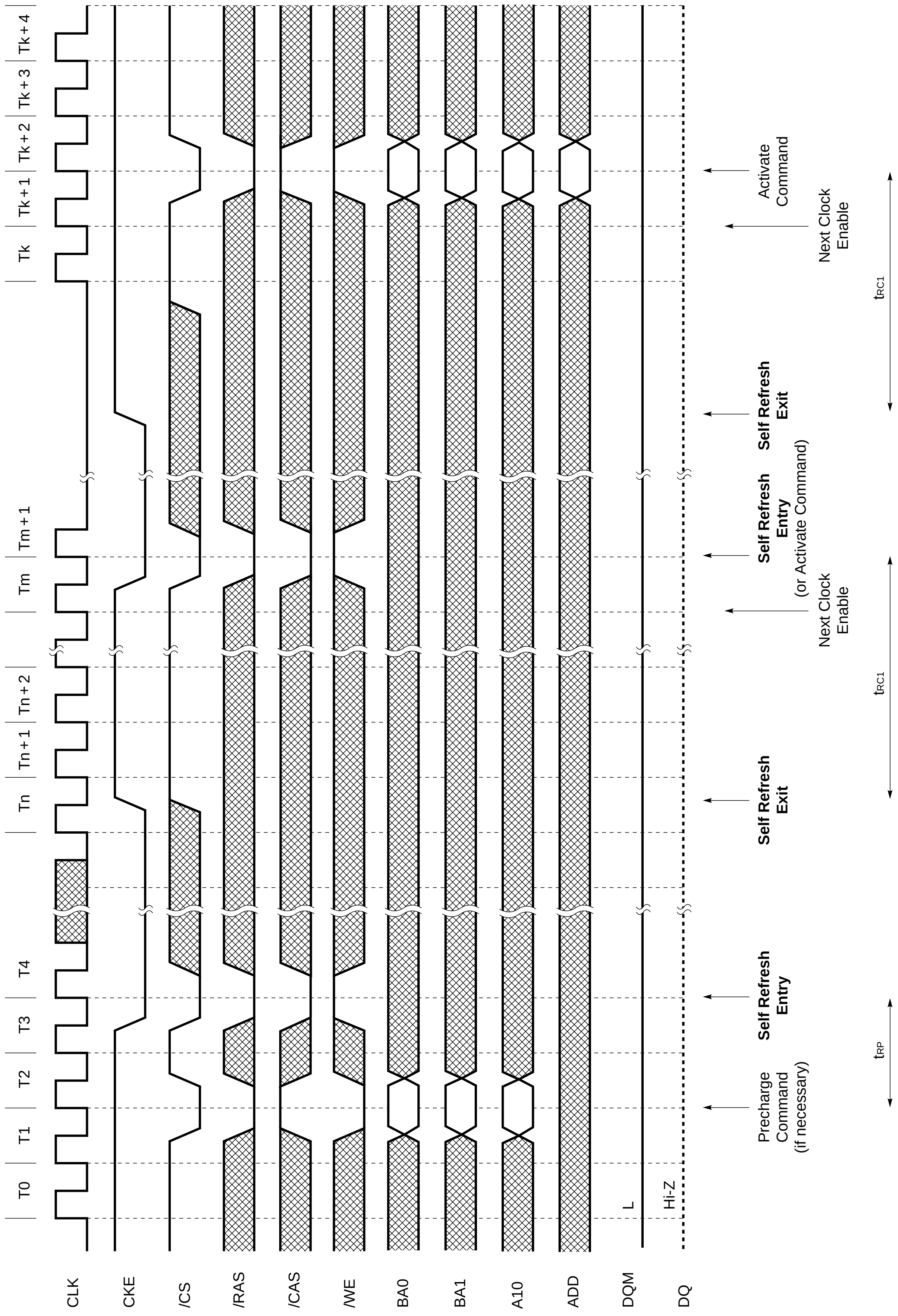
13.9 Power Down Mode and Clock Mask (Burst Length = 4, /CAS Latency = 2)



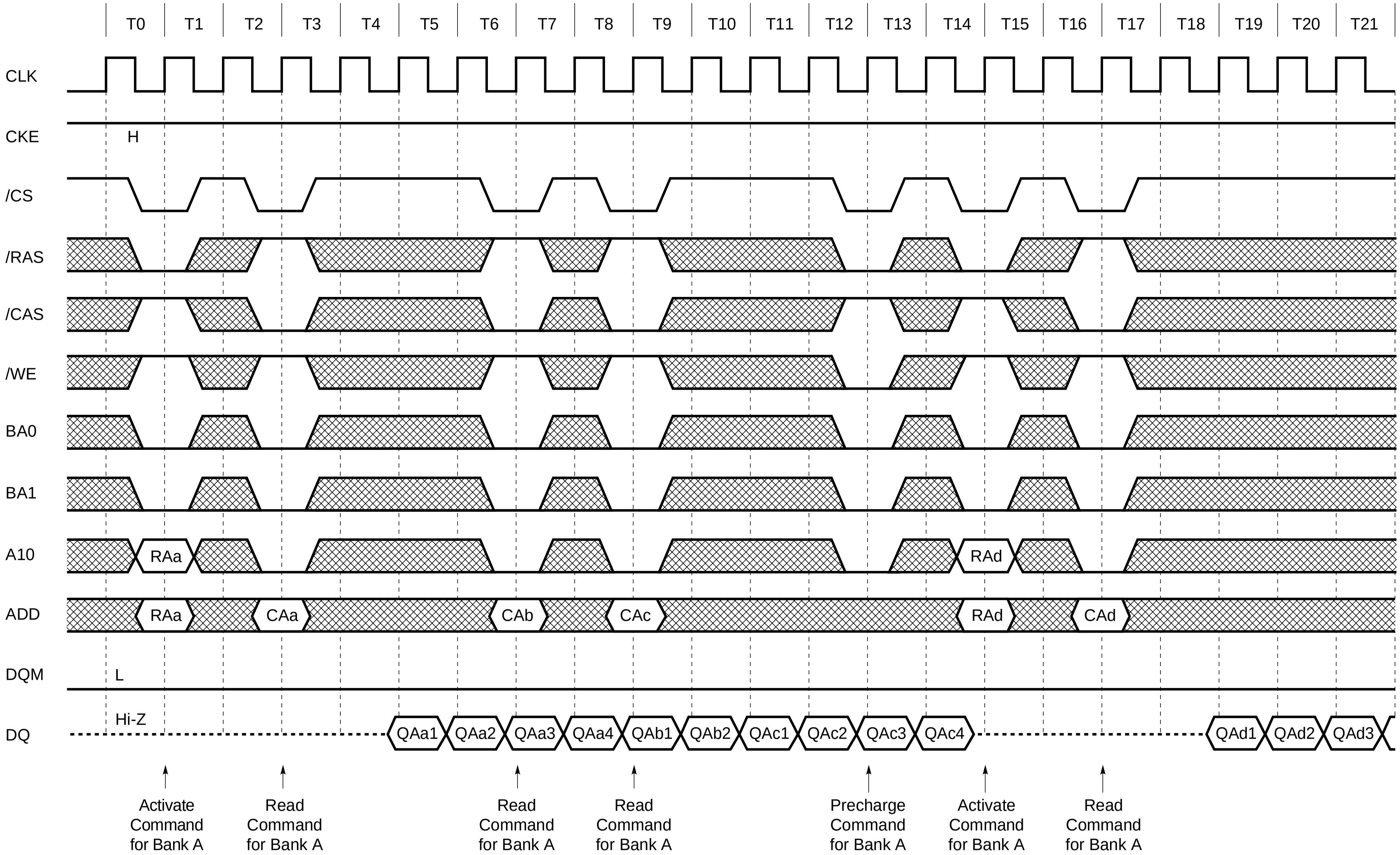
13.10 CBR (Auto) Refresh



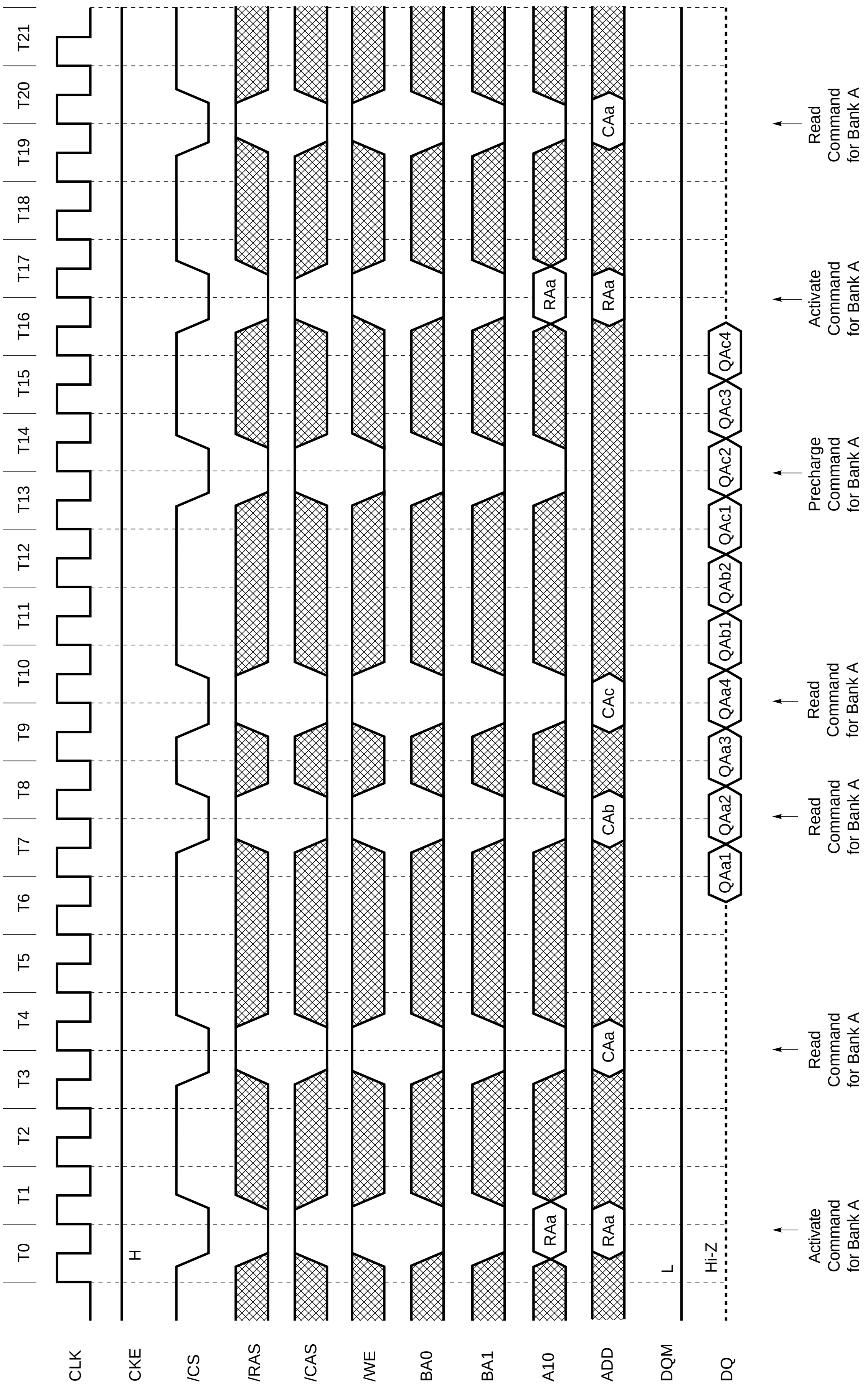
13.11 Self Refresh (Entry and Exit)



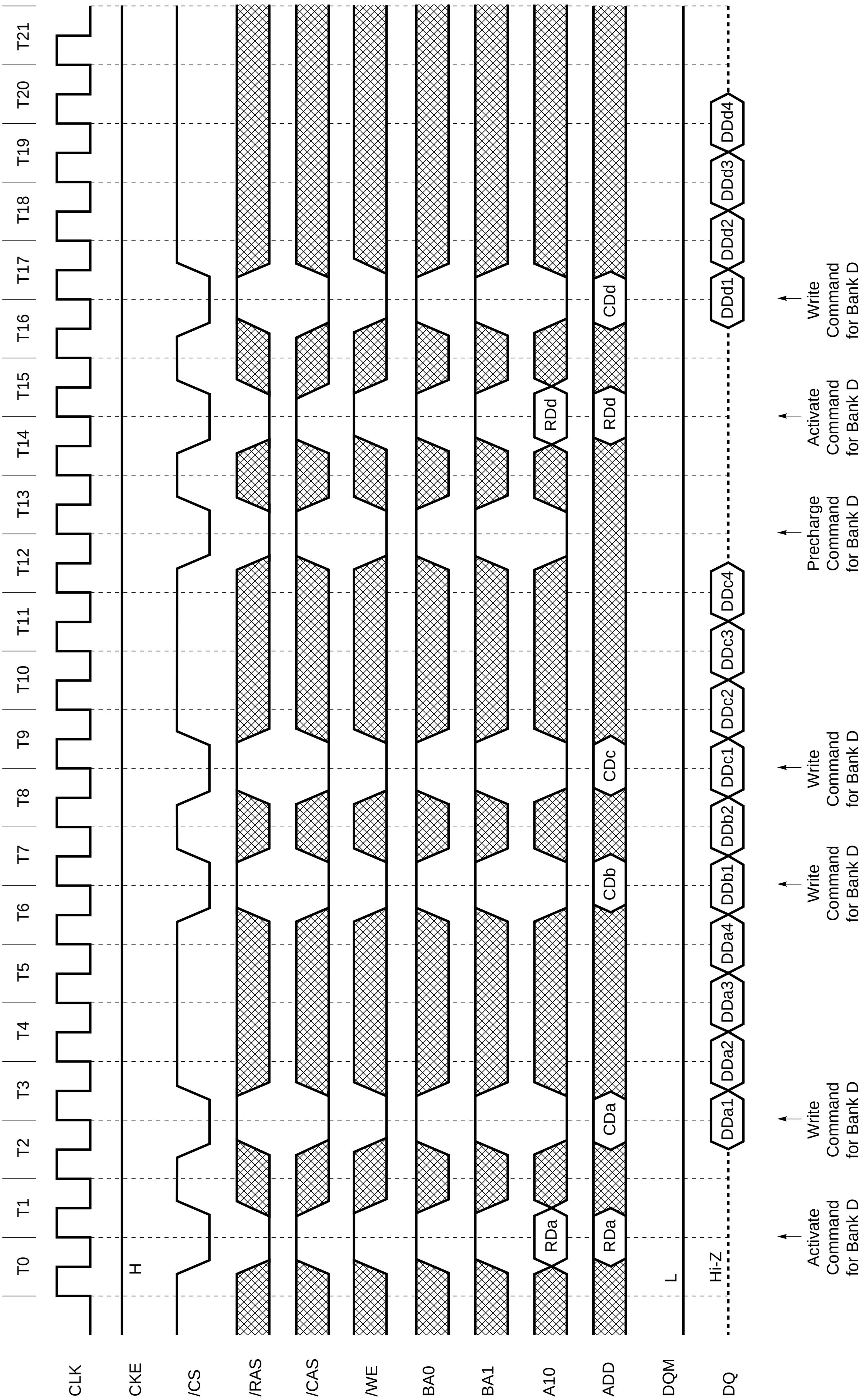
13.12 Random Column Read (Page with Same Bank) (1/2) (Burst Length = 4, /CAS Latency = 2)



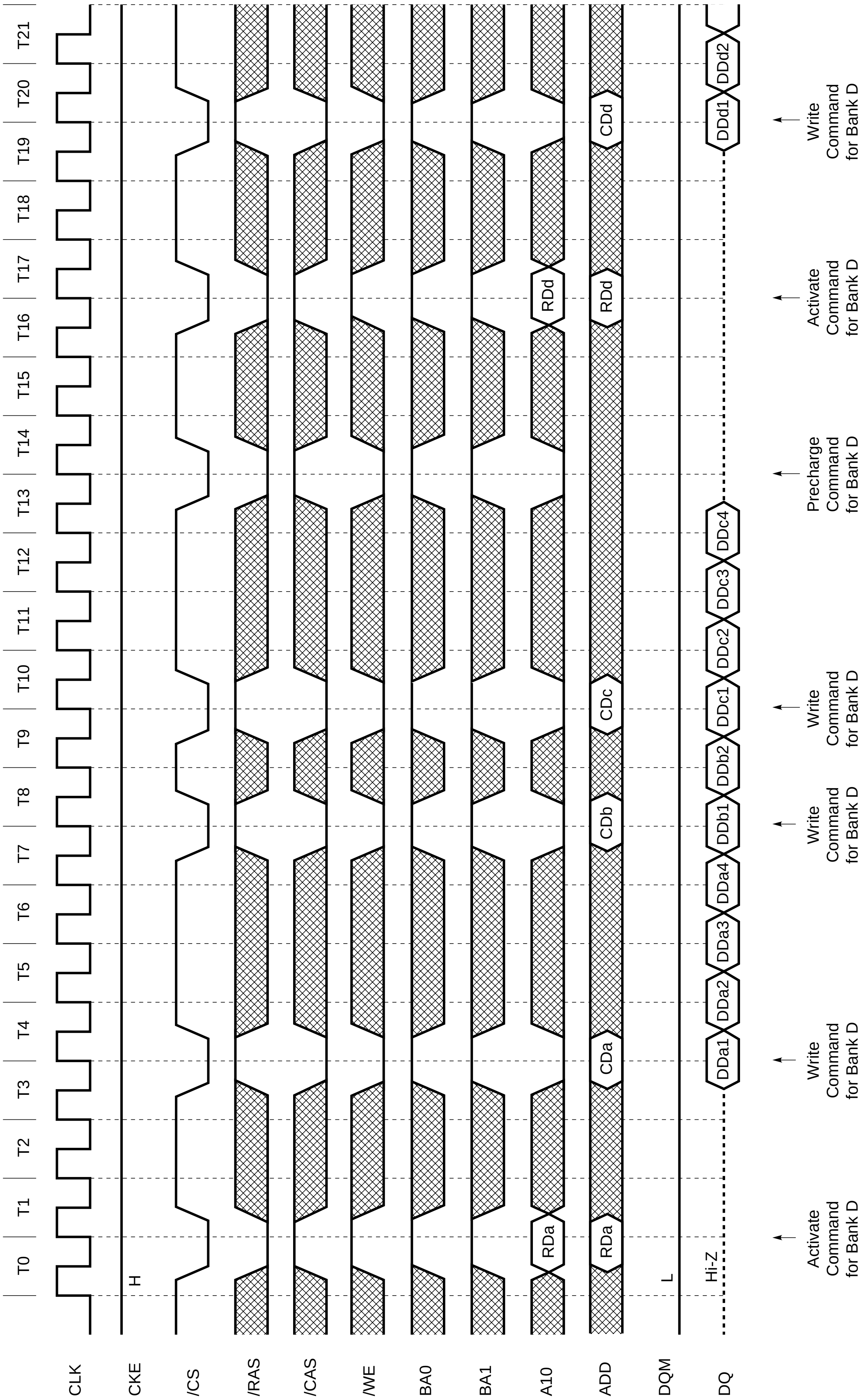
Random Column Read (Page with Same Bank) (2/2) (Burst Length = 4, /CAS Latency = 3)



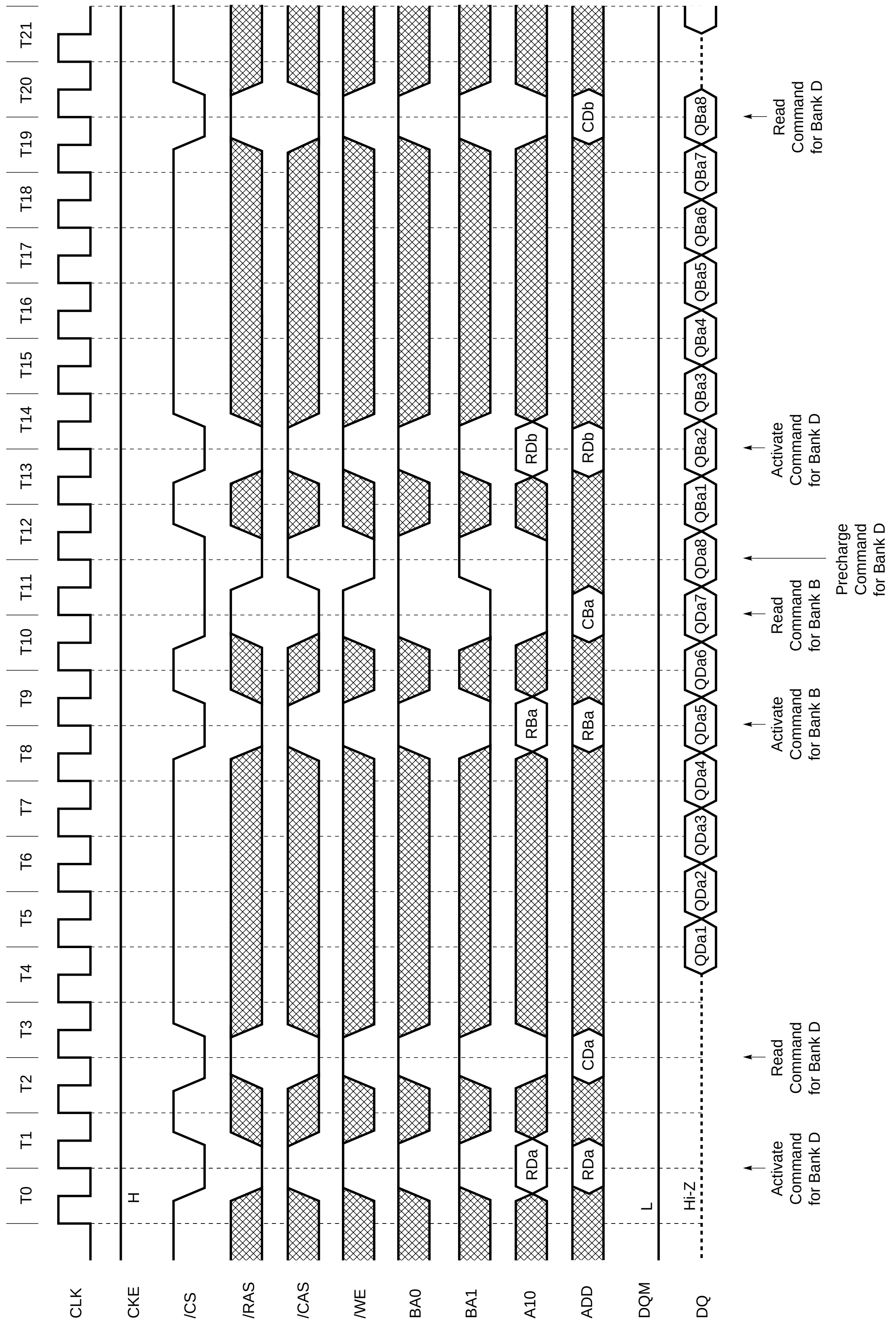
13.13 Random Column Write (Page with Same Bank) (1/2) (Burst Length = 4, /CAS Latency = 2)



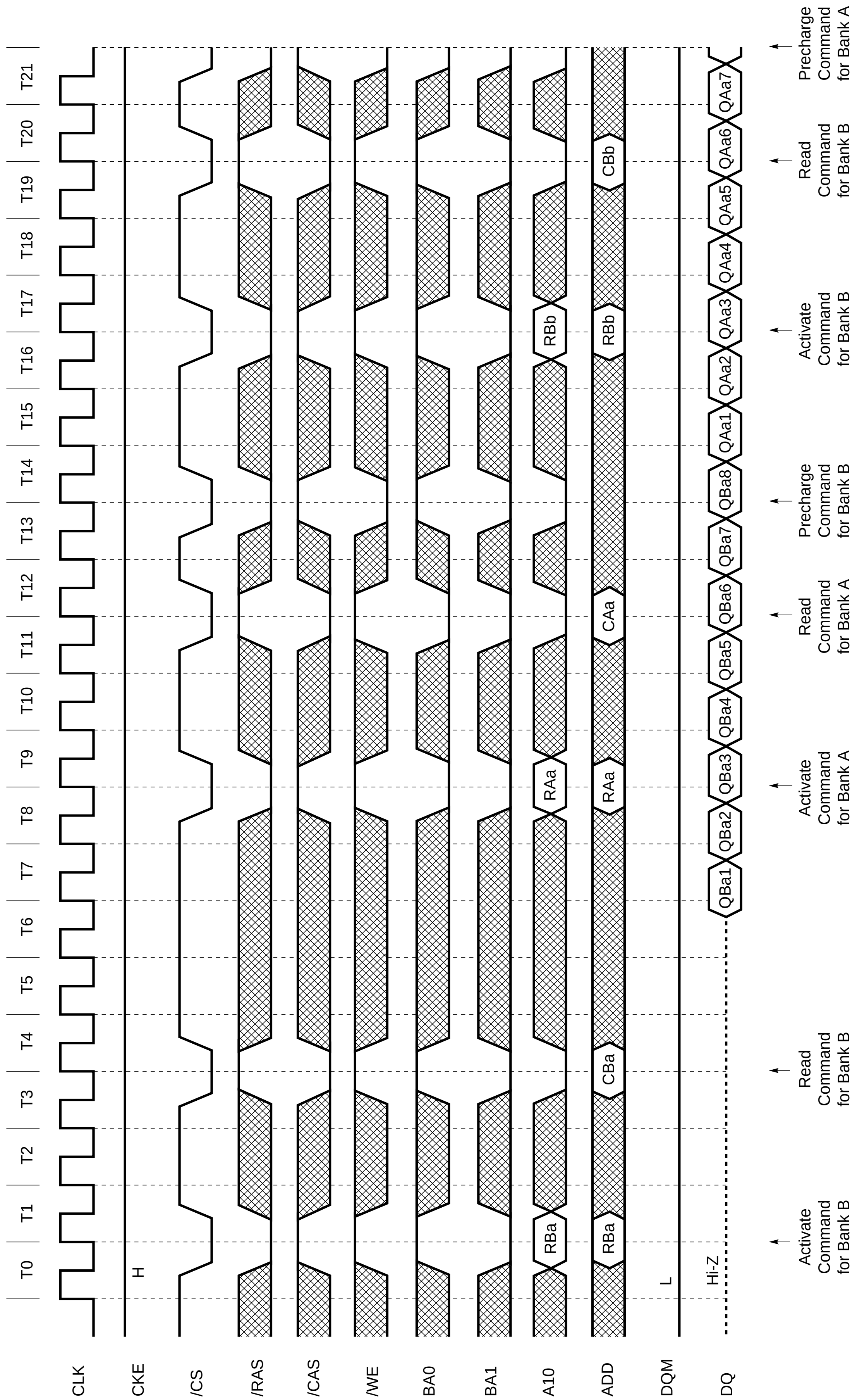
Random Column Write (Page with Same Bank) (2/2) (Burst Length = 4, /CAS Latency = 3)



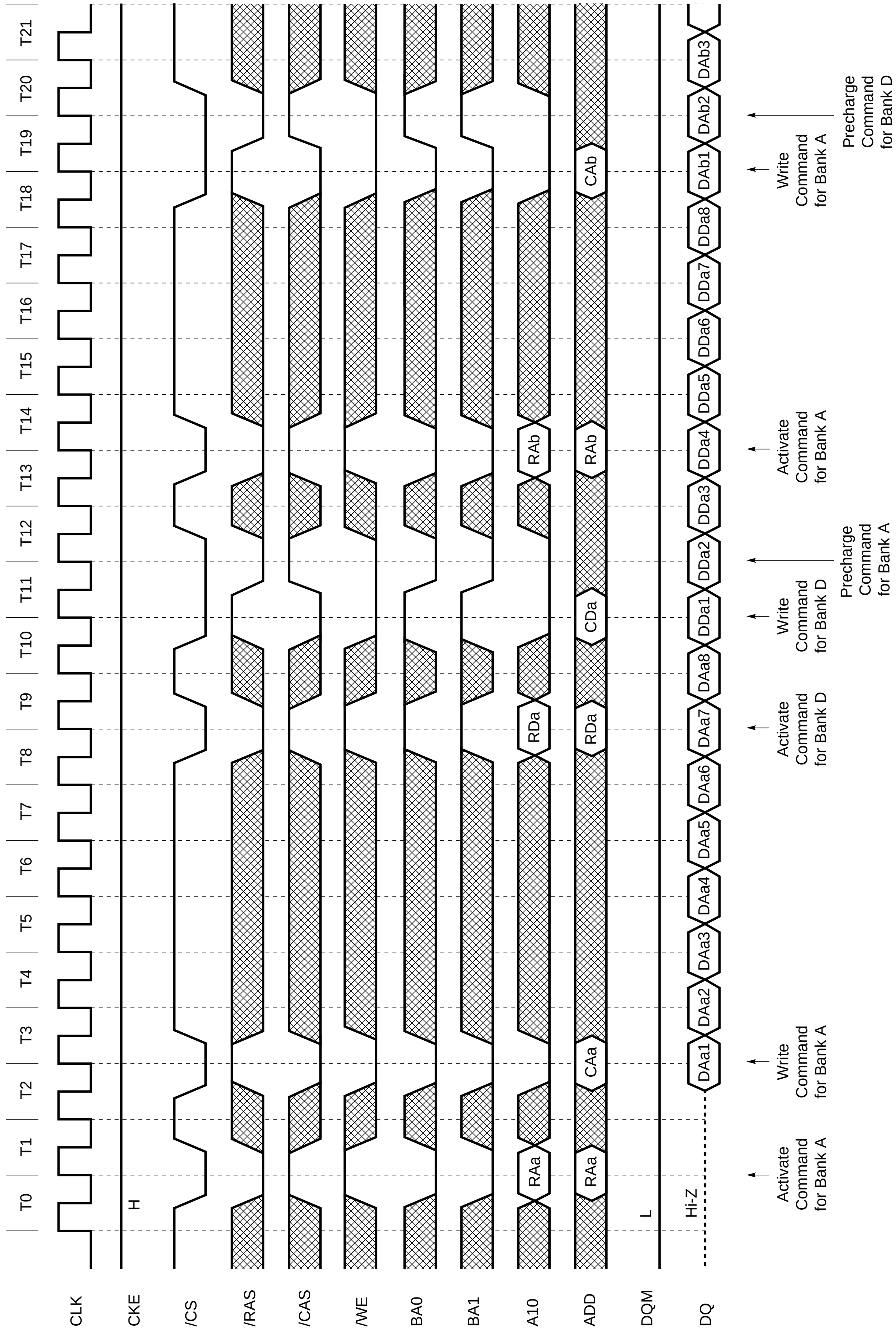
13.14 Random Row Read (Ping-Pong Banks) (1/2) (Burst Length = 8, /CAS Latency = 2)



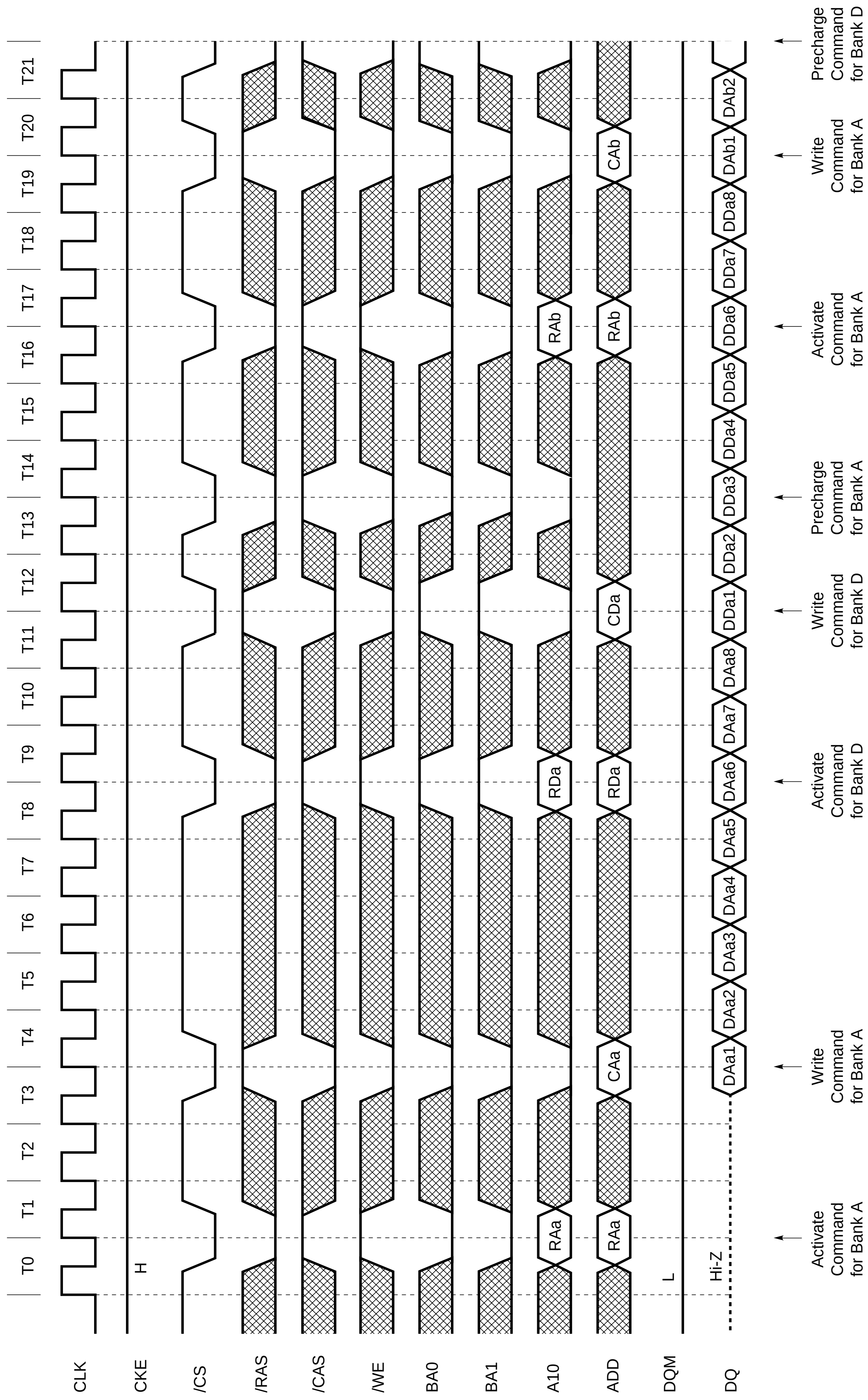
Random Row Read (Ping-Pong Banks) (2/2) (Burst Length = 8, /CAS Latency = 3)



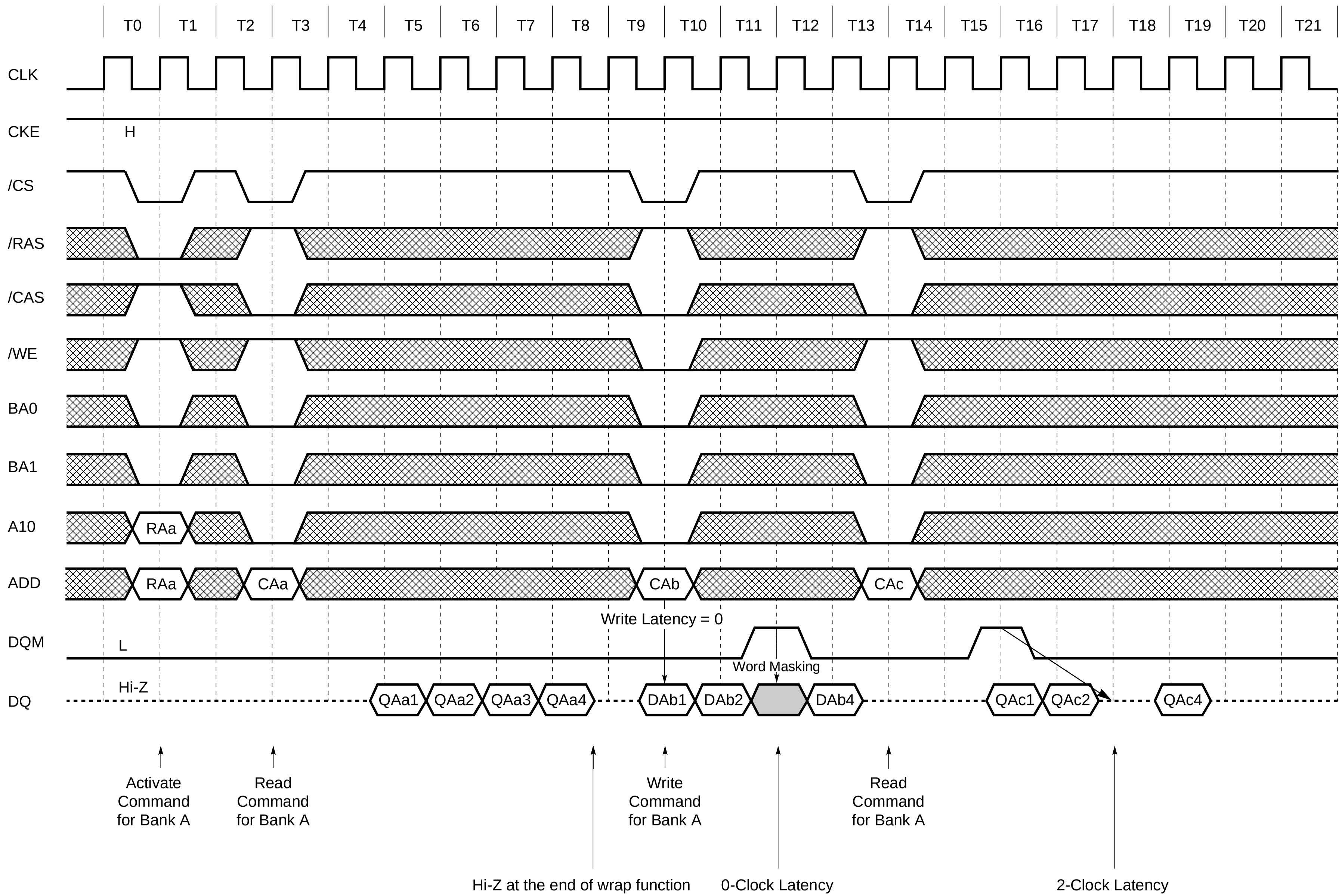
13.15 Random Row Write (Ping-Pong Banks) (1/2) (Burst Length = 8, /CAS Latency = 2)



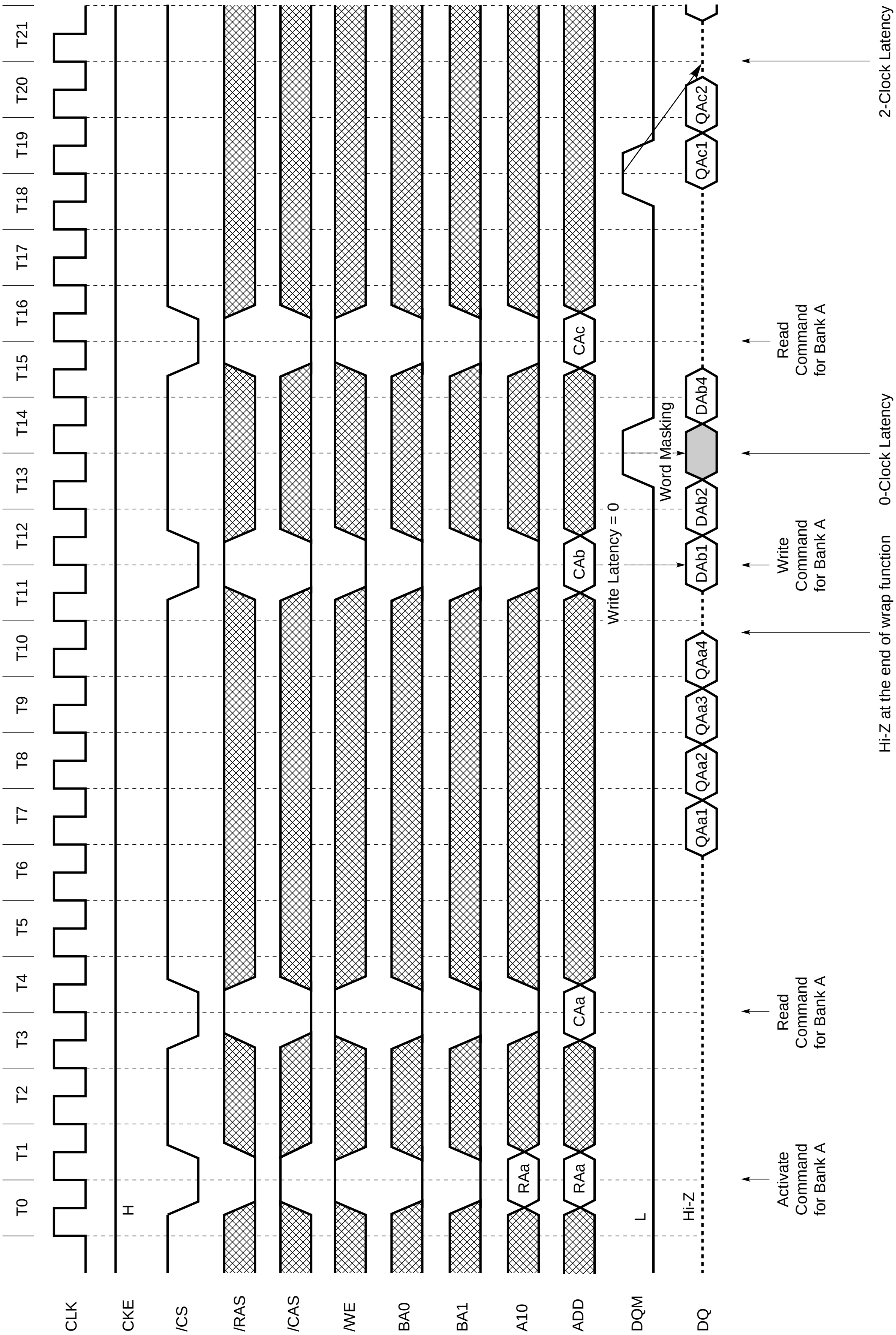
Random Row Write (Ping-Pong Banks) (2/2) (Burst Length = 8, /CAS Latency = 3)



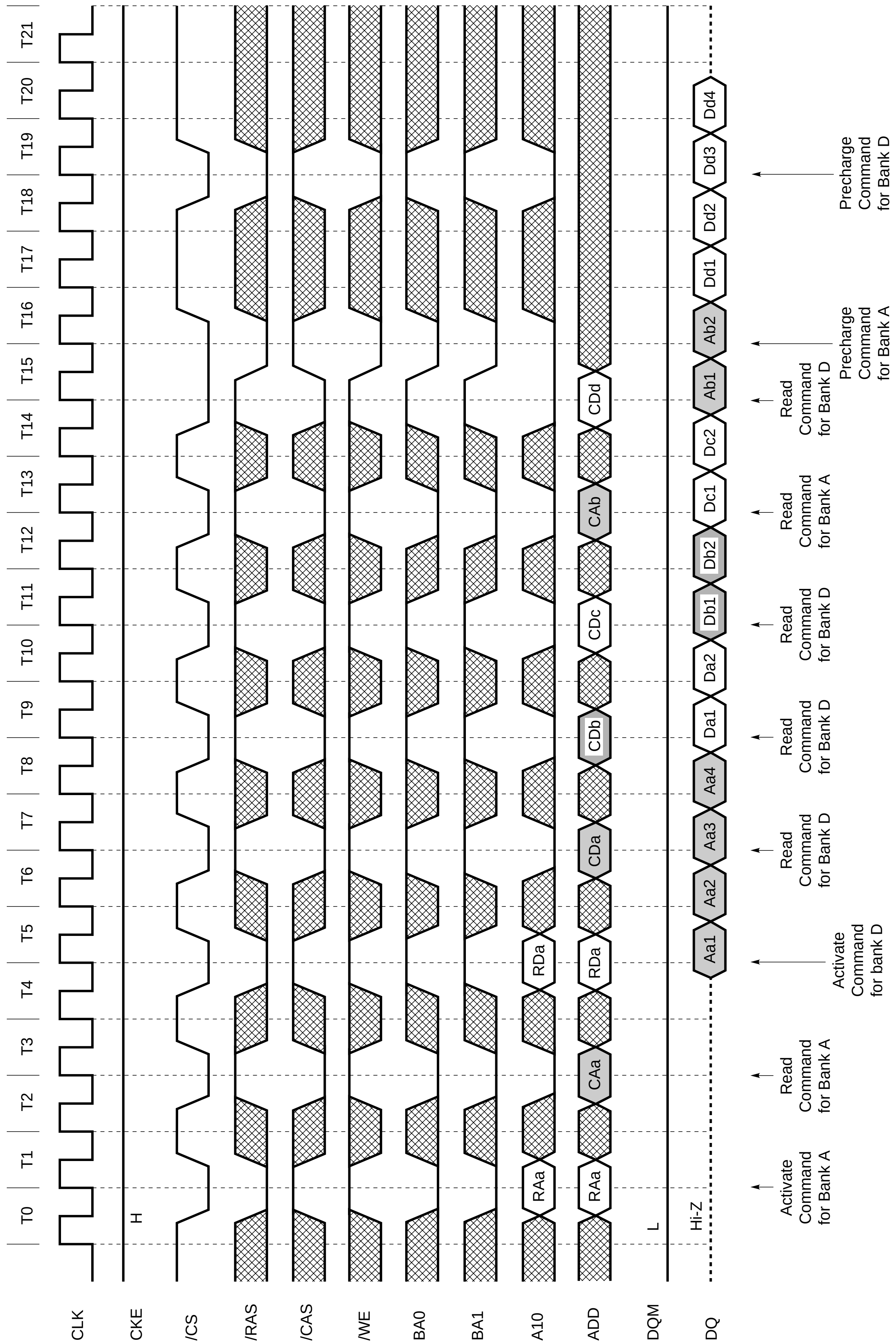
13.16 Read and Write (1/2) (Burst Length = 4, /CAS Latency = 2)



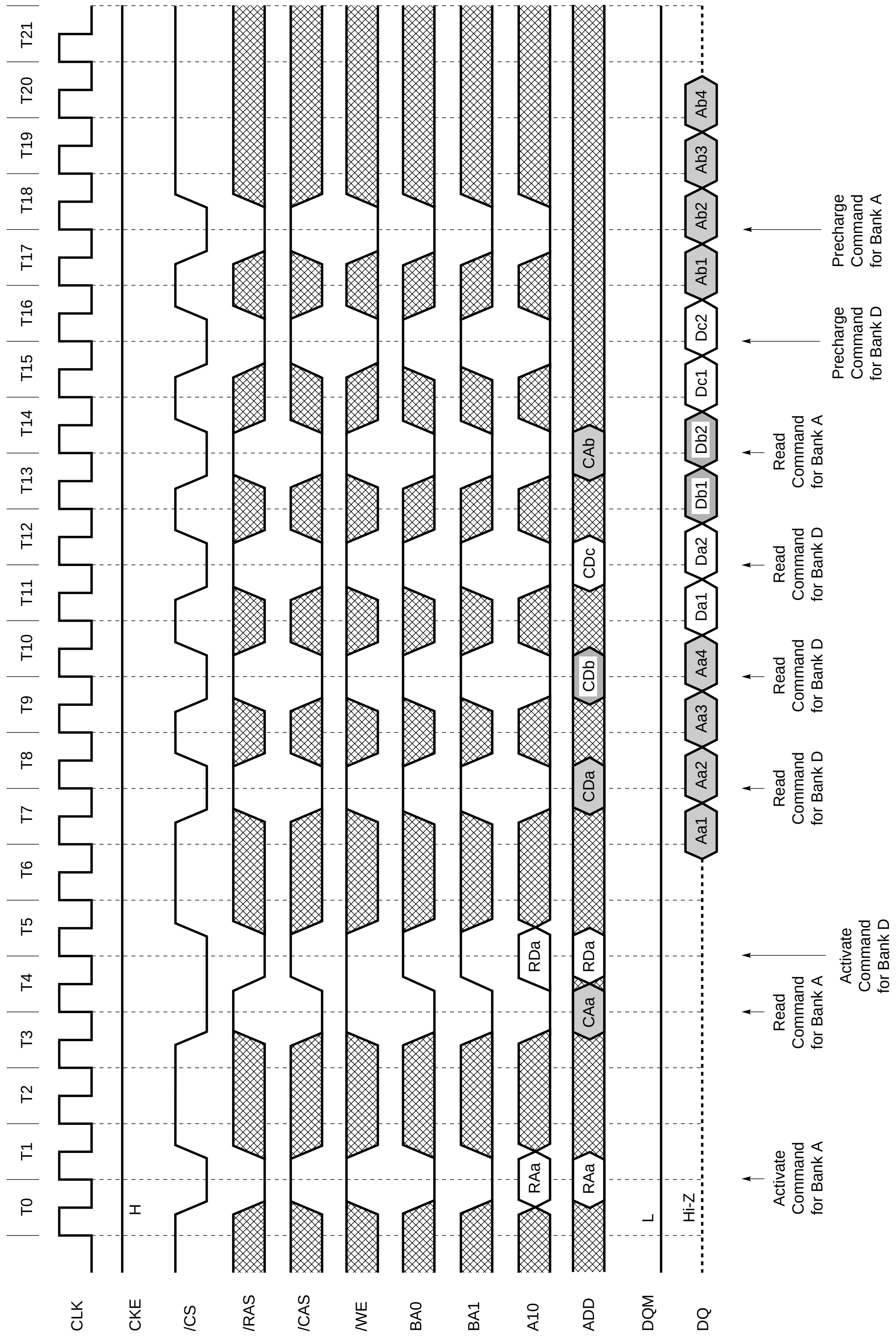
Read and Write (2/2) (Burst Length = 4, /CAS Latency = 3)



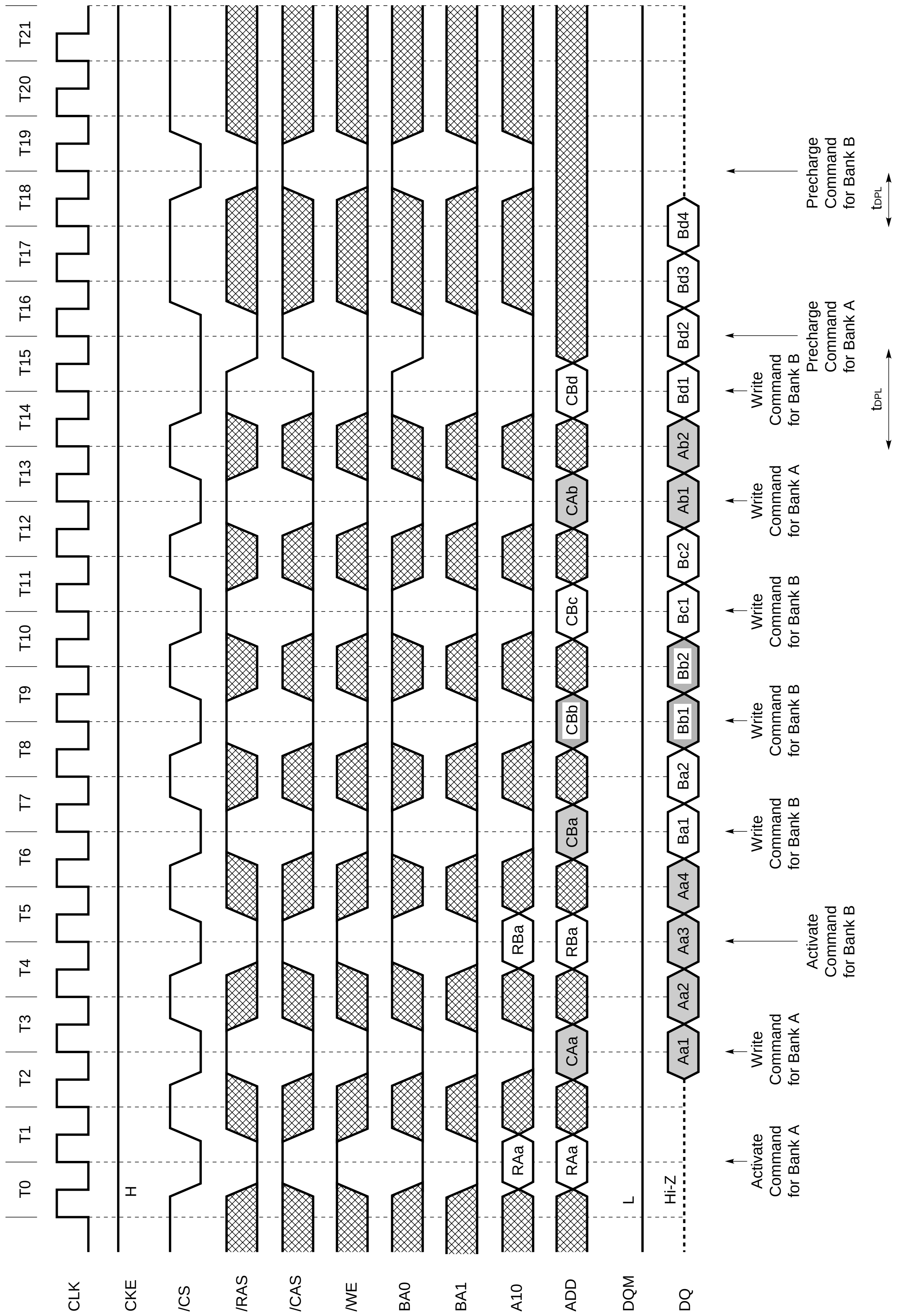
13.17 Interleaved Column Read Cycle (1/2) (Burst Length = 4, /CAS Latency = 2)



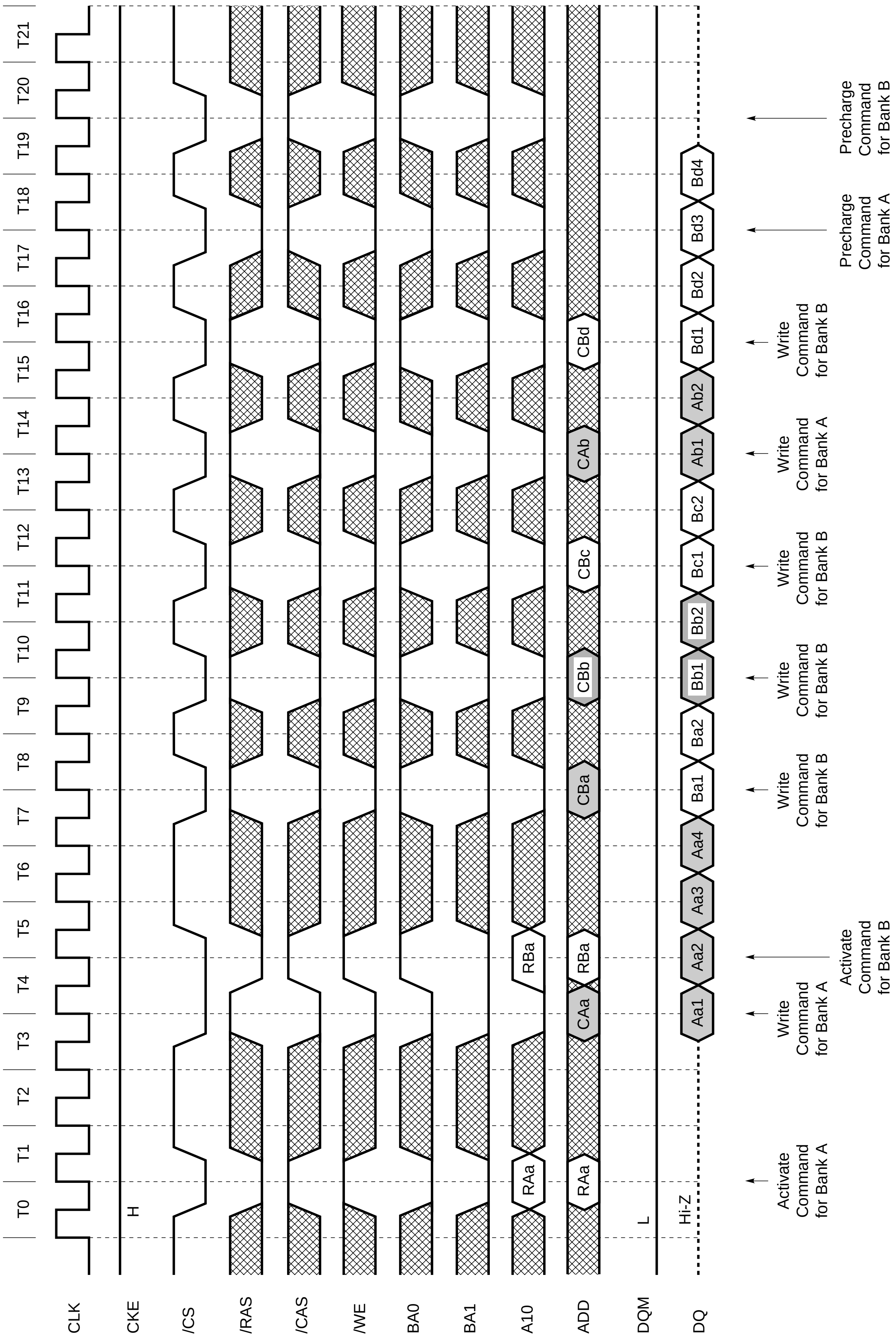
Interleaved Column Read Cycle (2/2) (Burst Length = 4, /CAS Latency = 3)



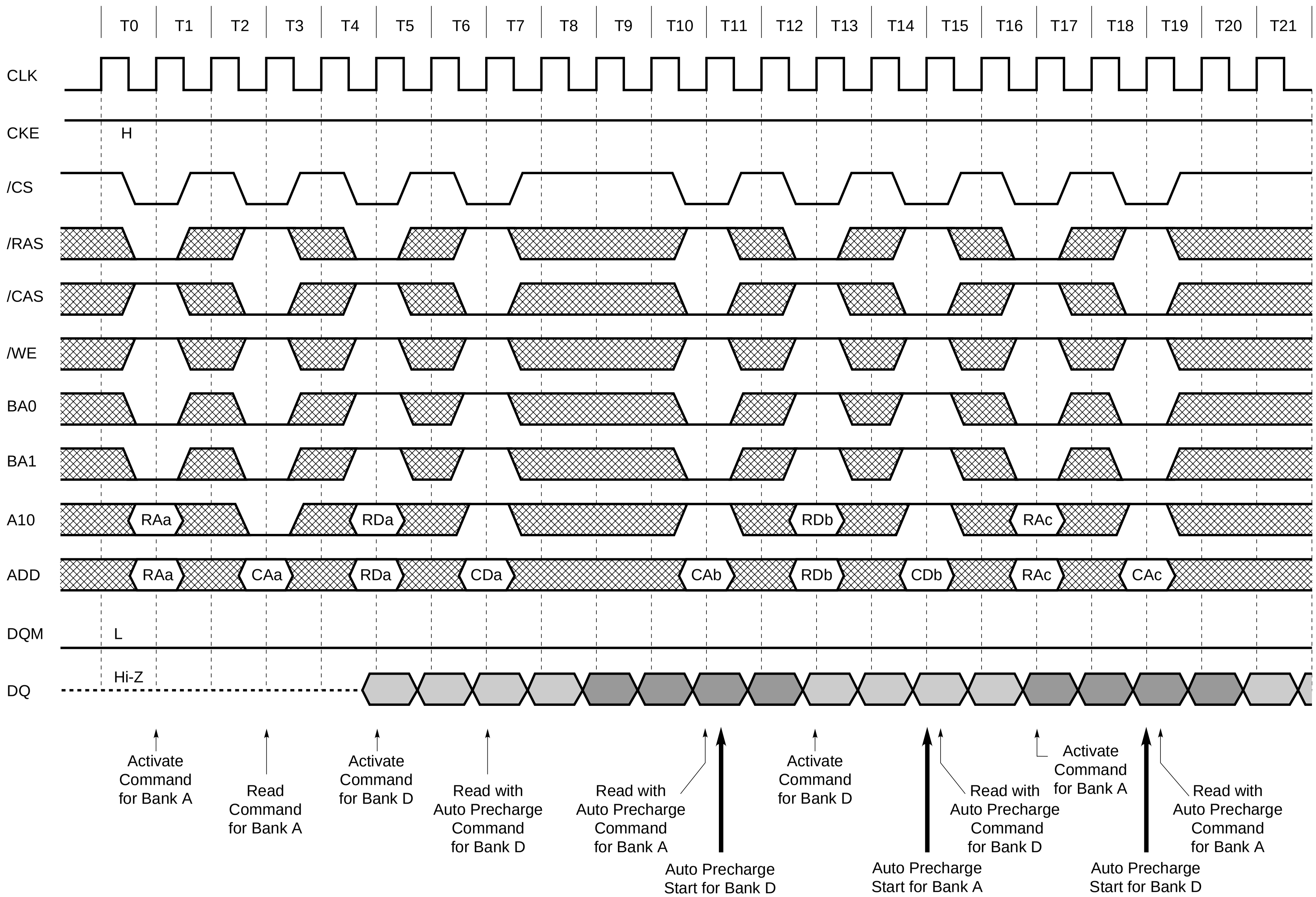
13.18 Interleaved Column Write Cycle (1/2) (Burst Length = 4, /CAS Latency = 2)



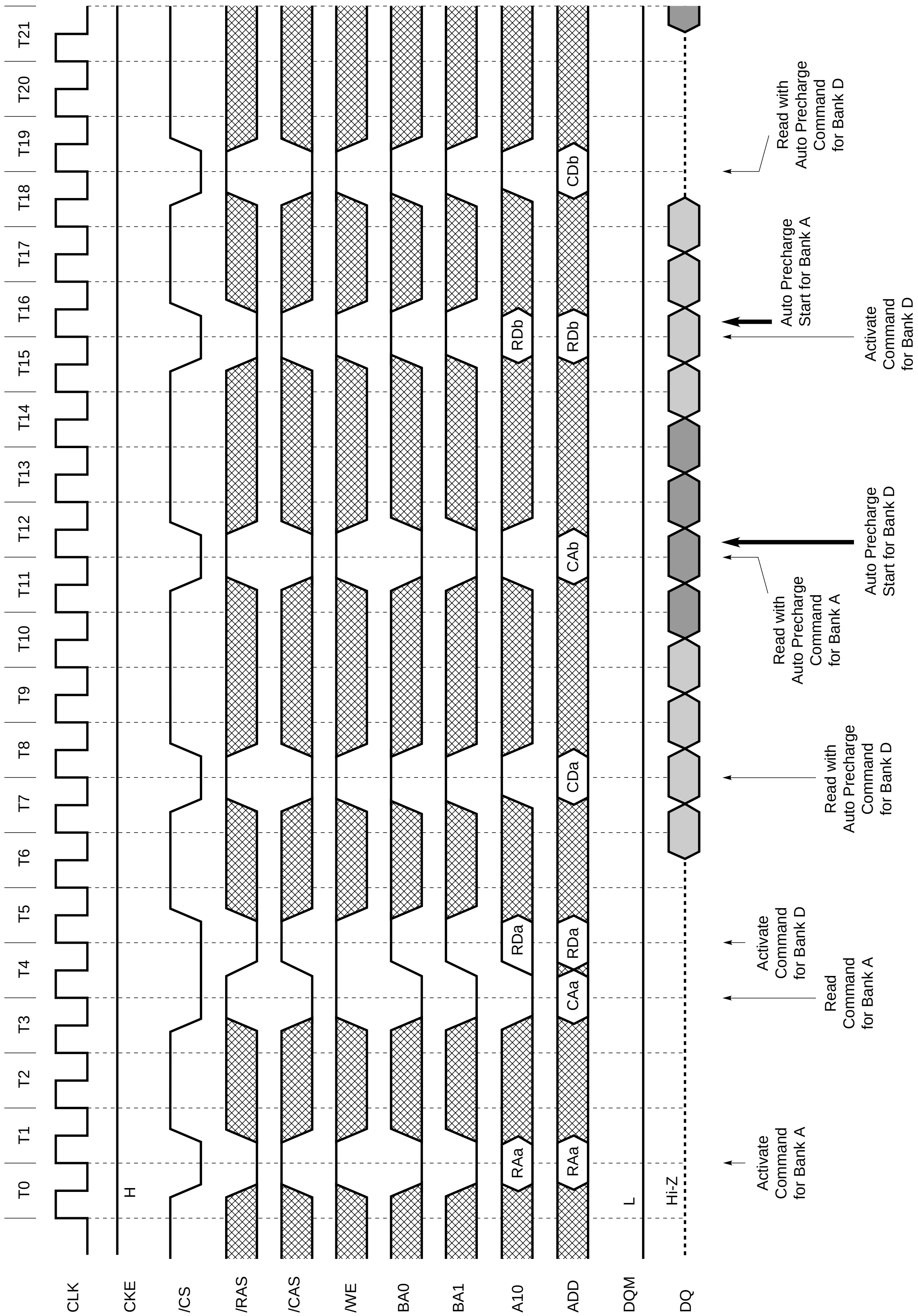
Interleaved Column Write Cycle (2/2) (Burst Length = 4, /CAS Latency = 3)



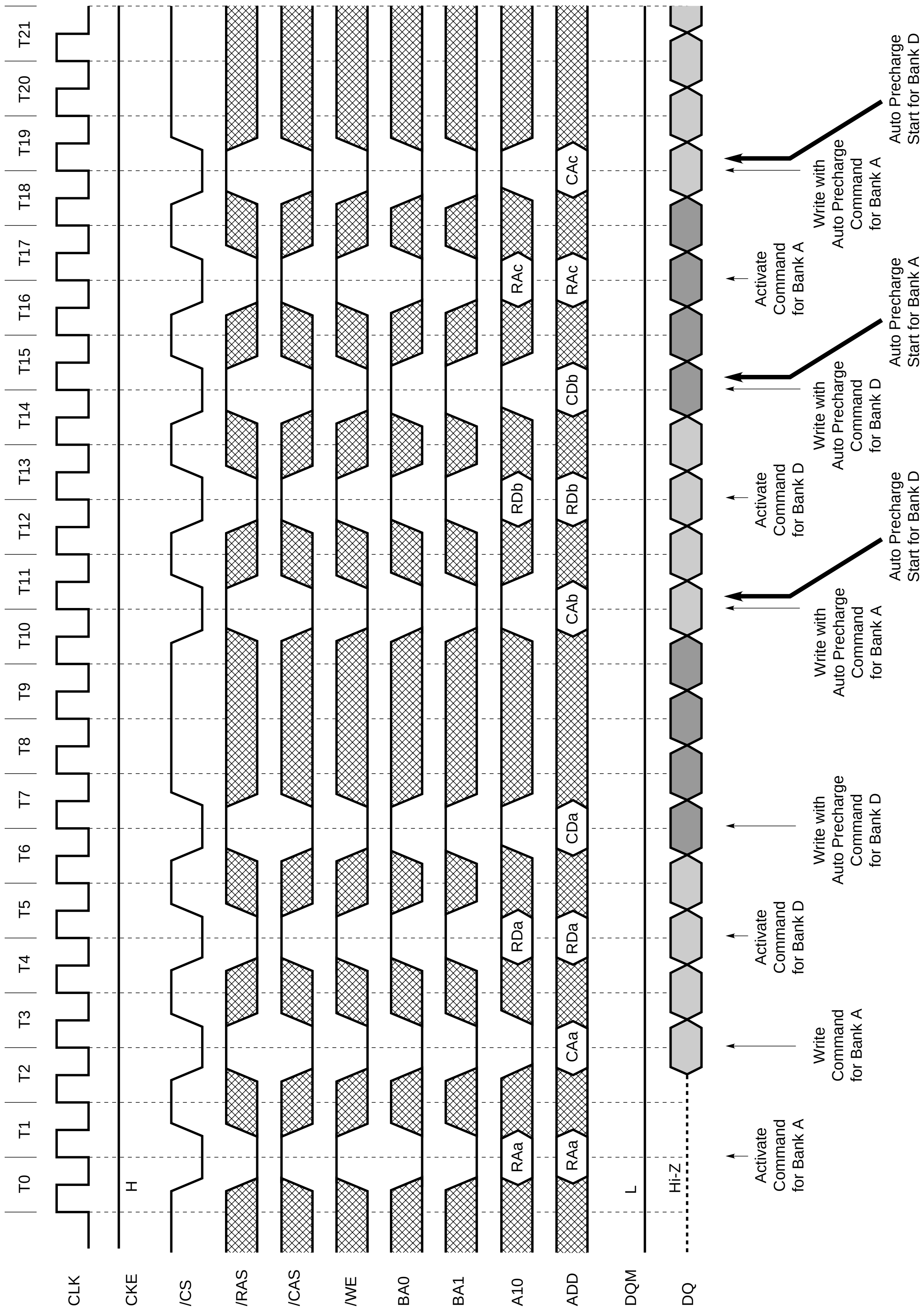
13.19 Auto Precharge after Read Burst (1/2) (Burst Length = 4, /CAS Latency = 2)



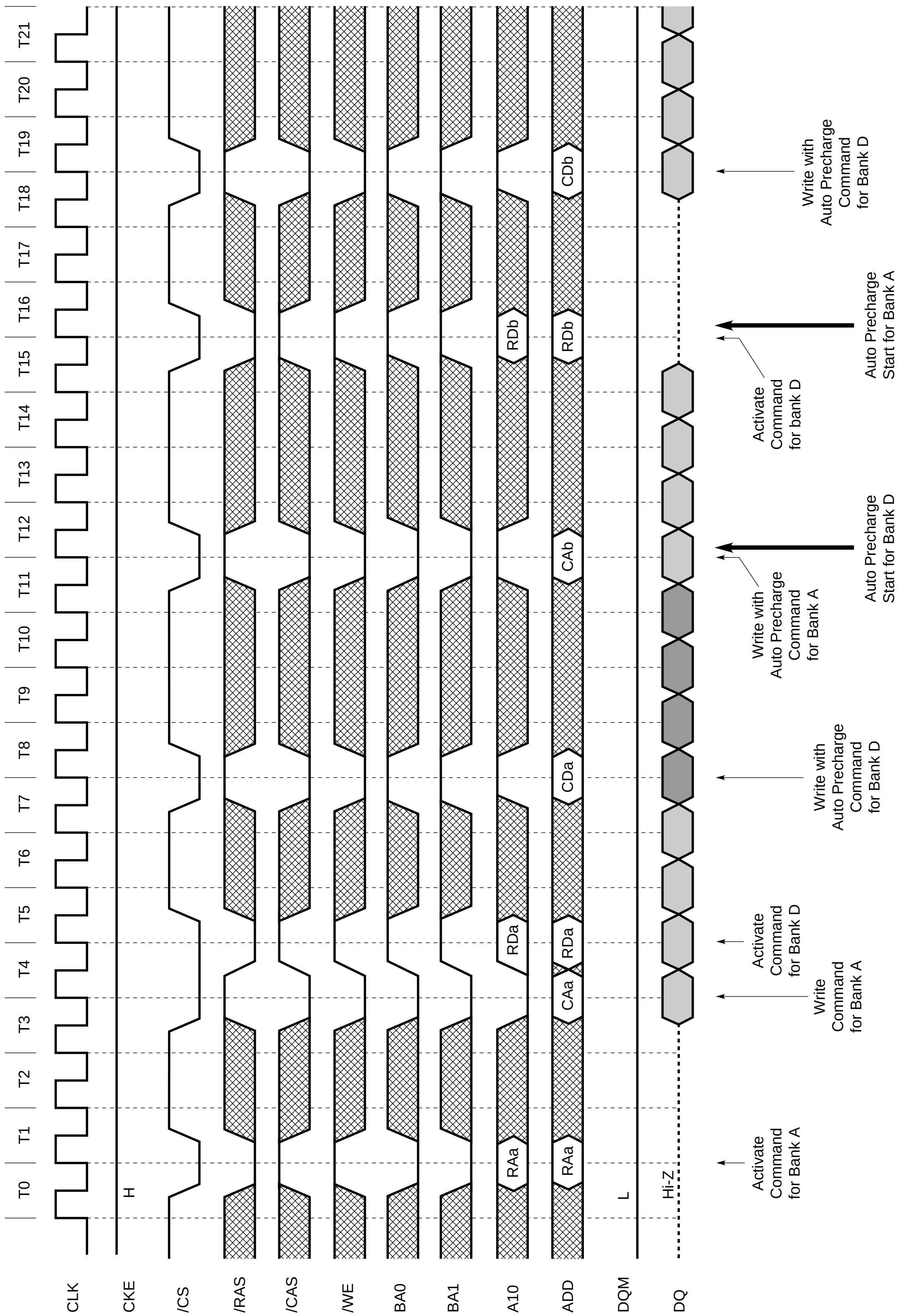
Auto Precharge after Read Burst (2/2) (Burst Length = 4, /CAS Latency = 3)



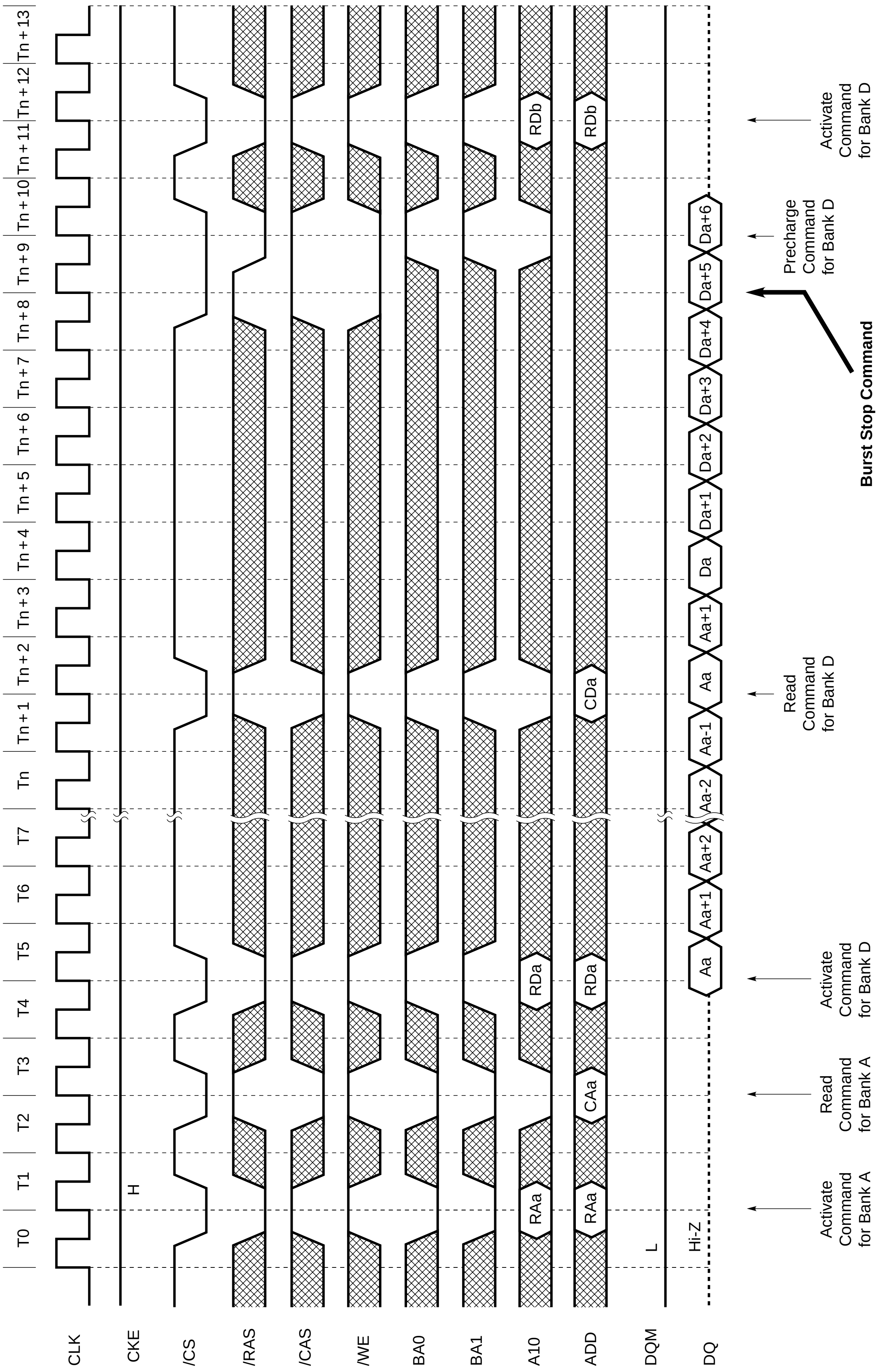
13.20 Auto Precharge after Write Burst (1/2) (Burst Length = 4, /CAS Latency = 2)



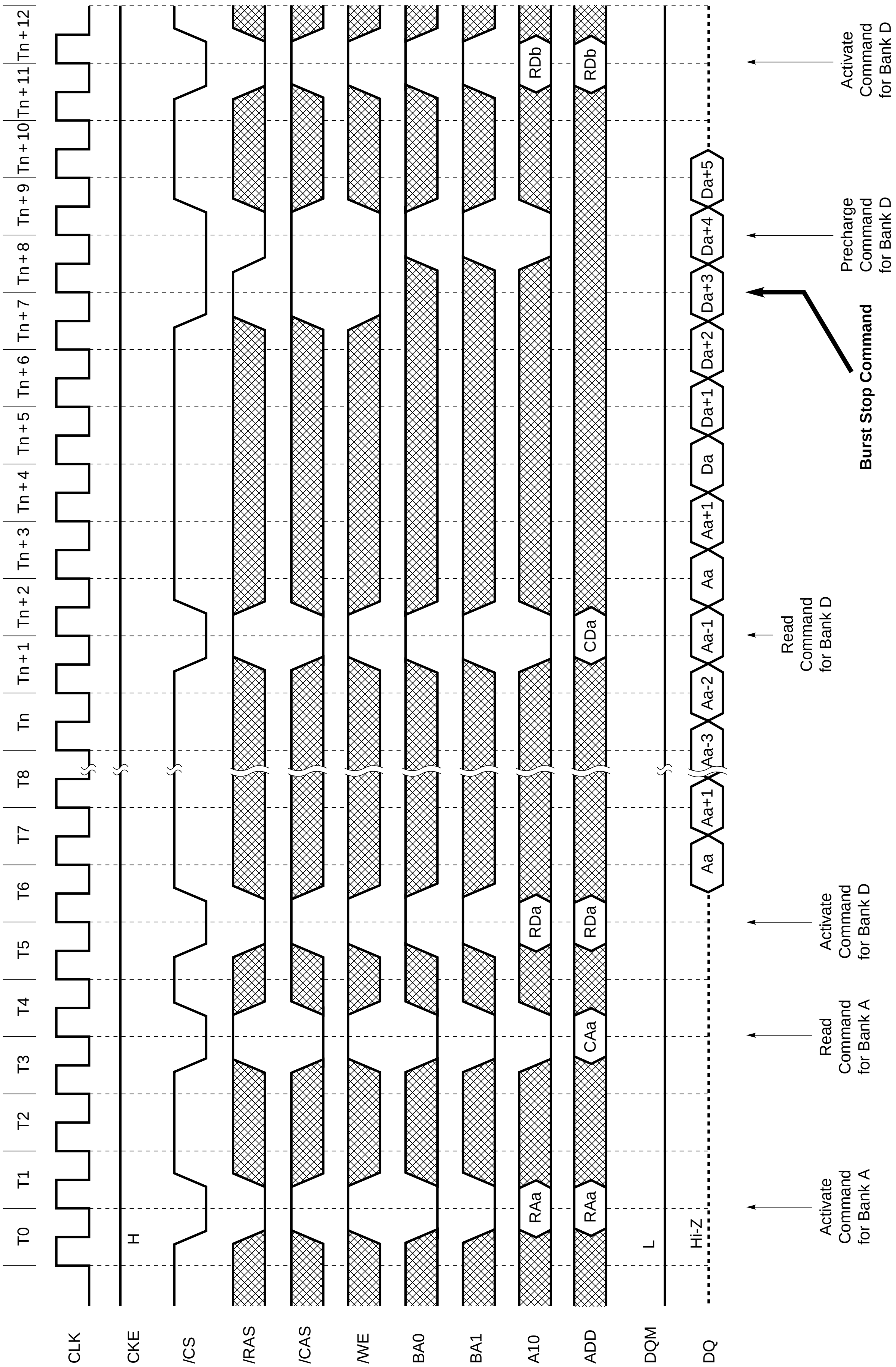
Auto Precharge after Write Burst (2/2) (Burst Length = 4, /CAS Latency = 3)



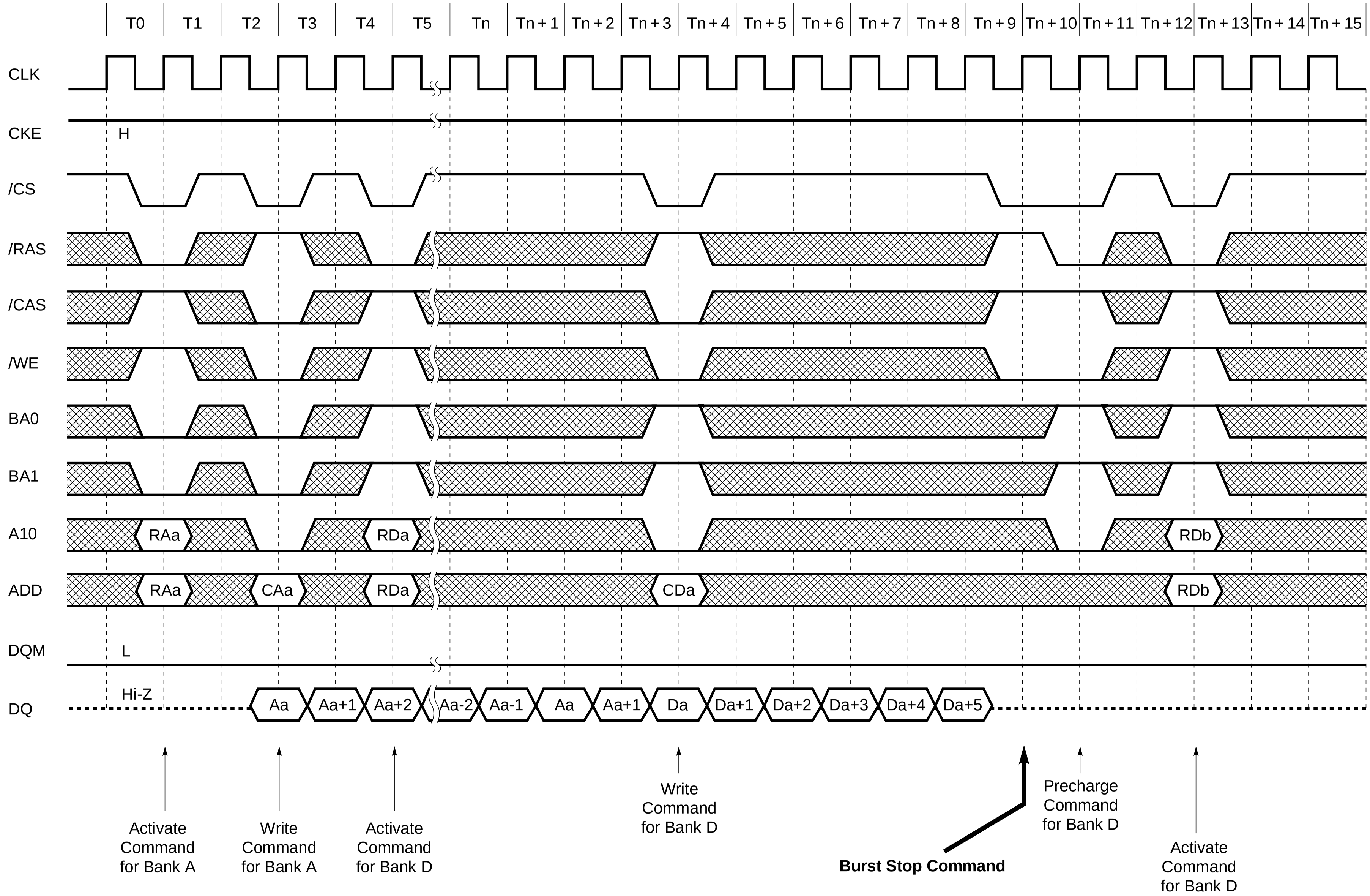
13.21 Full Page Read Cycle (1/2) (/CAS Latency = 2)



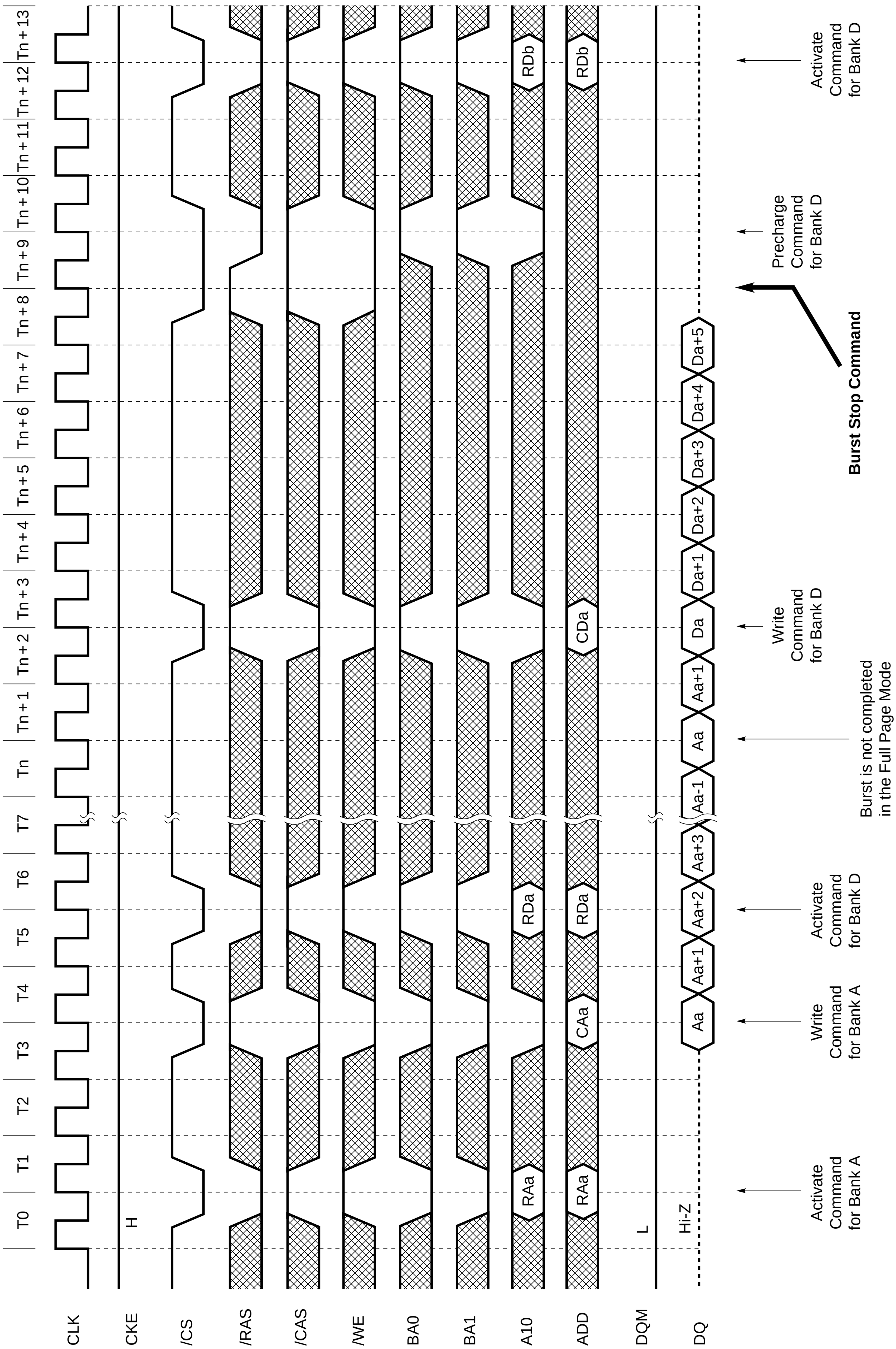
Full Page Read Cycle (2/2) (/CAS latency = 3)



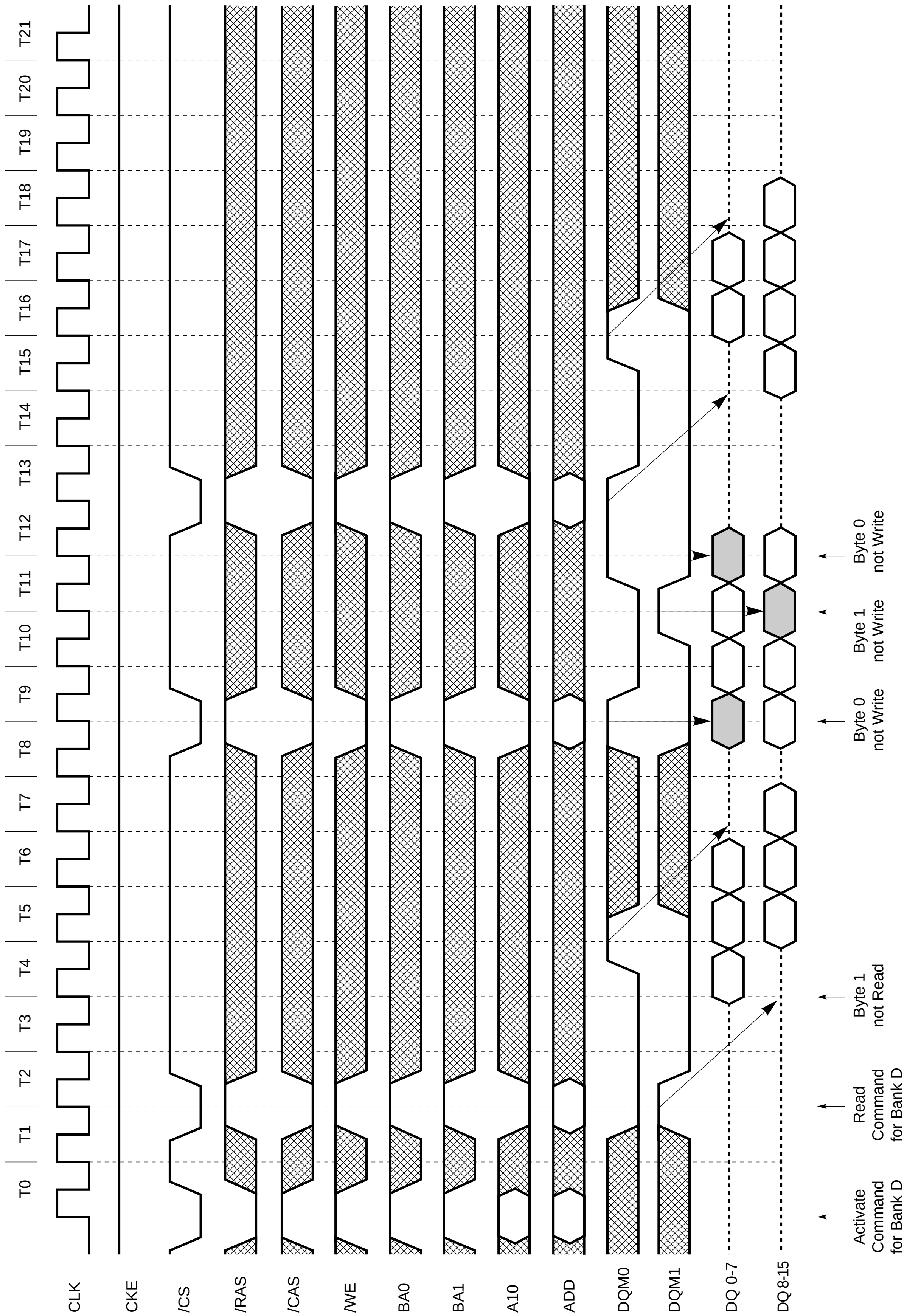
13.22 Full Page Write Cycle (1/2) (/CAS latency = 2)



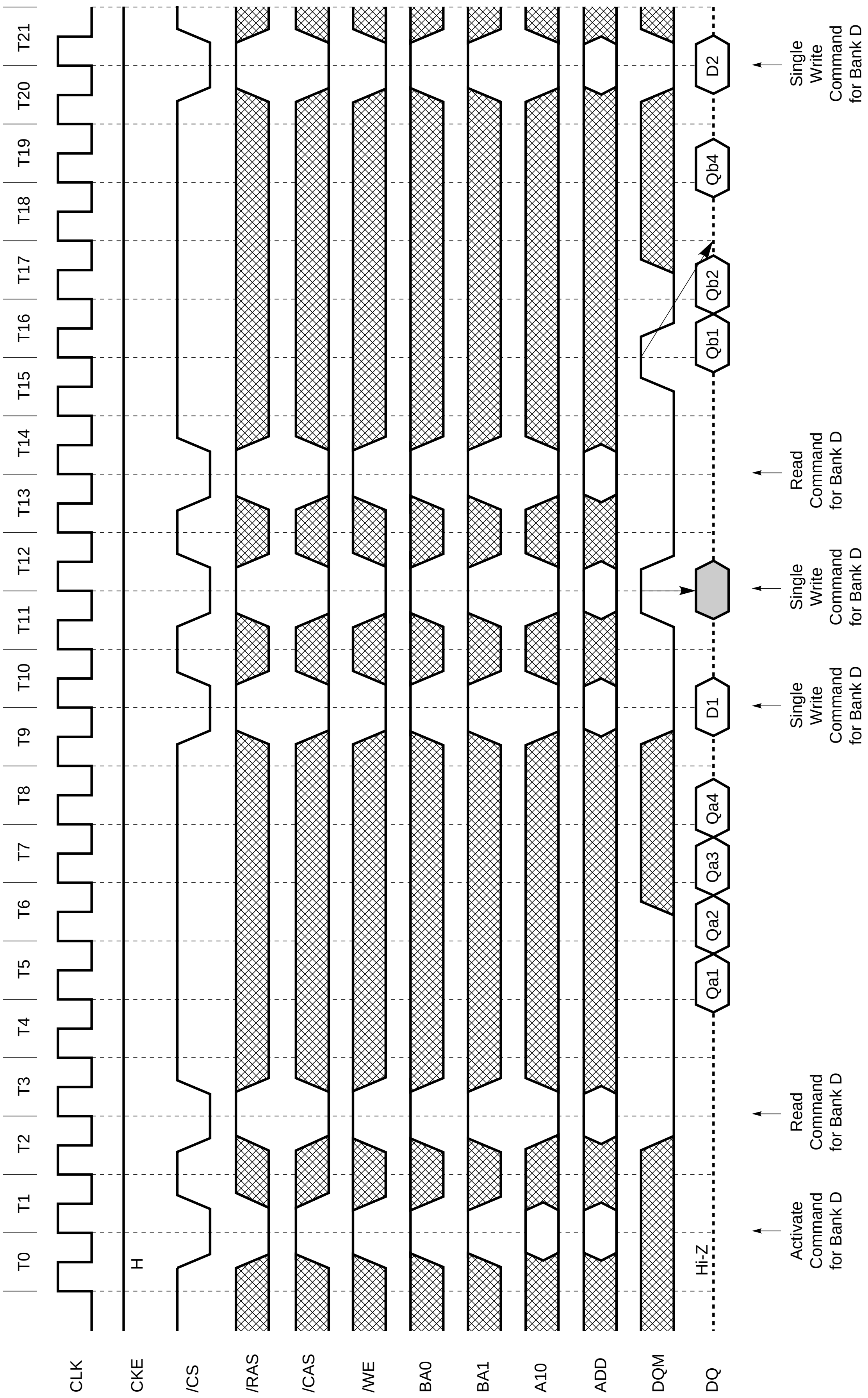
Full Page Write Cycle (2/2) (/CAS Latency = 3)



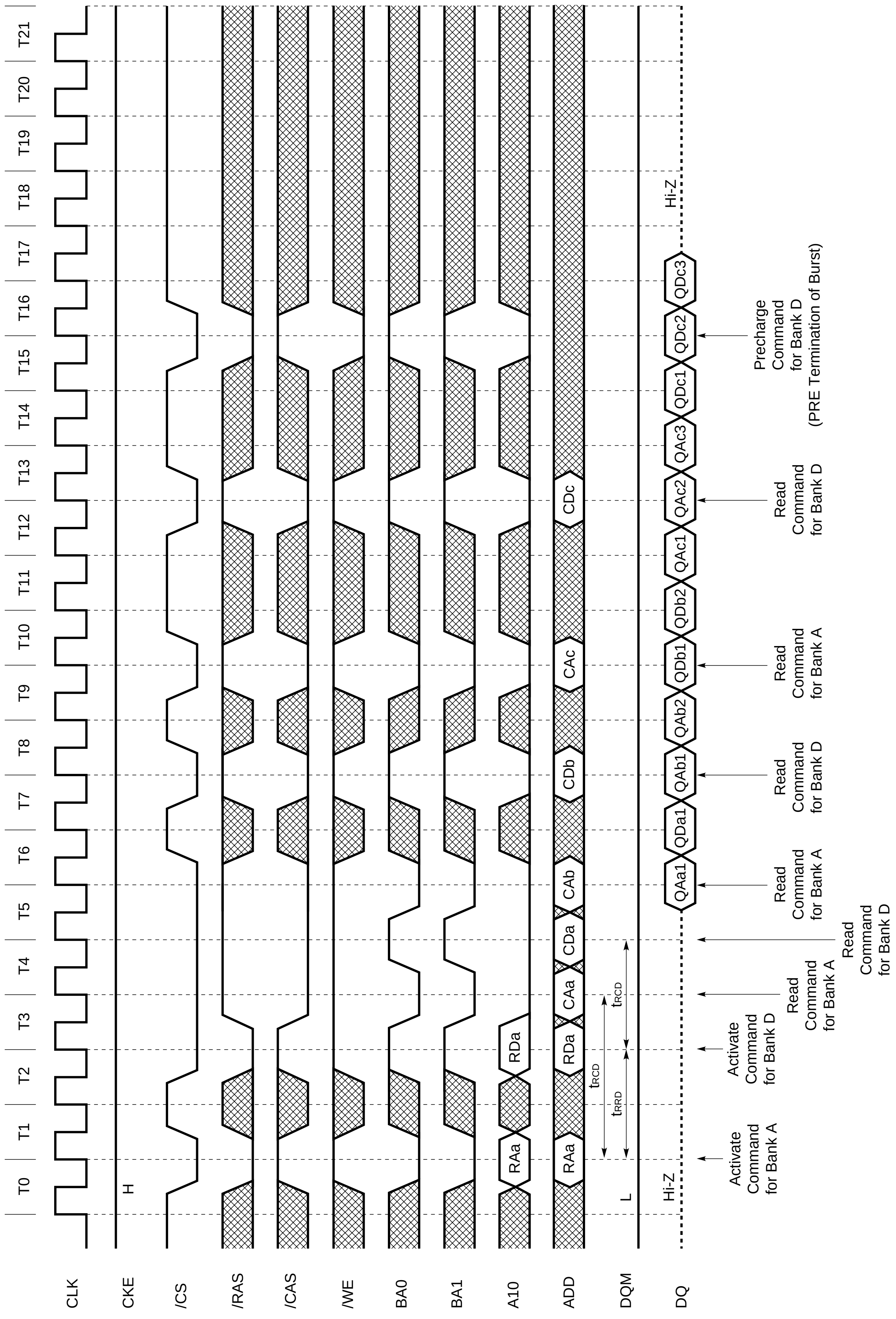
13.23 Byte Write Operation (Burst Length = 4, /CAS Latency = 2)



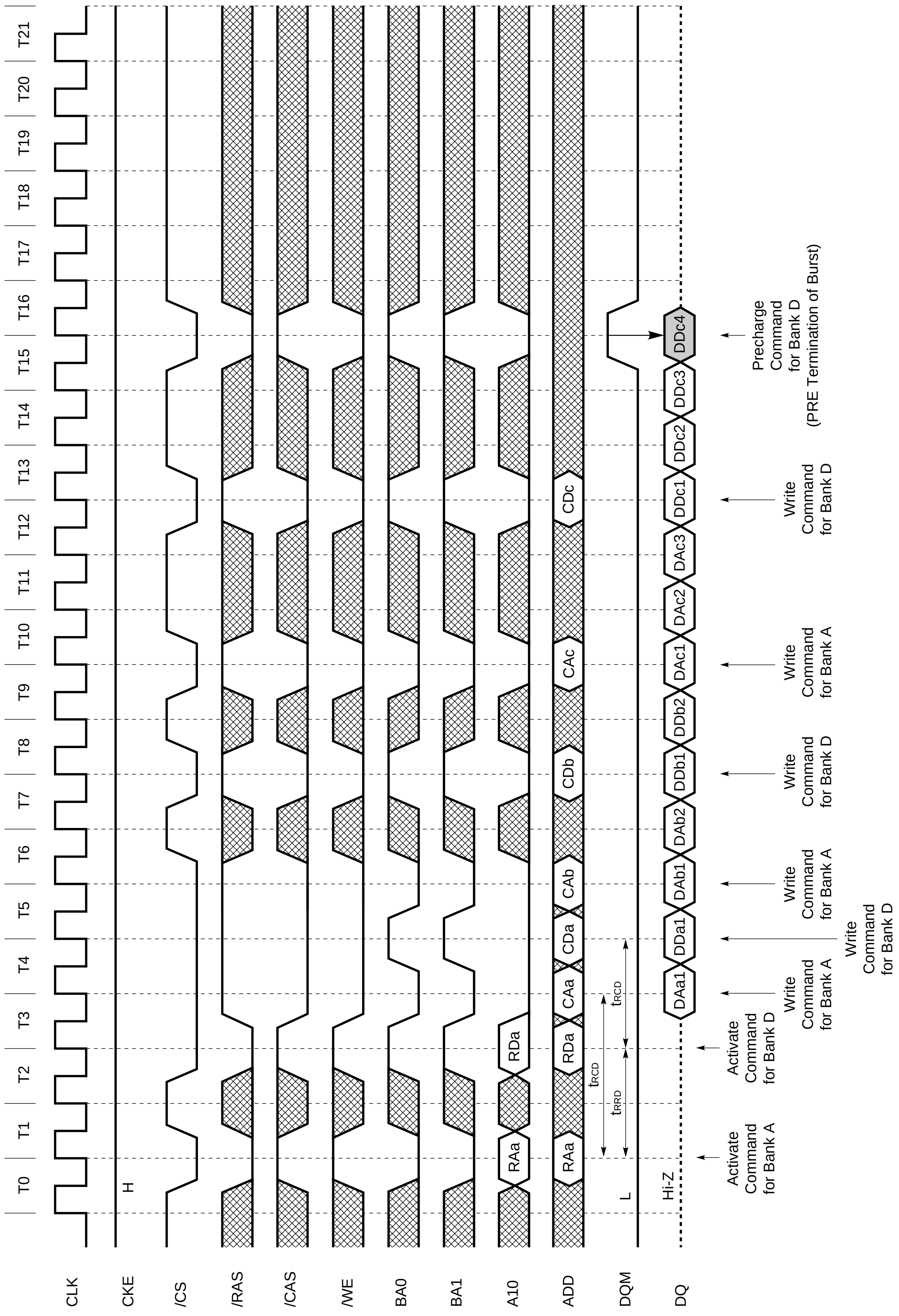
13.24 Burst Read and Single Write (Option) (Burst Length = 4, /CAS Latency = 2)



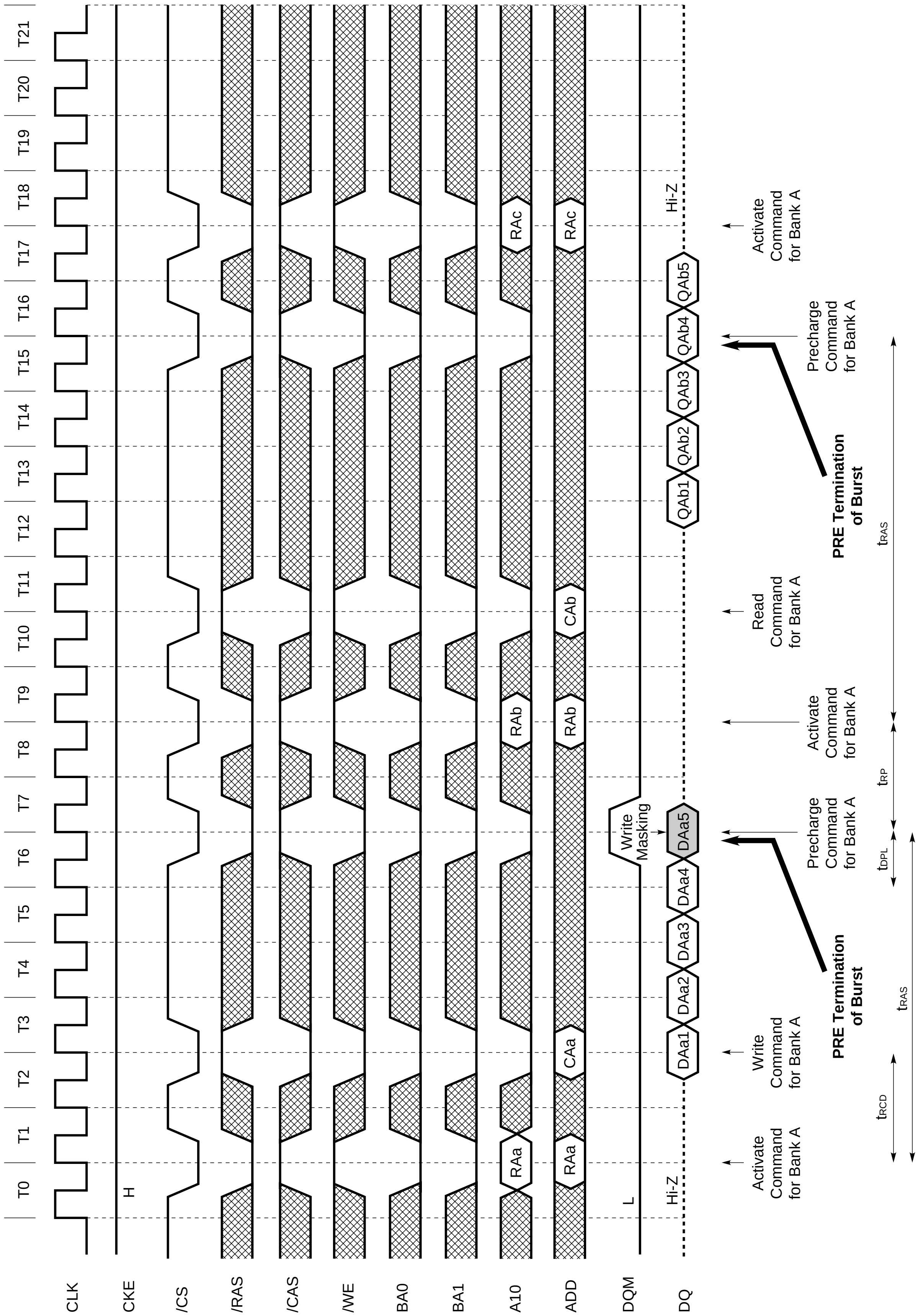
13.25 Full Page Random Column Read (Burst Length = Full Page, /CAS Latency = 2)



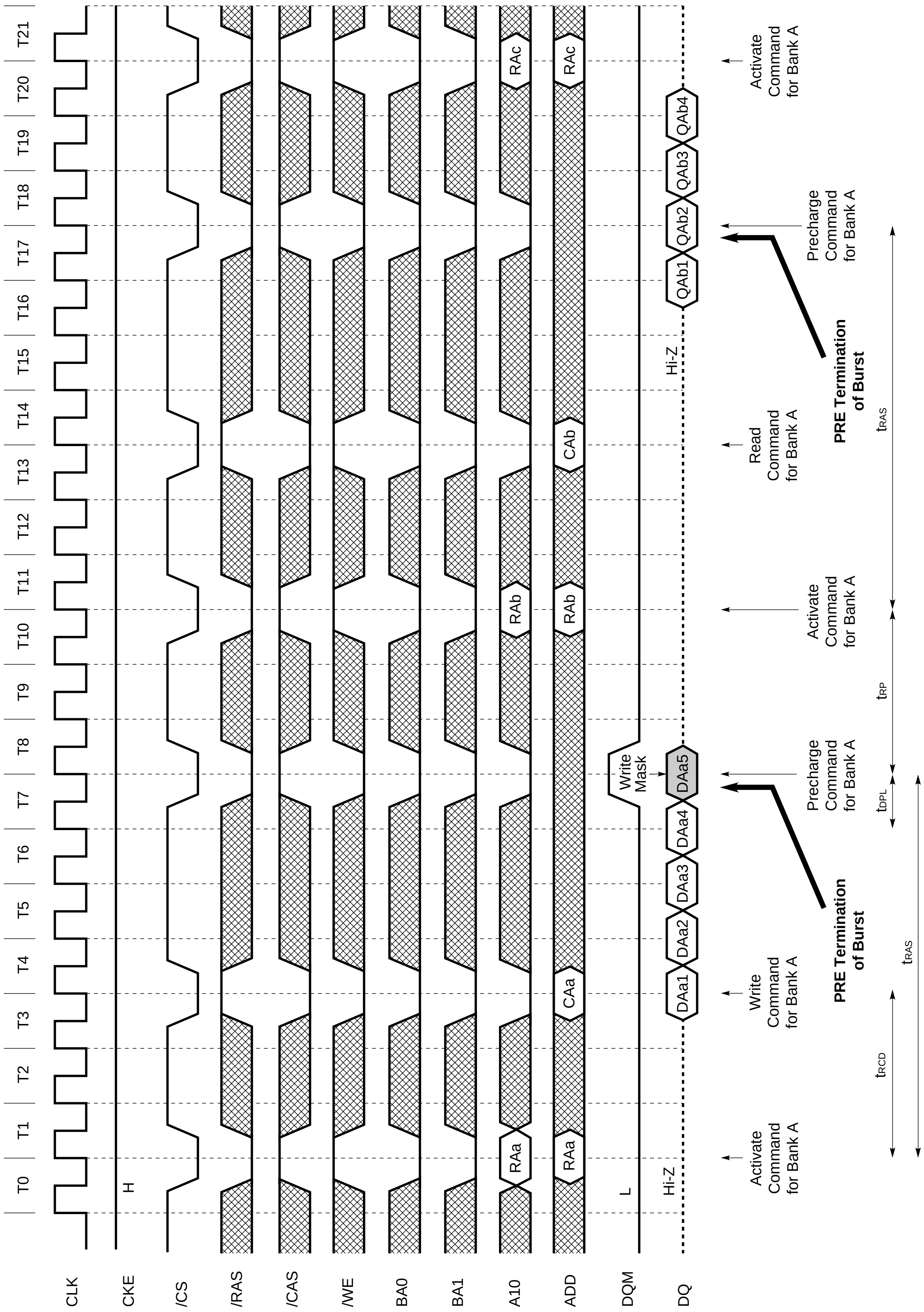
13.26 Full Page Random Column Write (Burst Length = Full Page, /CAS Latency = 2)



13.27 PRE (Precharge) Termination of Burst (1/2) (Burst Length = 8, /CAS Latency = 2)

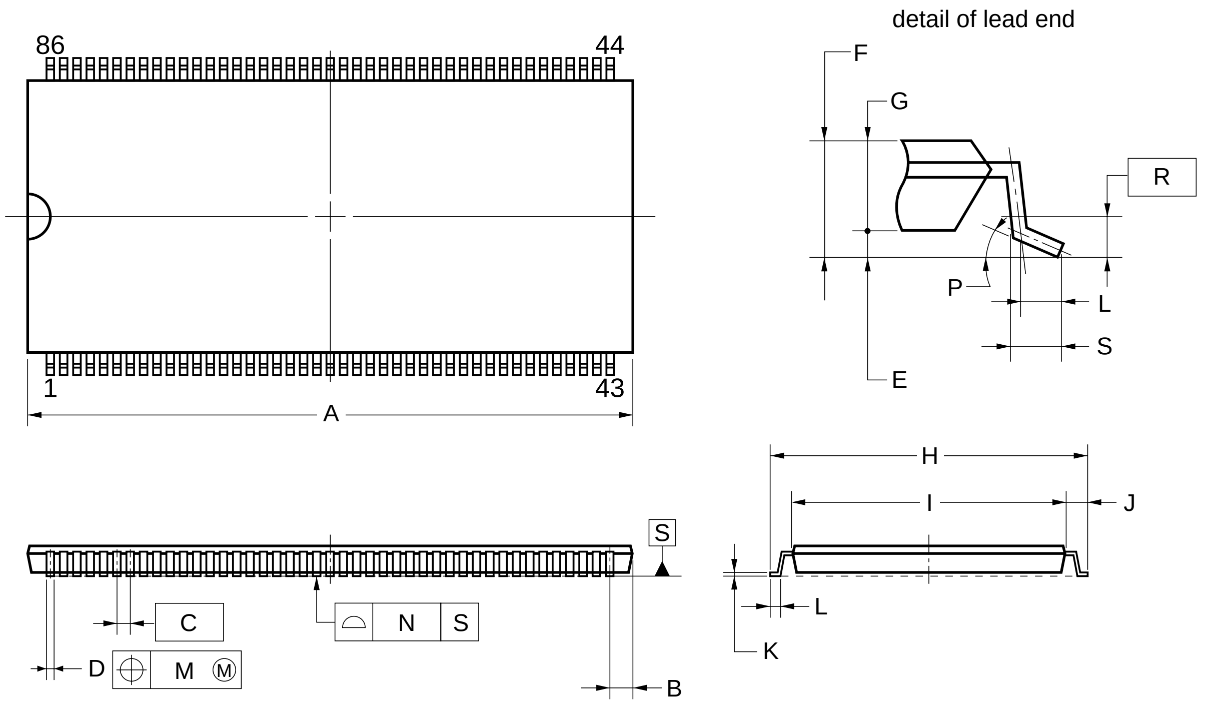


PRE (Precharge) Termination of Burst (2/2) (Burst Length = 8, /CAS Latency = 3)



★ **14. Package Drawing**

86-PIN PLASTIC TSOP (II) (10.16 mm (400))



NOTES

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. Dimension "A" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

ITEM	MILLIMETERS
A	22.22±0.05
B	0.765 MAX.
C	0.5 (T.P.)
D	$0.22^{+0.08}_{-0.07}$
E	0.10±0.05
F	1.1±0.1
G	1.00
H	11.76±0.20
I	10.16±0.10
J	0.80±0.20
K	$0.145^{+0.025}_{-0.015}$
L	0.50
M	0.08
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S86G5-50-9JH-1

15. Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD4564323.

Type of Surface Mount Device

μPD4564323G5: 86-pin Plastic TSOP (II) (10.16 mm (400))

16. Revision History

Edition / Date	Page		Description	
	This edition	Previous edition	Type of revision	Location
1st edition / June 1999	–	–	–	–
2nd edition / December 1999	p.2	p.2	Deletion	μPD4564323G5-A60L-9JH, 4564323G5-A70L-9JH, 4564323G5-A80L-9JH, μPD4564323G5-A10L-9JH, 4564323G5-A10BL-9JH
	p.3	p.3	Deletion	L (Low Power)
	p.33	p.33	Deletion	I_{CC6} (-AxxL (Maximum))
	p.34	p.34	Modification	Test Conditions
	p.79	p.79	Modification	Package Drawing

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.