GAL6001

High Performance E²CMOS FPLA
Generic Array Logic™

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 30ns Maximum Propagation Delay**
  - **— 27MHz Maximum Frequency**
  - **— 12ns Maximum Clock to Output Delay**
  - **— TTL Compatible 16mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **LOW POWER CMOS**
  - **— 90mA Typical Icc**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **UNPRECEDENTED FUNCTIONAL DENSITY**
  - **— 78 x 64 x 36 FPLA Architecture**
  - **— 10 Output Logic Macrocells**
  - **— 8 Buried Logic Macrocells**
  - **— 20 Input and I/O Logic Macrocells**
- **HIGH-LEVEL DESIGN FLEXIBILITY**
  - **— Asynchronous or Synchronous Clocking**
  - **— Separate State Register and Input Clock Pins**
  - **— Functional Superset of Existing 24-pin PAL® and FPLA Devices**
- **APPLICATIONS INCLUDE:**
  - **— Sequencers**
  - **— State Machine Control**
  - **— Multiple PLD Device Integration**

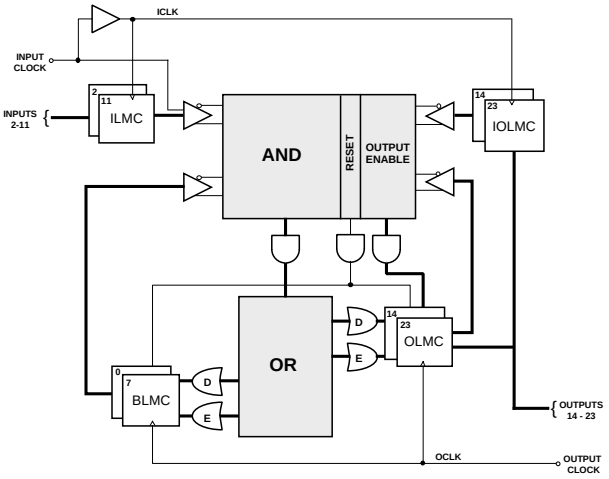
Description

Using a high performance E²CMOS technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers a high degree of functional integration and flexibility in a 24-pin, 300-mil package.

The GAL6001 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram



Macrocell Names

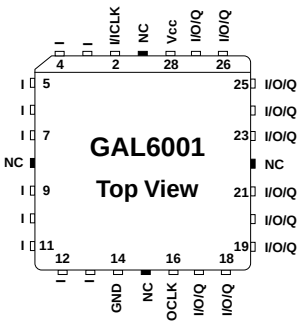
ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

Pin Names

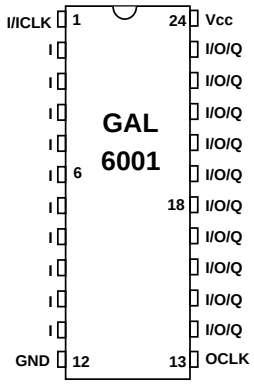
I_0 - I_{10}	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V_{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

Pin Configuration

PLCC



DIP



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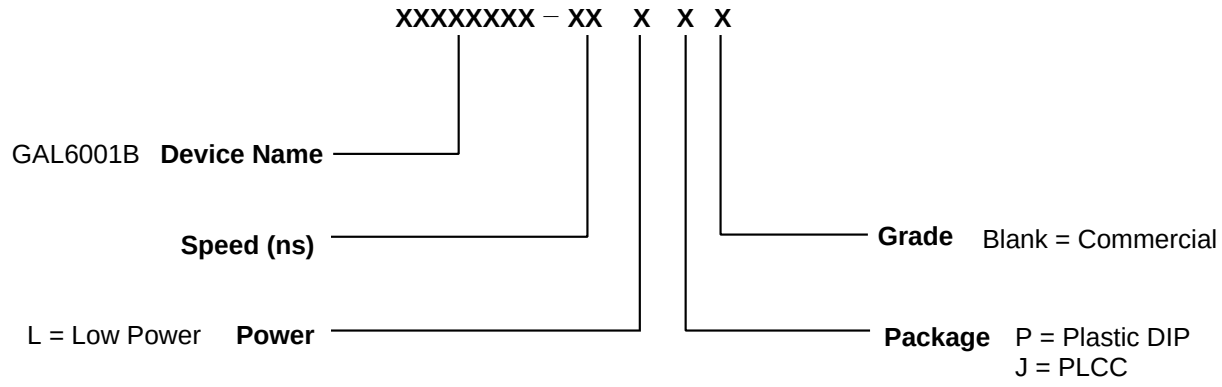
GAL6001 Ordering Information

Commercial Grade Specifications

Tpd (ns)	Fmax (MHz)	Icc (mA)	Ordering #	Package
30	27	150	GAL6001B-30LP	24-Pin Plastic DIP
		150	GAL6001B-30LJ	28-Lead PLCC

Part Number Description



Input Logic Macrocell (ILMC) and I/O Logic Macrocell (IOLMC)

The GAL6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Configurable input blocks provide system designers with unparalleled design flexibility. With the GAL6001, external registers and latches are not necessary.

Both the ILMC and the IOLMC are block configurable. However, the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

Output Logic Macrocell (OLMC) and Buried Logic Macrocell (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinatorial, D-type register with sum term (asynchronous) clock, or D/E-type register. Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the “D” XOR. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all “E” sum terms is selected through the “E” XOR.

When the macrocell is configured as a D/E type register, it is clocked from the common OCLK and the register clock enable input is controlled by the associated “E” sum term. This configuration is useful for building counters and state-machines with state hold functions.

When the macrocell is configured as a D-type register with a sum term clock, the register is always enabled and its “E” sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

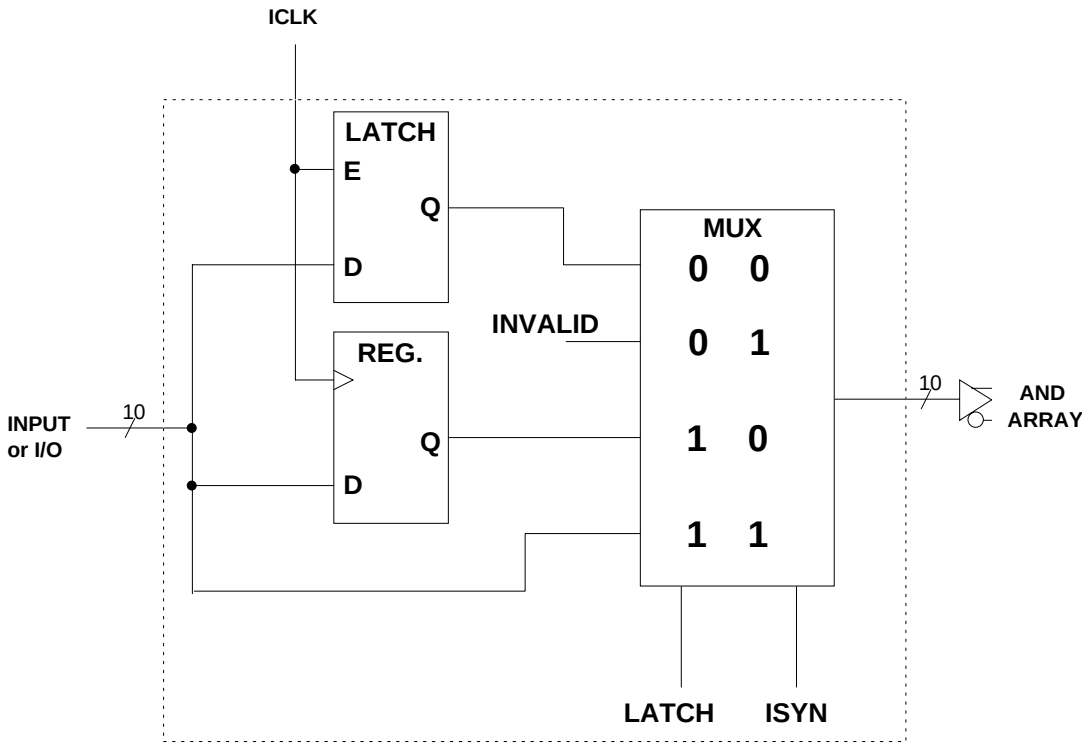
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an output pin, a logic one will occur because of the inverting output buffer.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer and always present). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried (the associated OLMC pin is an input), or dynamically buried with the use of the output enable product term.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK-, or T-register.

The three macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

ILMC and IOLMC Configurations



ILMC/IOLMC

Generic Logic Block Diagram

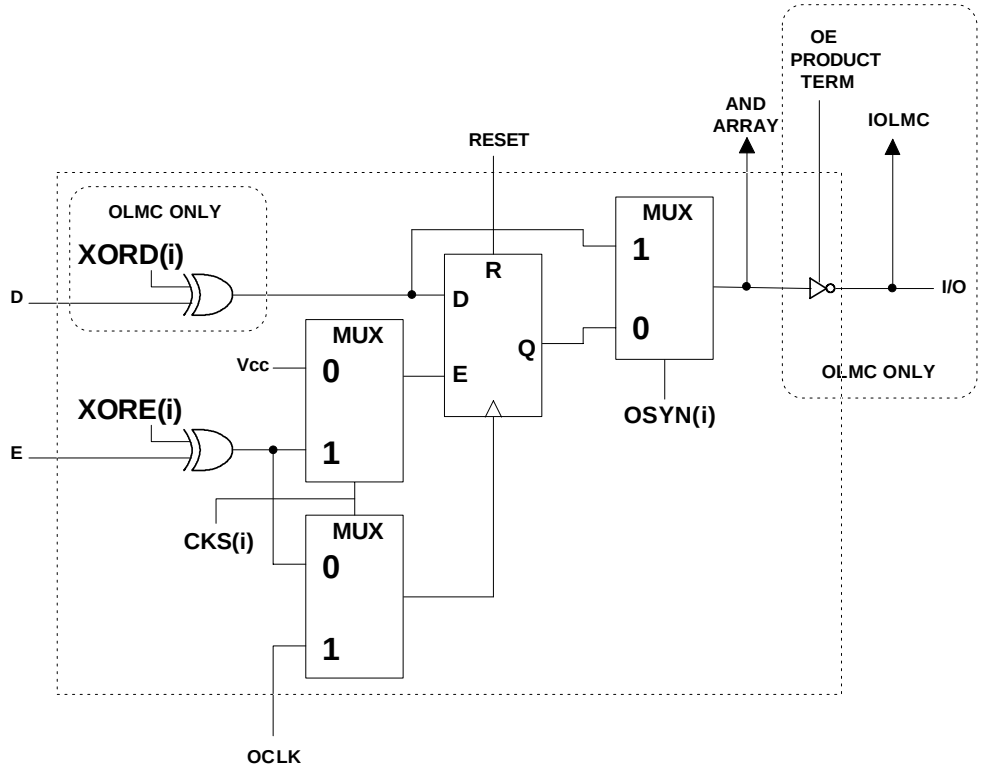
ILMC (Input Logic Macrocell)
JEDEC Fuse Numbers

ISYN	LATCH
8218	8219

IOLMC (I/O Logic Macrocell)
JEDEC Fuse Numbers

ISYN	LATCH
8220	8221

OLMC and BLMC Configurations



OLMC/BLMC

Generic Logic Block Diagram

OLMC (Output Logic Macrocell)

JEDEC Fuse Numbers

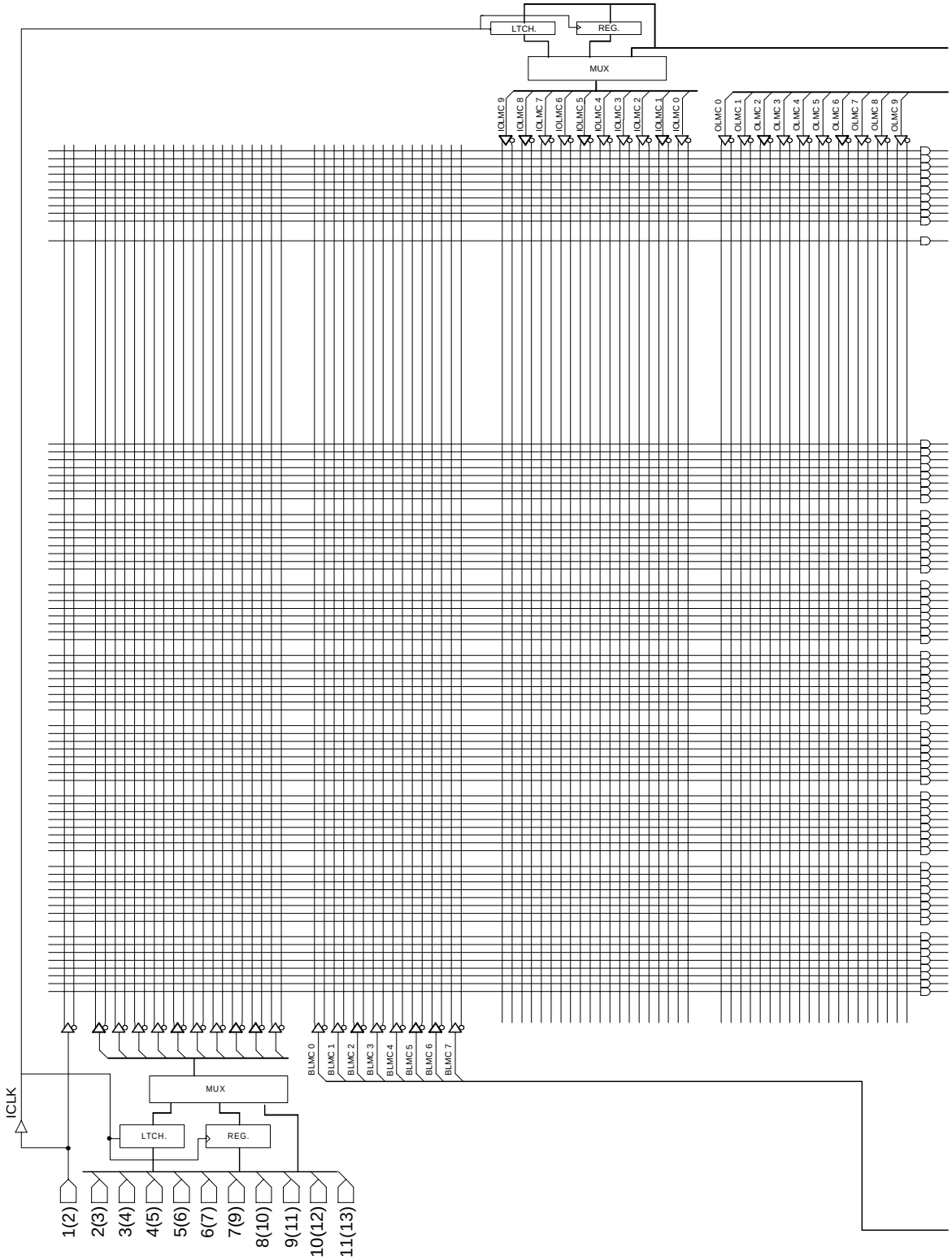
OLMC	OCLK	OSYN	XORE	XORD
0	8178	8179	8180	8181
1	8182	8183	8184	8185
2	8186	8187	8188	8189
3	8190	8191	8192	8193
4	8194	8195	8196	8197
5	8198	8199	8200	8201
6	8202	8203	8204	8205
7	8206	8207	8208	8209
8	8210	8211	8212	8213
9	8214	8215	8216	8217

BLMC (Buried Logic Macrocell)

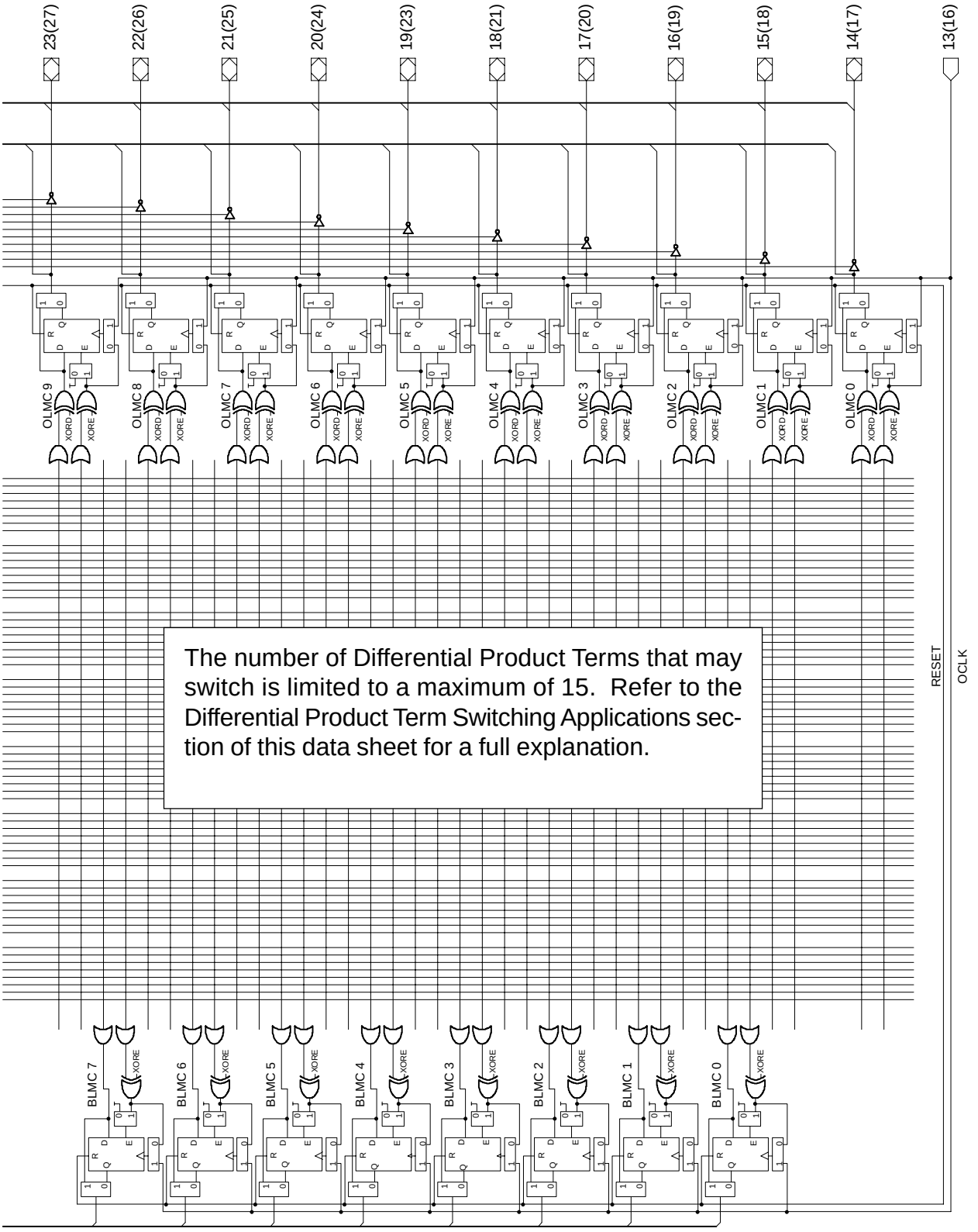
JEDEC Fuse Numbers

BLMC	OCLK	OSYN	XORE
7	8175	8176	8177
6	8172	8173	8174
5	8169	8170	8171
4	8166	8167	8168
3	8163	8164	8165
2	8160	8161	8162
1	8157	8158	8159
0	8154	8155	8156

GAL6001 Logic Diagram



GAL6001 Logic Diagram (Continued)



The number of Differential Product Terms that may switch is limited to a maximum of 15. Refer to the Differential Product Term Switching Applications section of this data sheet for a full explanation.

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V_{IH} \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–130	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -30	—	90	150	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

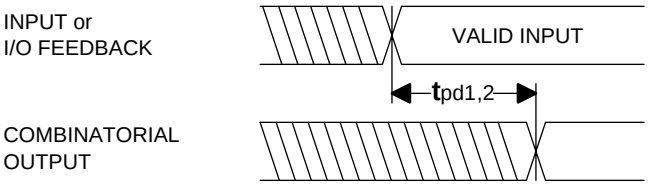
AC Switching Characteristics

Over Recommended Operating Conditions

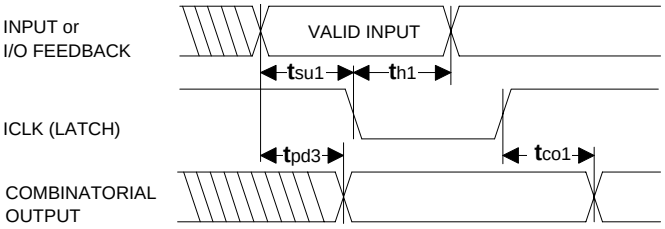
PARAMETER	TEST COND[1].	DESCRIPTION	COM -30 MIN.	COM -30 MAX.	UNITS
t_{pd1}	A	Combinatorial Input to Combinatorial Output	—	30	ns
t_{pd2}	A	Feedback or I/O to Combinatorial Output	—	30	ns
t_{pd3}	A	Transparent Latch Input to Combinatorial Output	—	35	ns
t_{co1}	A	Input Latch ICLK to Combinatorial Output Delay	—	35	ns
t_{co2}	A	Input Reg. ICLK to Combinatorial Output Delay	—	35	ns
t_{co3}	A	Output D/E Reg. OCLK to Output Delay	—	12	ns
t_{co4}	A	Output D Reg. Sum Term CLK to Output Delay	—	35	ns
t_{su1}	—	Setup Time, Input before Input Latch ICLK	2.5	—	ns
t_{su2}	—	Setup Time, Input before Input Reg. ICLK	2.5	—	ns
t_{su3}	—	Setup Time, Input or Feedback before D/E Reg. OCLK	25	—	ns
t_{su4}	—	Setup Time, Input or Feedback before D Reg. Sum Term CLK	7.5	—	ns
t_{su5}	—	Setup Time, Input Reg. ICLK before D/E Reg. OCLK	30	—	ns
t_{su6}	—	Setup Time, Input Reg. ICLK before D Reg. Sum Term CLK	15	—	ns
t_{h1}	—	Hold Time, Input after Input Latch ICLK	5	—	ns
t_{h2}	—	Hold Time, Input after Input Reg. ICLK	5	—	ns
t_{h3}	—	Hold Time, Input or Feedback after D/E Reg. OCLK	0	—	ns
t_{h4}	—	Hold Time, Input or Feedback after D Reg. Sum Term CLK	10	—	ns
f_{max}	—	Maximum Clock Frequency, OCLK	27	—	MHz
t_{wh1}	—	ICLK or OCLK Pulse Duration, High	10	—	ns
t_{wh2}	—	Sum Term CLK Pulse Duration, High	15	—	ns
t_{wl1}	—	ICLK or OCLK Pulse Duration, Low	10	—	ns
t_{wl2}	—	Sum Term CLK Pulse Duration, Low	15	—	ns
t_{arw}	—	Reset Pulse Duration	15	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	25	ns
t_{dis}	C	Input or I/O to Output Disabled	—	25	ns
t_{ar}	A	Input or I/O to Asynchronous Reg. Reset	—	35	ns
t_{arr1}	—	Asynchronous Reset to OCLK Recovery Time	20	—	ns
t_{arr2}	—	Asynchronous Reset to Sum Term CLK Recovery Time	10	—	ns

1) Refer to **Switching Test Conditions** section.

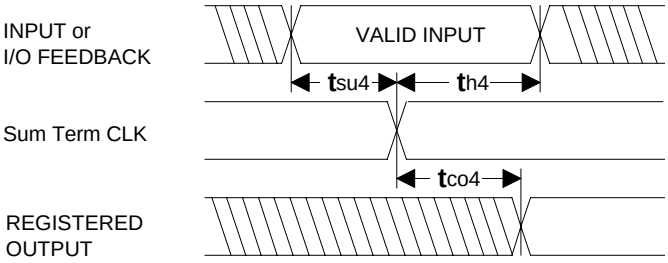
Switching Waveforms



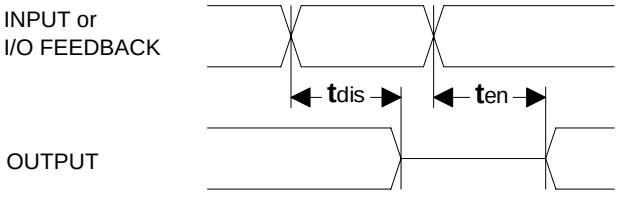
Combinatorial Output



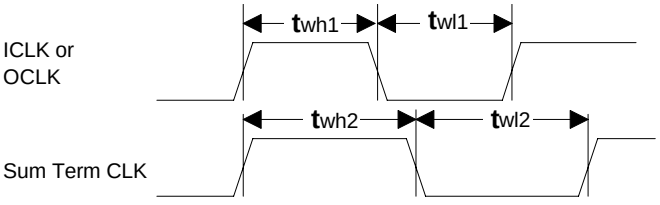
Latched Input



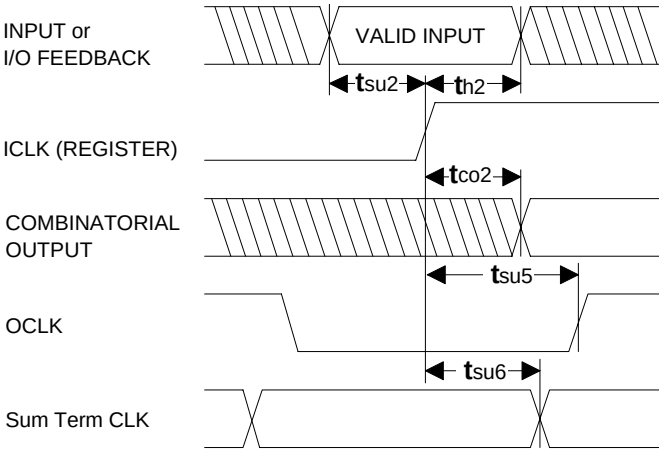
Registered Output (Sum Term CLK)



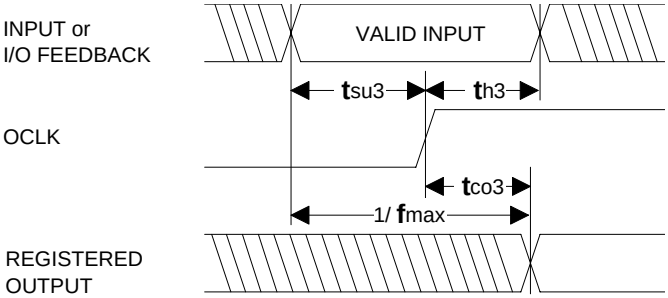
Input or I/O to Output Enable/Disable



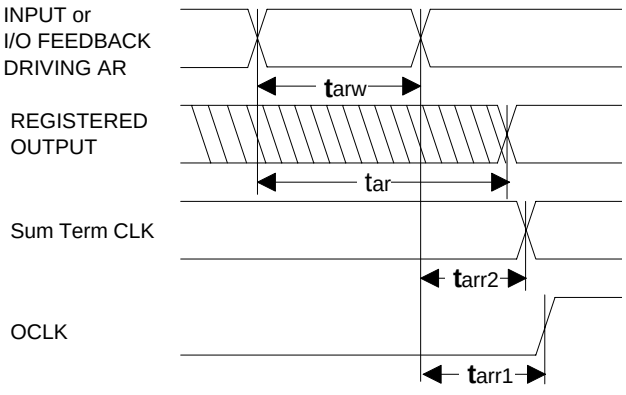
Clock Width



Registered Input

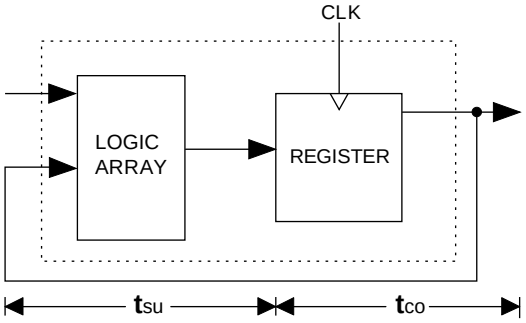


Registered Output (OCLK)



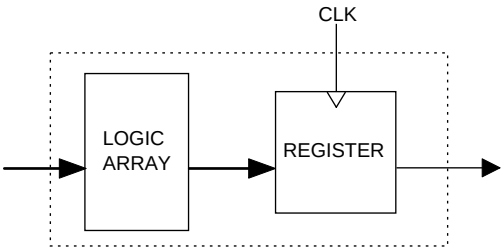
Asynchronous Reset

fmax Descriptions



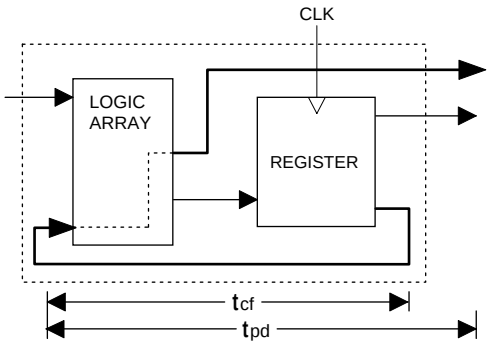
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

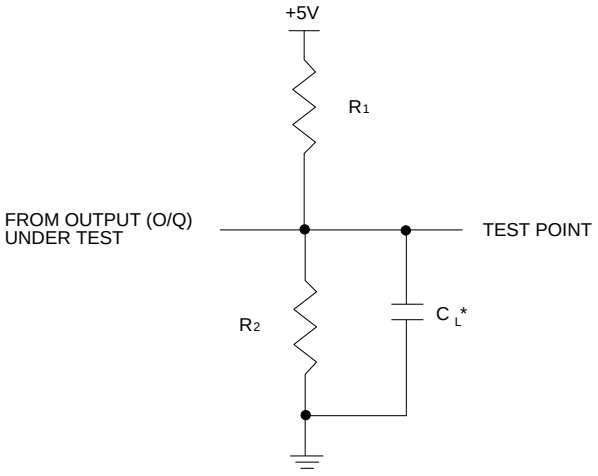
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Array Description

The GAL6001 contains two E^2 reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY
The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complement forms). 64 product terms serve as inputs to the OR array. The RESET product term generates the RESET signal described in the Output and Buried Logic Macrocells section. There are 10 output enable product terms which allow device pins 14-23 to be bi-directional or tri-state.

OR ARRAY
The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

Electronic Signature

An electronic signature (ES) is provided in every GAL6001 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

Security Cell

A security cell is provided in every GAL6001 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND and OR arrays. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Bulk Erase

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

Register Preload

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

Latch-Up Protection

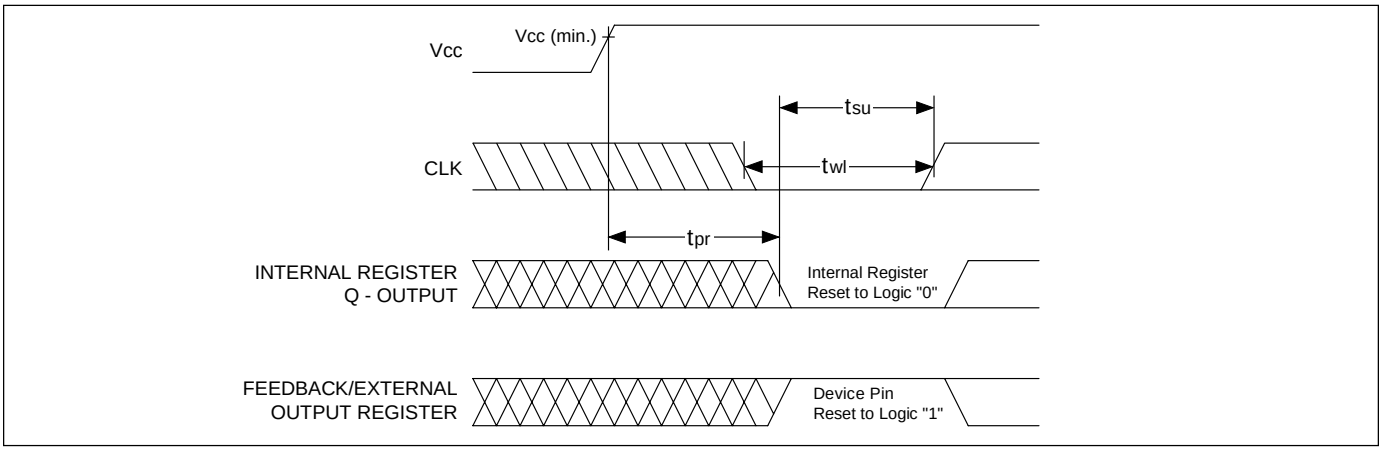
GAL6001 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

Input Buffers

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL6001 devices do not possess active pull-ups within their input structures. As a result, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Power-Up Reset



Circuitry within the GAL6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL6001. First, the VCC rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Differential Product Term Switching (DPTS) Applications

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

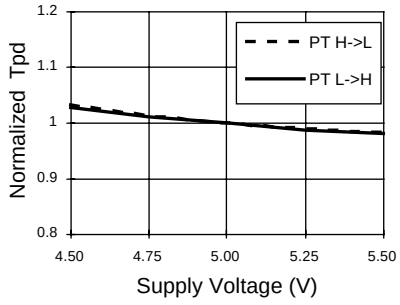
$$DPTS = \left| (P\text{-}Terms)_{LH} - (P\text{-}Terms)_{HL} \right|$$

DPTS restricts the number of product terms that can be switched simultaneously - there is no limit on the number of product terms that can be used.

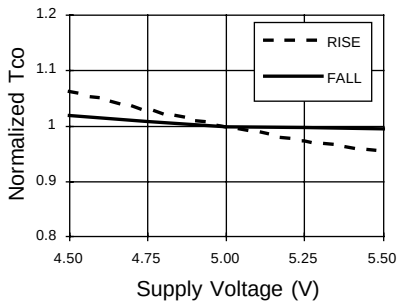
A software utility is available from Lattice Semiconductor Applications Engineering that will perform this calculation on any GAL6001 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice Semiconductor representative or by contacting Lattice Semiconductor's Applications Engineering Dept. (Tel: 503-681-0118 or 1-888-ISP-PLDS; FAX: 681-3037).

Typical AC and DC Characteristic Diagrams

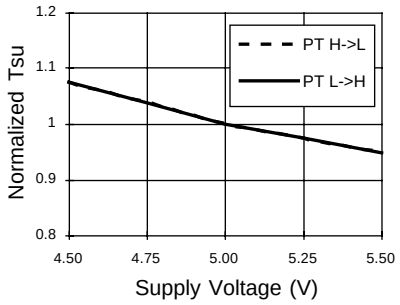
Normalized Tpd vs Vcc



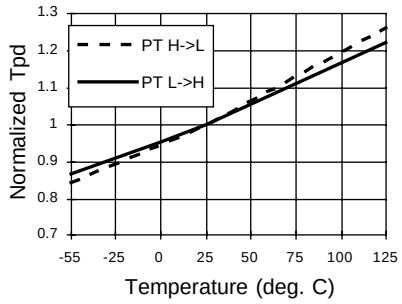
Normalized Tco vs Vcc



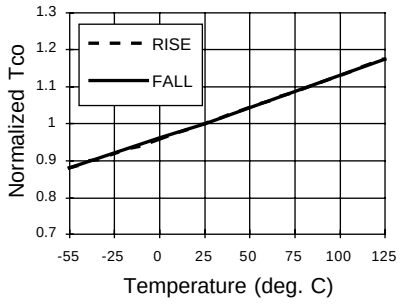
Normalized Tsu vs Vcc



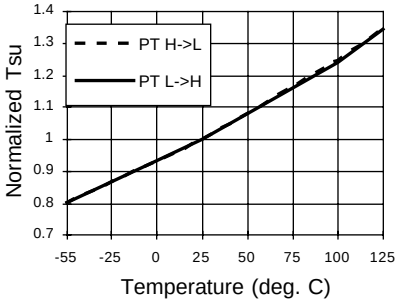
Normalized Tpd vs Temp



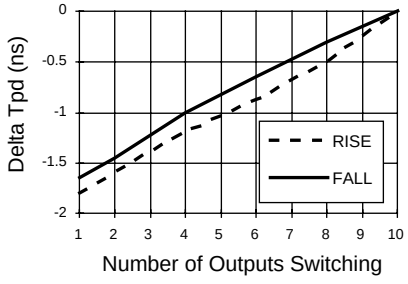
Normalized Tco vs Temp



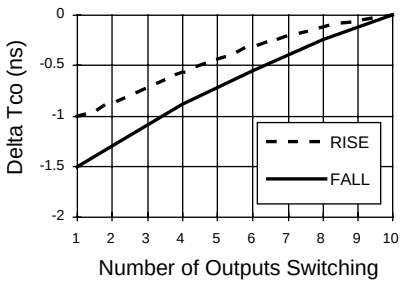
Normalized Tsu vs Temp



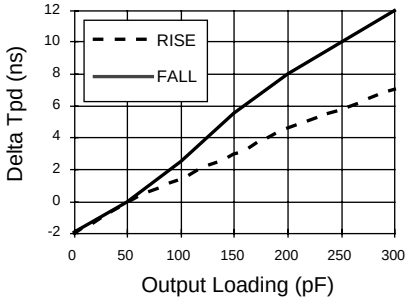
Delta Tpd vs # of Outputs Switching



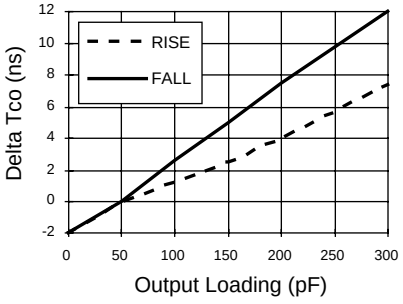
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

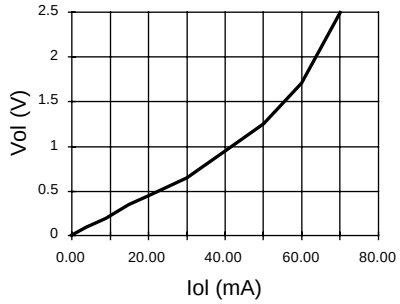


Delta Tco vs Output Loading

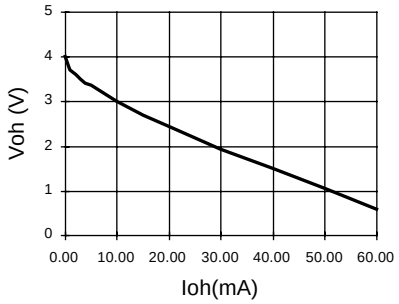


Typical AC and DC Characteristic Diagrams

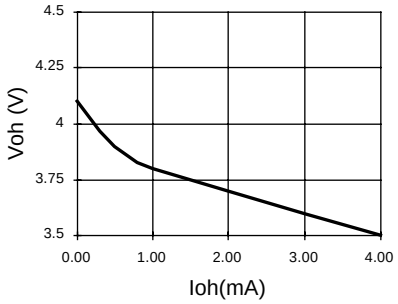
Vol vs Iol



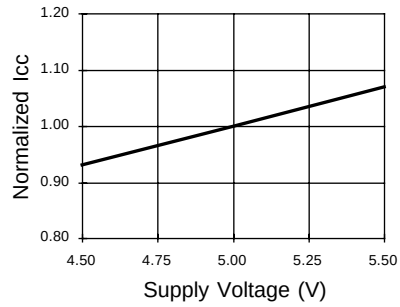
Voh vs Ioh



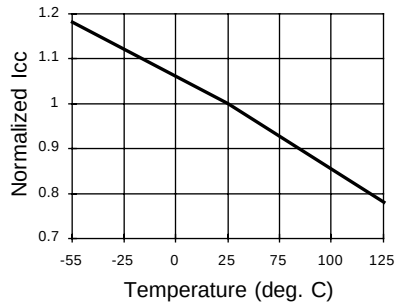
Voh vs Ioh



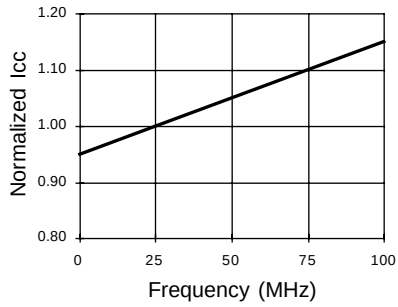
Normalized Icc vs Vcc



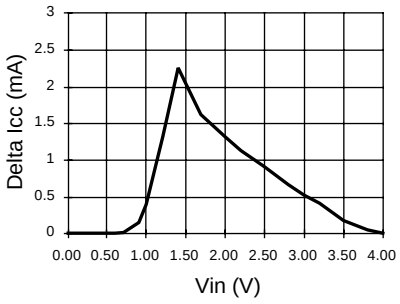
Normalized Icc vs Temp



Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)