NEC

MOS Integrated Circuit

μPD720122

USB2.0 Generic Device Controller

The μPD720122 is USB2.0 Generic Device Controller, which combines the NEC Electronics USB2.0 PHY and End-point Controller. The Controller has certified by USB Implementers Forum. End-point Controller has banked two Bulk End-point and one Interrupt End-point, and selectable three general CPU bus-types, suitable for designing various USB device. The controller has the external local bus, that enables to perform high speed data transferring when CPU is accessing to the controller. These IP Blocks in the controller are based completely on an NEC Electronics ASIC core, so μPD720122 is suitable to design for the prototype system that are intended to design ASIC in the future.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

μPD720122 User's Manual: S15829E

FEATURES

- Complaint with USB2.0 specification (Maximum data transferring rate: 480 Mbps)
- USB2.0 certified (TestID=40000822)
- High(480Mbps) / Full(12Mbps)- Speed support and switch automatically
- Easy to design NEC Electronics ASIC
- Generic USB2.0 Device Controller
- Two Bulk End-points and One Interrupt End-point
- Performed Data Local Bus independent from CPU bus.
  (Maximum Data Transferring rate: 21 MBps with DMA mode)
- Selectable three CPU Bus Interface

ORDERING INFORMATION

Part Number	Package
μPD720122GC-9EU	100-pin plastic TQFP (Fine pitch) (14 × 14)
μPD720122F1-DN2	109-pin plastic FBGA (11 × 11)

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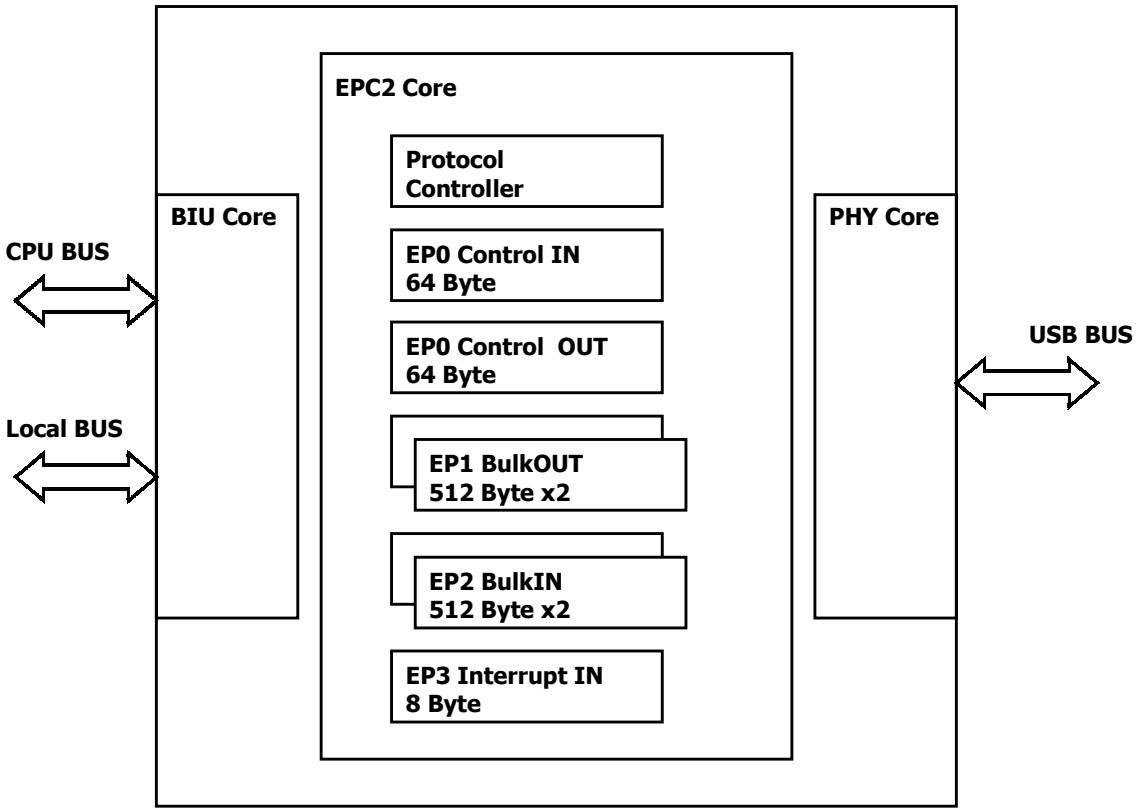
The mark ★ shows major revised points.

BLOCK DIAGRAM



PHY Core : USB2.0 transceiver with serial interface engine

EPC2 Core : Endpoint controller

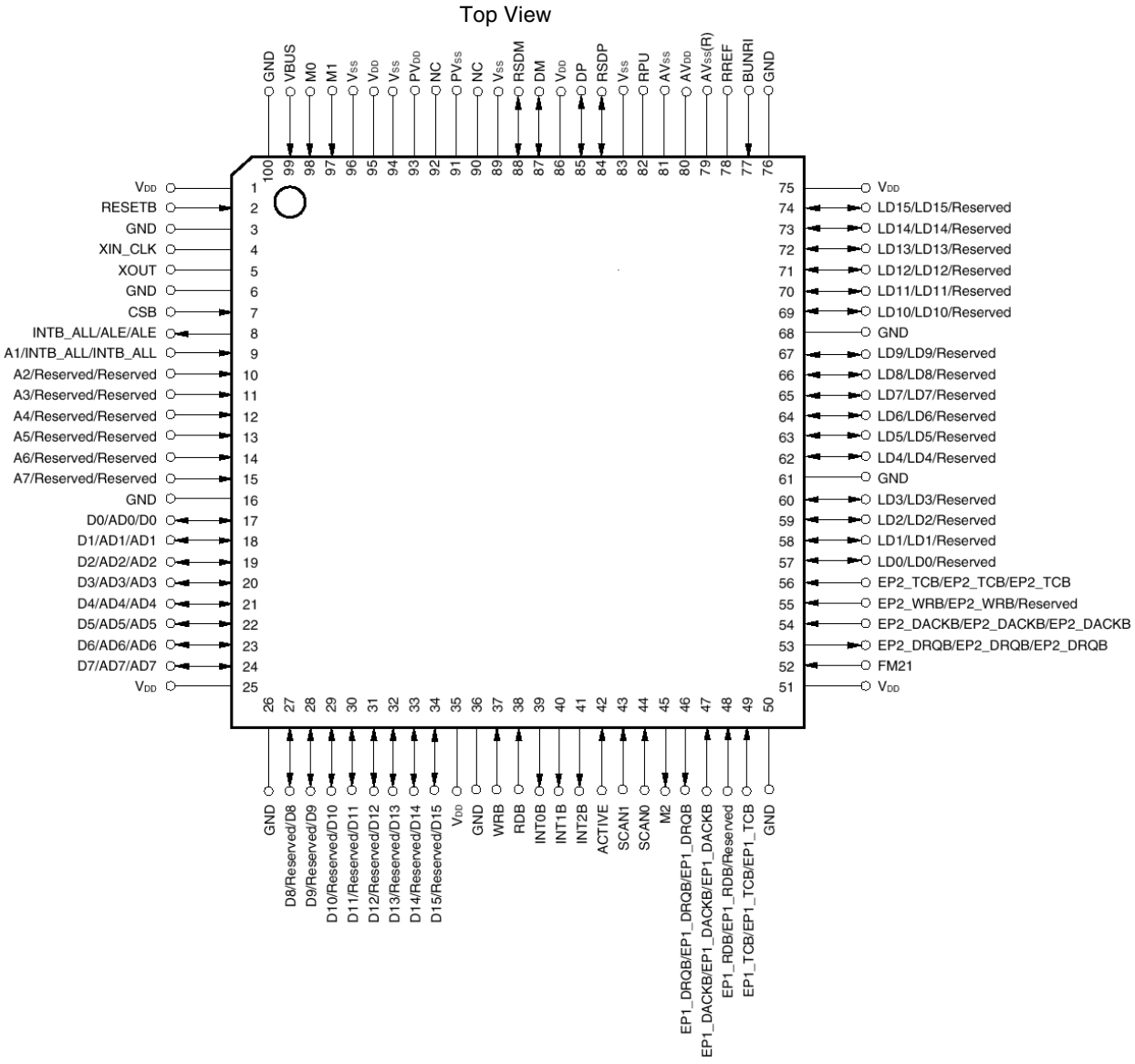
BIU Core : Bus Interface Unit

PIN CONFIGURATION

- **100-pin plastic TQFP (Fine pitch) (14 × 14)**

  μ PD720122GC-9EU

Top View



Remark The function of the pin is shown with Function 1/Function 2/Function 3 from the left.

μ PD720122GC-9EU (1/2)

Pin No.	Pin Name Function1	Pin Name Function2	Pin Name Function3	Pin No.	Pin Name Function1	Pin Name Function2	Pin Name Function3
1	V_{DD}	V_{DD}	V_{DD}	26	GND	GND	GND
2	RESETB	RESETB	RESETB	27	D8	Reserved	D8
3	GND	GND	GND	28	D9	Reserved	D9
4	XIN_CLK	XIN_CLK	XIN_CLK	29	D10	Reserved	D10
5	XOUT	XOUT	XOUT	30	D11	Reserved	D11
6	GND	GND	GND	31	D12	Reserved	D12
7	CSB	CSB	CSB	32	D13	Reserved	D13
8	INTB_ALL	ALE	ALE	33	D14	Reserved	D14
9	A1	INTB_ALL	INTB_ALL	34	D15	Reserved	D15
10	A2	Reserved	Reserved	35	V_{DD}	V_{DD}	V_{DD}
11	A3	Reserved	Reserved	36	GND	GND	GND
12	A4	Reserved	Reserved	37	WRB	WRB	WRB
13	A5	Reserved	Reserved	38	RDB	RDB	RDB
14	A6	Reserved	Reserved	39	INT0B	INT0B	INT0B
15	A7	Reserved	Reserved	40	INT1B	INT1B	INT1B
16	GND	GND	GND	41	INT2B	INT2B	INT2B
17	D0	AD0	D0	42	ACTIVE	ACTIVE	ACTIVE
18	D1	AD1	AD1	43	SCAN1	SCAN1	SCAN1
19	D2	AD2	AD2	44	SCAN0	SCAN0	SCAN0
20	D3	AD3	AD3	45	M2	M2	M2
21	D4	AD4	AD4	46	EP1_DRQB	EP1_DRQB	EP1_DRQB
22	D5	AD5	AD5	47	EP1_DACKB	EP1_DACKB	EP1_DACKB
23	D6	AD6	AD6	48	EP1_RDB	EP1_RDB	Reserved
24	D7	AD7	AD7	49	EP1_TCB	EP1_TCB	EP1_TCB
25	V_{DD}	V_{DD}	V_{DD}	50	GND	GND	GND

μ PD720122GC-9EU (2/2)

Pin No.	Pin Name Fucntion1	Pin Name Function2	Pin Name Function3	Pin No.	Pin Name Fucntion1	Pin Name Function2	Pin Name Function3
51	V_{DD}	V_{DD}	V_{DD}	76	GND	GND	GND
52	FM21	FM21	FM21	77	BUNRI	BUNRI	BUNRI
53	EP2_DRQB	EP2_DRQB	EP2_DRQB	78	RREF	RREF	RREF
54	EP2_DACKB	EP2_DACKB	EP2_DACKB	79	AV_{SS}(R)	AV_{SS}(R)	AV_{SS}(R)
55	EP2_WRB	EP2_WRB	Reserved	80	AV_{DD}	AV_{DD}	AV_{DD}
56	EP2_TCB	EP2_TCB	EP2_TCB	81	AV_{SS}	AV_{SS}	AV_{SS}
57	LD0	LD0	Reserved	82	RPU	RPU	RPU
58	LD1	LD1	Reserved	83	V_{SS}	V_{SS}	V_{SS}
59	LD2	LD2	Reserved	84	RSDP	RSDP	RSDP
60	LD3	LD3	Reserved	85	DP	DP	DP
61	GND	GND	GND	86	V_{DD}	V_{DD}	V_{DD}
62	LD4	LD4	Reserved	87	DM	DM	DM
63	LD5	LD5	Reserved	88	RSDM	RSDM	RSDM
64	LD6	LD6	Reserved	89	V_{SS}	V_{SS}	V_{SS}
65	LD7	LD7	Reserved	90	NC	NC	NC
66	LD8	LD8	Reserved	91	PV_{SS}	PV_{SS}	PV_{SS}
67	LD9	LD9	Reserved	92	NC	NC	NC
68	GND	GND	GND	93	PV_{DD}	PV_{DD}	PV_{DD}
69	LD10	LD10	Reserved	94	V_{SS}	V_{SS}	V_{SS}
70	LD11	LD11	Reserved	95	V_{DD}	V_{DD}	V_{DD}
71	LD12	LD12	Reserved	96	V_{SS}	V_{SS}	V_{SS}
72	LD13	LD13	Reserved	97	M1	M1	M1
73	LD14	LD14	Reserved	98	M0	M0	M0
74	LD15	LD15	Reserved	99	VBUS	VBUS	VBUS
75	V_{DD}	V_{DD}	V_{DD}	100	GND	GND	GND

Remark AV_{SS} (R) should be used to connect RREF through 1 % precision reference resistor of 9.1 kΩ.

- **109-pin plastic FBGA (11 × 11)**

  μPD720122F1-DN2

Bottom View

	M	L	K	J	H	G	F	E	D	C	B	A	
12	23 NC	24 BUNRI	25 AV_{SS}(R)	26 AV_{SS}	27 RSDP	28 V_{DD}	29 NC	30 NC	31 V_{DD}	32 M1	33 VBUS	34 NC	12
11	22 LD15	63 NC	64 RREF	65 AV_{DD}	66 GND	67 RSDM	68 PV_{SS}	69 GND	70 GND	71 M0	72 NC	35 RESETB	11
10	21 LD13	62 LD14	95 GND	96 RPU	97 DP	98 GND	99 DM	100 PV_{DD}	101 V_{DD}	102 GND	73 GND	36 XIN_CLK	10
9	20 LD11	61 LD12	94 V_{DD}							103 CSB	74 XOUT	37 GND	9
8	19 LD9	60 LD10	93 GND							104 A2	75 INTB_ALL	38 A1	8
7	18 LD7	59 LD8	92 LD4							105 A6	76 A5	39 A3	7
6	17 GND	58 LD5	91 LD6							106 A4	77 GND	40 A7	6
5	16 LD2	57 LD1	90 LD3							107 D1	78 D2	41 D0	5
4	15 EP2_TCB	56 EP2_WRB	89 LD0						109 GND	108 V_{DD}	79 D4	42 D3	4
3	14 EP2_DACKB	55 EP2_DRQB	88 GND	87 V_{DD}	86 SCAN1	85 WRB	84 INT0B	83 V_{DD}	82 D13	81 GND	80 D6	43 D5	3
2	13 FM21	54 NC	53 EP1_RDB	52 EP1_DRQB	51 SCAN0	50 INT2B	49 RDB	48 D14	47 D11	46 D9	45 NC	44 D7	2
1	12 NC	11 EP1_TCB	10 EP1_DACKB	9 M2	8 ACTIVE	7 INT1B	6 GND	5 D15	4 D12	3 D10	2 D8	1 NC	1

Remarks The pin name is showing it with Function1.

As for the pin name of Function2 and Function3, please refer to the table of the next page.

μ PD720122F1-DN2 (1/2)

Pin No.	Pin Name Function1	Pin Name Function2	Pin Name Function3	Pin No.	Pin Name Function1	Pin Name Function2	Pin Name Function3
1	NC	NC	NC	26	AV_{SS}	AV_{SS}	AV_{SS}
2	D8	Reserved	D8	27	RSDP	RSDP	RSDP
3	D10	Reserved	D10	28	V_{DD}	V_{DD}	V_{DD}
4	D12	Reserved	D12	29	NC	NC	NC
5	D15	Reserved	D15	30	NC	NC	NC
6	GND	GND	GND	31	V_{DD}	V_{DD}	V_{DD}
7	INT1B	INT1B	INT1B	32	M1	M1	M1
8	ACTIVE	ACTIVE	ACTIVE	33	VBUS	VBUS	VBUS
9	M2	M2	M2	34	NC	NC	NC
10	EP1_DACKB	EP1_DACKB	EP1_DACKB	35	RESETB	RESETB	RESETB
11	EP1_TCB	EP1_TCB	EP1_TCB	36	XIN_CLK	XIN_CLK	XIN_CLK
12	NC	NC	NC	37	GND	GND	GND
13	FM21	FM21	FM21	38	A1	INTB_ALL	INTB_ALL
14	EP2_DACKB	EP2_DACKB	EP2_DACKB	39	A3	Reserved	Reserved
15	EP2_TCB	EP2_TCB	EP2_TCB	40	A7	Reserved	Reserved
16	LD2	LD2	Reserved	41	D0	AD0	D0
17	GND	GND	GND	42	D3	AD3	AD3
18	LD7	LD7	Reserved	43	D5	AD5	AD5
19	LD9	LD9	Reserved	44	D7	AD7	AD7
20	LD11	LD11	Reserved	45	NC	NC	NC
21	LD13	LD13	Reserved	46	D9	Reserved	D9
22	LD15	LD15	Reserved	47	D11	Reserved	D11
23	NC	NC	NC	48	D14	Reserved	D14
24	BUNRI	BUNRI	BUNRI	49	RDB	RDB	RDB
25	AV_{SS}(R)	AV_{SS}(R)	AV_{SS}(R)	50	INT2B	INT2B	INT2B

Remark AVSS (R) should be used to connect RREF through 1 % precision reference resistor of 9.1 kΩ.

μ PD720122F1-DN2 (2/2)

Pin No.	Pin Name Function1	Pin Name Function2	Pin Name Function3	Pin No.	Pin Name Function1	Pin Name Function2	Pin Name Function3
51	SCAN0	SCAN0	SCAN0	81	GND	GND	GND
52	EP1_DRQB	EP1_DRQB	EP1_DRQB	82	D13	Reserved	D13
53	EP1_RDB	EP1_RDB	Reserved	83	V_{DD}	V_{DD}	V_{DD}
54	NC	NC	NC	84	INT0B	INT0B	INT0B
55	EP2_DRQB	EP2_DRQB	EP2_DRQB	85	WRB	WRB	WRB
56	EP2_WRB	EP2_WRB	Reserved	86	SCAN1	SCAN1	SCAN1
57	LD1	LD1	Reserved	87	V_{DD}	V_{DD}	V_{DD}
58	LD5	LD5	Reserved	88	GND	GND	GND
59	LD8	LD8	Reserved	89	LD0	LD0	Reserved
60	LD10	LD10	Reserved	90	LD3	LD3	Reserved
61	LD12	LD12	Reserved	91	LD6	LD6	Reserved
62	LD14	LD14	Reserved	92	LD4	LD4	Reserved
63	NC	NC	NC	93	GND	GND	GND
64	RREF	RREF	RREF	94	V_{DD}	V_{DD}	V_{DD}
65	AV_{DD}	AV_{DD}	AV_{DD}	95	GND	GND	GND
66	GND	GND	GND	96	RPU	RPU	RPU
67	RSDM	RSDM	RSDM	97	DP	DP	DP
68	PV_{SS}	PV_{SS}	PV_{SS}	98	GND	GND	GND
69	GND	GND	GND	99	DM	DM	DM
70	GND	GND	GND	100	PV_{DD}	PV_{DD}	PV_{DD}
71	M0	M0	M0	101	V_{DD}	V_{DD}	V_{DD}
72	NC	NC	NC	102	GND	GND	GND
73	GND	GND	GND	103	CSB	CSB	CSB
74	XOUT	XOUT	XOUT	104	A2	Reserved	Reserved
75	INTB_ALL	ALE	ALE	105	A6	Reserved	Reserved
76	A5	Reserved	Reserved	106	A4	Reserved	Reserved
77	GND	GND	GND	107	D1	AD1	AD1
78	D2	AD2	AD2	108	V_{DD}	V_{DD}	V_{DD}
79	D4	AD4	AD4	109	GND	GND	GND
80	D6	AD6	AD6	-	-	-	-

1. PIN INFORMATION

(1/2)

Pin Name	I/O	Buffer Type	Active Level	Function
RESETB	I	5 V tolerant Input Schmitt	Low	Asynchronous reset signaling
XIN_CLK	I	3.3 V Input		System clock input or oscillator In
XOUT	O	3.3 V Output		Oscillator out
CSB	I	5 V tolerant Input	Low	Chip select signal
INTB_ALL	O	5 V tolerant Output	Low	Interrupt request signal
ALE	I	5 V tolerant Input	High	Address strobe signal (Function2/3)
A(7:1)	I	5 V tolerant Input		Address input (Function1)
D(15:0)	I/O	5 V tolerant I/O		Data bus (I/O) (Function1)
AD(7:0)	I/O	5 V tolerant I/O		Address/data multiplexed bus (I/O) (Function2)
D0	I/O	5 V tolerant I/O		Data bus (I/O) (Function3)
AD(7:1)	I/O	5 V tolerant I/O		Address/data multiplexed bus (I/O) (Function3)
D(15:8)	I/O	5 V tolerant I/O		Data bus (I/O) (Function3)
WRB	I	5 V tolerant Input	Low	Write command input
RDB	I	5 V tolerant Input	Low	Read command input
INT0B	O	5 V tolerant Output	Low	Interrupt request (INT Status 0)
INT1B	O	5 V tolerant Output	Low	Interrupt request (INT Status 1)
INT2B	O	5 V tolerant Output	Low	Interrupt request (INT Status 2)
ACTIVE	I	5 V tolerant Input		DMA-related pins active level select(Function2/3)
SCAN(1:0)	I	3.3 V Input 50 kΩ Pull Down		Chip test pin.
M2	O	5 V tolerant Output		Status output pin
EP1_DRQB	O	5 V tolerant Output	Low	DMA transfer request output pin of EP1
EP1_DACKB	I	5 V tolerant Input	Low	DMA transfer enable input pin of EP1
EP1_RDB	I	5 V tolerant Input	Low	DMA Read command input pin of EP1
EP1_TCB	I	5 V tolerant Input	Low	DMA terminal count input pin of EP1
FM21	I	3.3 V Input		NEC Electronics test pin
EP2_DRQB	O	5 V tolerant Output	Low	DMA transfer request output pin of EP2
EP2_DACKB	I	5 V tolerant Input	Low	DMA transfer enable input pin of EP2
EP2_WRB	I	5 V tolerant Input	Low	DMA Write command input pin of EP2
EP2_TCB	I	5 V tolerant Input	Low	DMA terminal count input pin of EP2
LD(15:0)	I/O	5 V tolerant I/O		Data bus (I/O) pin for external local bus
BUNRI	I	5V torelant Input		NEC Electronics test pin
RREF	A	Analog		Reference resistor
RPU	A	USB pull-up control		USB's 1.5 kΩ pull-up resistor control
RSDP	O	USB full speed D+ O		USB's full speed D+ signal
DP	I/O	USB high speed D+ I/O		USB's high speed D+ signal
DM	I/O	USB high speed D- I/O		USB's high speed D– signal

(2/2)

Pin Name	I/O	Buffer Type	Active Level	Function
RSDM	O	USB full speed D- O		USB's full speed D– signal
M(1:0)	I	5 V tolerant Input		Function mode setting
VBUS	I	5 V tolerant Input Note		VBUS monitoring
AV_{DD}, PV_{DD}				3.3 V_{DD} for Analog circuit
V_{DD}				3.3 V_{DD}
AV_{SS}, PV_{SS}				V_{SS} for Analog circuit
V_{SS}, GND				V_{SS}
NC				Not connect
Reserved				Not used

Note VBUS pin may be used to monitor for VBUS line even if V_{DD}, AV_{DD}, and PV_{DD} are shut off. System must ensure that the input voltage level for VBUS pin is less than 3.0 V due to the absolute maximum rating is not exceeded.

Remark "5 V tolerant" means that the buffer is 3.3 V buffer with 5 V tolerant circuit.

The operation mode of the BIU can be set by external pins, as shown below. Fix external pins (M1 and M0) when using them.

Pin		BIU Operation Mode	Outline
M1	M0		
0	0	16-bit mode (Function 1)	A 16-bit CPU bus and an external local bus dedicated to data transfer for bulk IN/OUT can be used in this mode. The internal register length is 16 bits.
0	1	8-bit mode (Function 2)	Multiplexed bus mode of 8-bit address bus and 8-bit data bus. The register length is 8 bits only in this mode (registers can only be accessed in byte units). Therefore, the address space in this mode differs from that in the other modes. The active levels of some external local bus control pins can be changed by the Active pin.
1	0	16-bit mix mode (Function 3)	Multiplexed bus mode of 8-bit address bus and 16-bit data bus. The internal register length is 16 bits. The active levels of some external local bus control pins can be changed by the Active pin.
1	1	Setting prohibited (Function 4)	Setting prohibited

2. ELECTRICAL SPECIFICATIONS

2.1 Buffer List

- 3.3 V oscillator interface

  XIN,XOUT

- 3.3 V input buffer

  FM21,SCAN(1:0)

- 5V torelant input buffer

  RESETB,CSB,A(7:0),WRB,RDB,ACTIVE,EP1_DACKB,EP1_RDB,EP1_TCB,EP2_DACKB,EP2_WRB,
  EP2_TCB,BUNRI,M0,M1,VBUS,ALE

- 5V torelant output buffer

  INTB_ALL,INT0B,INT1B,INT2B,M2,EP1_DRQB,EP2_DRQB

- 5V torelant I/O buffer

  D(15:0),LD(15:0),AD(7:0),D0,AD(7:1),D(15:8)

- USB interface

  DP,DM,RSDP,RSDM,RREF,RPU

2.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance value for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “Max.” value is applied, the input voltage is guaranteed as low level voltage.
Hysteresys voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_{ri}	Indicates allowable input rise time to input pins. Input rise time is transition time from $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$.
Input fall time	t_{fi}	Indicates allowable input fall time to input pins. Input fall time is transition time from $0.9 \times V_{DD}$ to $0.1 \times V_{DD}$.

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

2.3 Absolute Maximum Ratings

Parameter		Symbol	Conditions	Ratings	Unit
Voltage		V_{DD}		–0.5 to +4.6	V
I/O voltage		V_I/V_O			
	Note 1		$V_I/V_O < V_{DD}$+3.0 V	–0.5 to +6.6	V
	Note 2		$V_I/V_O < V_{DD}$+0.3 V	–0.5 to +4.6	V
Output current		I_O			
	Note 3		I_{OL} = 6 mA	6	mA
Operating ambient temperature		T_A		0 to +70	°C
Storage temperature		T_{stg}		–65 to +150	°C

Notes 1. 5 V torelant input buffer, output buffer, I/O buffer

2. 3.3 V input buffer,3.3 V oscillator interface

3. 5 V torelant output buffer, I/O buffer(OUT)

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2.4 Recommended Operating Range

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.3 V Power	3.0	3.3	3.6	V
Negative trigger voltage	V_N		0.6		1.8	V
Positive trigger voltage	V_P		1.2		2.4	V
Hysteresis voltage	V_H		0.3		1.5	V
Input voltage, low	V_{IL}		0		0.8	V
Input voltage, high	V_{IH}	3.3 V input buffer	2.0		V_{DD}	V
		5V torelant input buffer, I/O buffer	2.0		5.5	V
Rise/fall time	t_r/t_f		0		200	ns

2.5 DC Characteristics

The DC characteristics are classified into those of the USB interface and those of the BIU block.

2.5.1 DC characteristics of USB interface

Parameter	Symbol	Conditions	Min.	Max.	Unit
Serial resistor between DP (DM) and RSDP (RSDM)	R_S		35.64	36.36	Ω
Driver output resistance (also serves as high-speed termination)	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Bus pull-up resistor on upstream facing port	R_{PU}		1.425	1.575	Ω
Termination voltage for upstream facing port pull-up (full-speed)	V_{TERM}		3.0	3.6	V
Input levels for full-speed:					
High-level input voltage (driven)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	| (D+) – (D–) |	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output levels for full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to V_{SS}	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover voltage	V_{CRS}		1.3	2.0	V
Input levels for high-speed:					
High-speed squelch detection threshold (differential signal amplitude)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal amplitude)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range (guideline for receiver)	V_{HSCM}		–50	500	mV
High-speed differential input signaling level	See Figure 2-4				
Output levels for high-speed:					
High-speed idle level	V_{HSOI}		–10.0	10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		–10.0	10	mV
Chirp J level (different voltage)	V_{CHIRPJ}		700	1100	mV
Chirp K level (different voltage)	V_{CHIRPK}		–900	–500	mV

Figure 2-1. Differential Input Sensitivity Range for Low-/Full-Speed

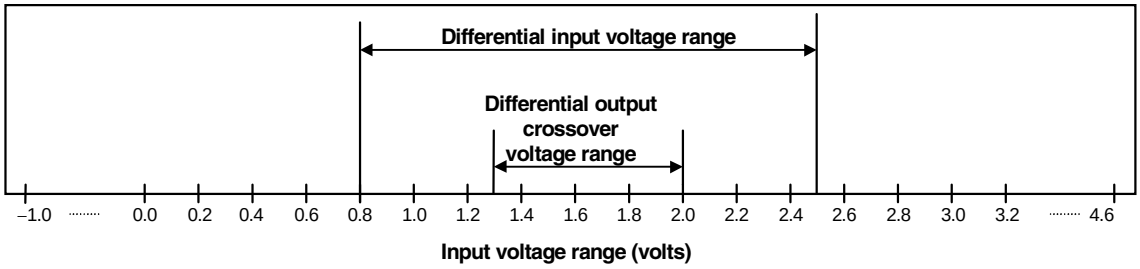


Figure 2-2. Full-Speed Buffer Voh/Ioh Characteristics for High-Speed Capable Transceiver

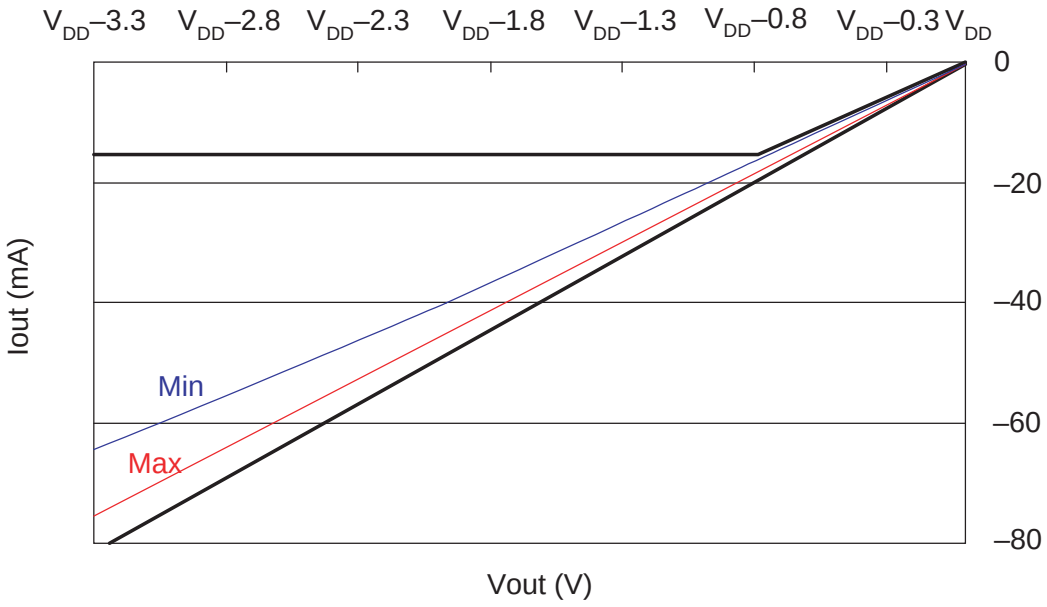


Figure 2-3. Full-Speed Buffer Vol/Iol Characteristics for High-Speed Capable Transceiver

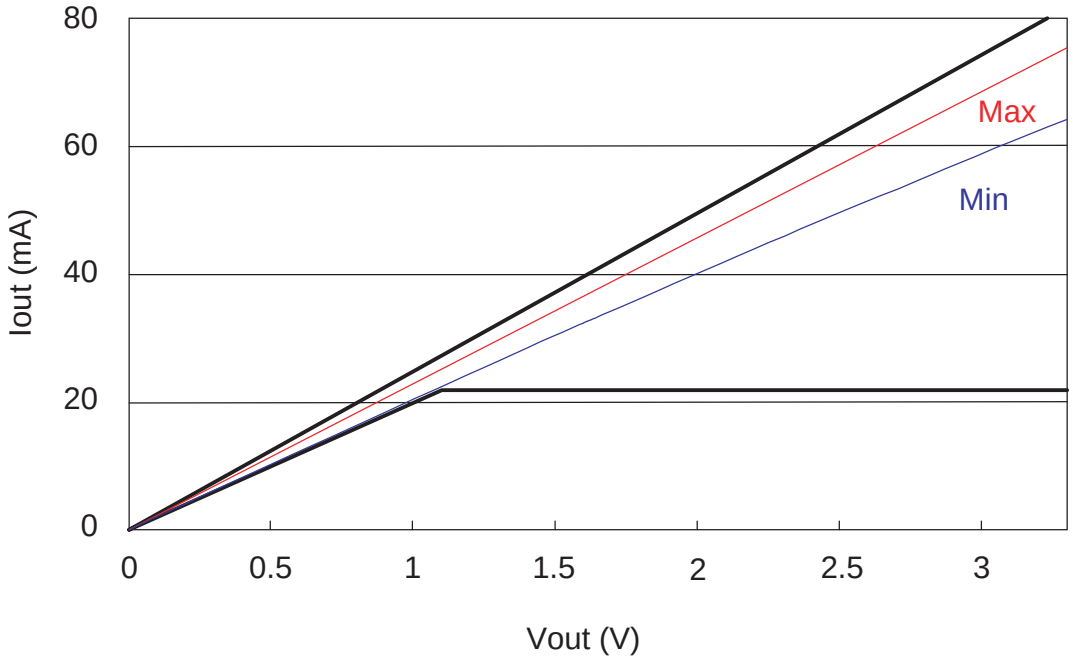


Figure 2-4. Receiver Sensitivity for Transceiver at D+/D–

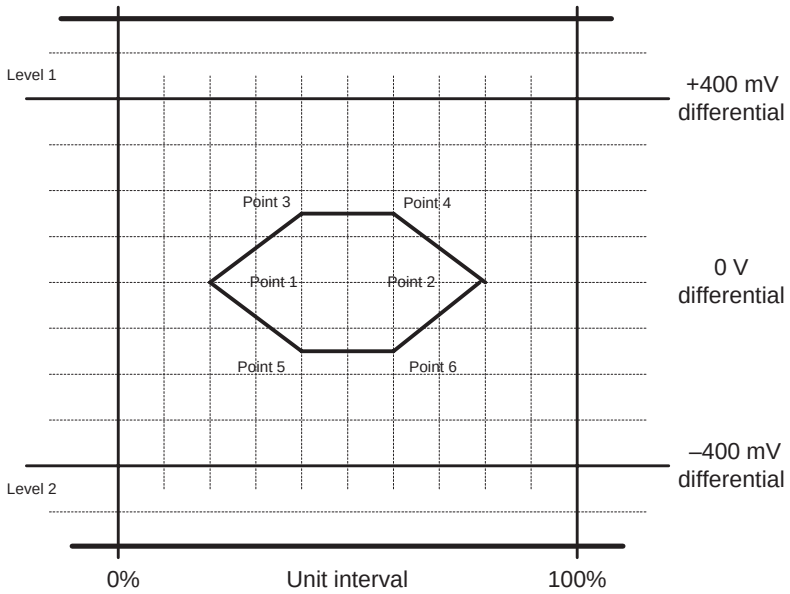
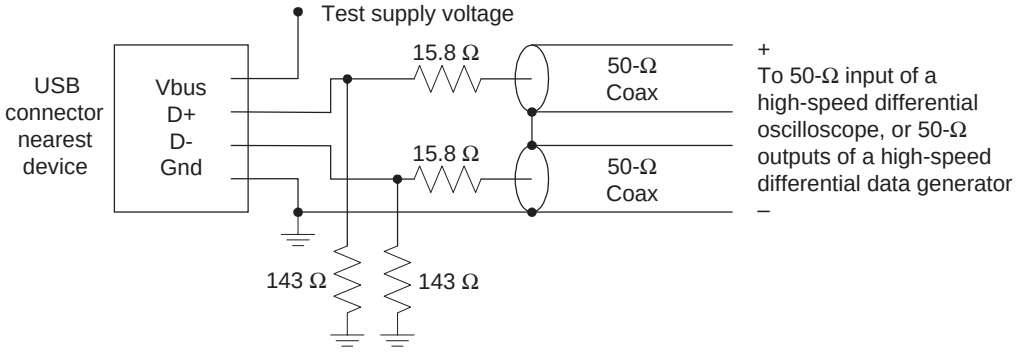


Figure 2-5. Receiver Measurement Fixtures



2.5.2 DC characteristics of BIU

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or GND			±10	μA
Output short current	I_{OS}				–250	mA
Input leakage current	I_I	$V_I = V_{DD}$ or GND		$±10^{-5}$		μA
Output current, low	I_{OL}	V_{OL} = 0.4 V[Note]	6			mA
Output current, high	I_{OH}	V_{OH} = 2.4 V	–2			mA
Output voltage, low	V_{OL}	I_{OL} = 0 mA			0.1	V
Output voltage, high	V_{OH}	I_{OH} = 0 mA	V_{DD}–0.2			V

Note 5V-Tolerant Output

2.5.3 Pin capacitance

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}		4.5		6.5	pF
Output/bidirectional capacitance	C_{OUT}		8.5		11	pF

Remark These are just estimated values.

2.5.4 Power consumption

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Power consumption	P_H	HS mode	V_{DD}		195	273	mA
			AV_{DD}		12	17	mA
	P_F	FS mode	V_{DD}		120	168	mA
			AV_{DD}		12	17	mA
	P_{S1}	Suspend mode 1[Note 1]	V_{DD}		1.5	2.2	mA
			AV_{DD}		0.1	0.2	μA
	P_{S2}	Suspend mode 2[Note 2]	V_{DD}		370	520	μA
			AV_{DD}		0.1	0.2	μA

Notes 1. SND PHY Reg. SPND bit = 1

2. SND PHY Reg. SPND bit = 1
GPR Reg. CONNECTB bit = 0
GPR Reg. PUE bit = 0
BIU Control 0 Reg. OSC_DISCONB bit = 1

2.6 AC Characteristics (T_A = 0 to +70°C, V_{DD} = 3.3 V ±10%)

The AC characteristics are classified into those of the USB interface block and those of the BIU.

2.6.1 Overall AC characteristics and those of BIU

(1) Clock

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_{CLK}	X'tal	-500ppm	30	+500ppm	MHz
		Oscillator block	-500ppm	30	+500ppm	MHz
Clock Duty cycle	T_{DUTY}		40	50	60	%

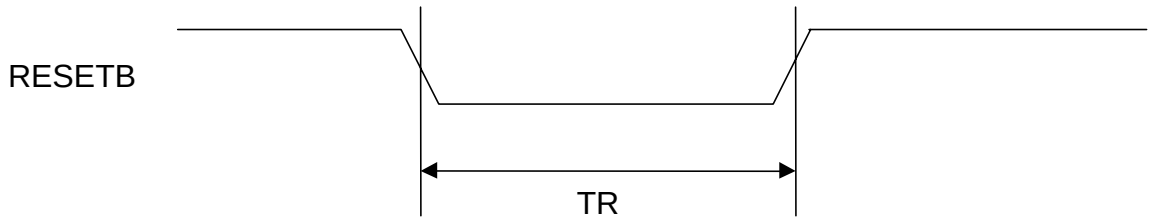
Remarks 1. Reccomended accurarcy of clock frequency is ±100ppm.

2. Required accurarcy of X'tal or Oscillator block is includeing initial frequency accuracy, the spread of X'tal capacityor loading, supply voltage, temperature, and aging etc.

(2) Reset

Symbol	Specification	Min.	Typ.	Max.	Unit
TR	Reset width	2			μs

HW reset timing



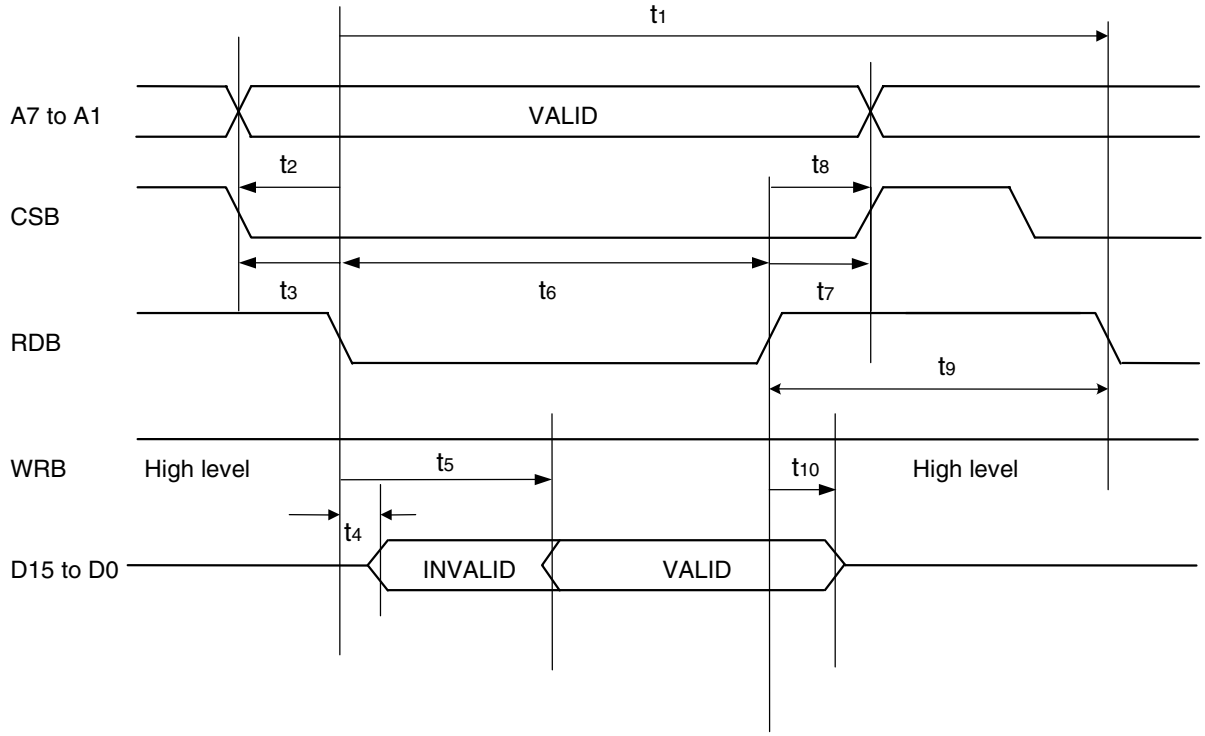
2.6.2 AC characteristics of BIU block with Function 1 selected

(1) CPU BUS read operation

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	Read cycle time	91		∞	ns
T2	Address setup time (RDB↓)	5		∞	ns
T3	Chip select setup time (RDB↓)	5		∞	ns
T4	Buffer direction change time (RDB↓)	–		14	ns
T5	Output data delay time (RDB↓)	–		57	ns
T6	Read command width	57		∞	ns
T7	Chip select hold time (RDB↑)	5		∞	ns
T8	Address hold time (RDB↑)	5		∞	ns
T9	RDB inactive time	34		∞	ns
T10	Output data hold time (RDB↑)	4		–	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

CPU bus read timing

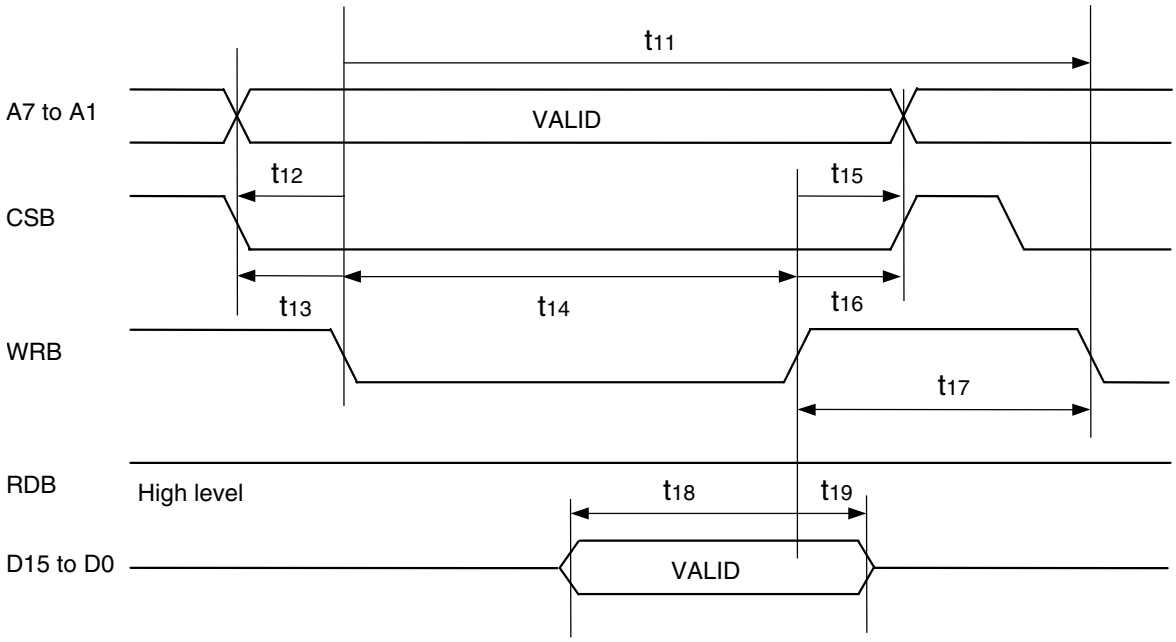


(2) CPU bus write operation

Symbol	Parameter	Min.	Typ.	Max.	Unit
T11	Write cycle time	68		∞	ns
T12	Address setup time (WRB↓)	5		∞	ns
T13	Chip select setup time (WRB↓)	5		∞	ns
T14	Write command width	34		∞	ns
T15	Address hold time (WRB↑)	5		∞	ns
T16	Chip select hold time (WRB↑)	5		∞	ns
T17	WRB inactive time	34		∞	ns
T18	Input data setup time	10		∞	ns
T19	Input data hold time	0		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

CPU bus write timing

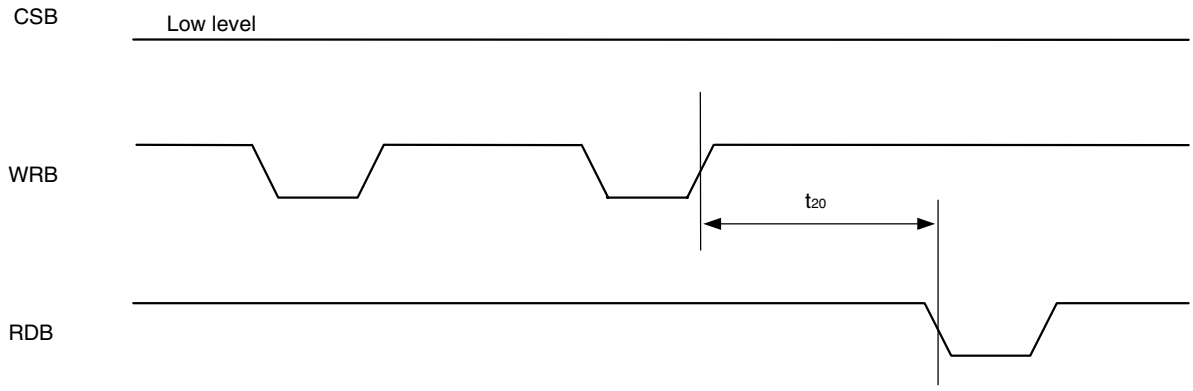


(3) CPU BUS RDB vs. WRB timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T20	WRB vs. RDB inactive time	34		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

CPU bus read vs. write change timing



(4) CPU bus DMA transfer

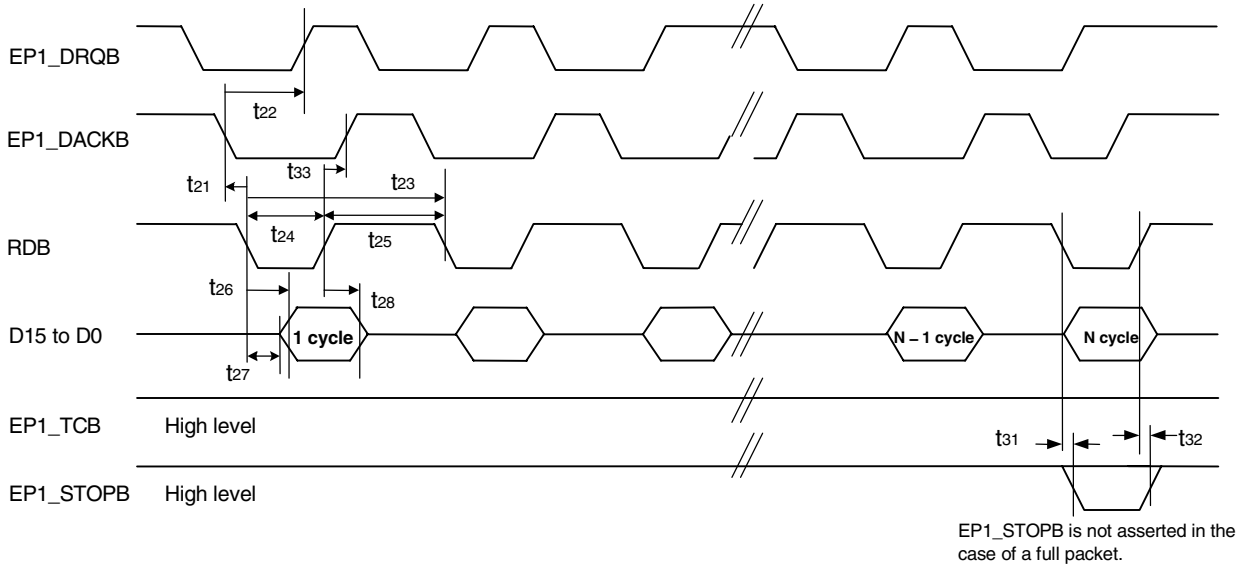
(a) CPU bus DMA single mode read transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T21	DMA request acknowledge setup time (RDB↓)	0		∞	ns
T22	DMA request off time (EP1_DACKB↓)	–		54	ns
T23	DMA single mode read transfer cycle time	91		∞	ns
T24	Read command width	57		∞	ns
T25	Read command inactive time	34		∞	ns
T26	Read data delay time (RDB↓)	–		57	ns
T27	Buffer direction change time (RDB↓)	–		14	ns
T28	Read data hold time (RDB↑)	4		–	ns
T29	EP1_TCB setup time (RDB↓)	0		**Note**	ns
T30	EP1_TCB hold time (RDB↓)	17		∞	ns
T31	EP1_STOPB delay time (RDB↓)	–		15	ns
T32	EP1_STOPB OFF delay time (RDB↑)	3		–	ns
T33	DMA request acknowledge hold time (RDB↑)	0		∞	ns
T34	Undefined	–		–	ns

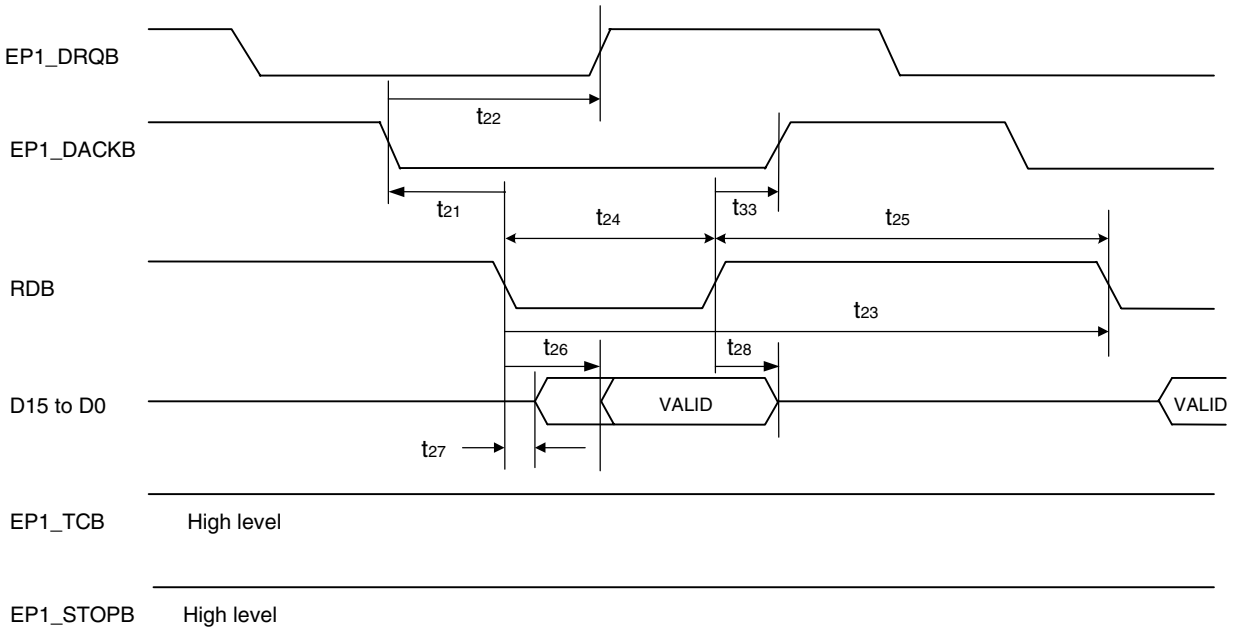
Note Can be input after previous RDB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

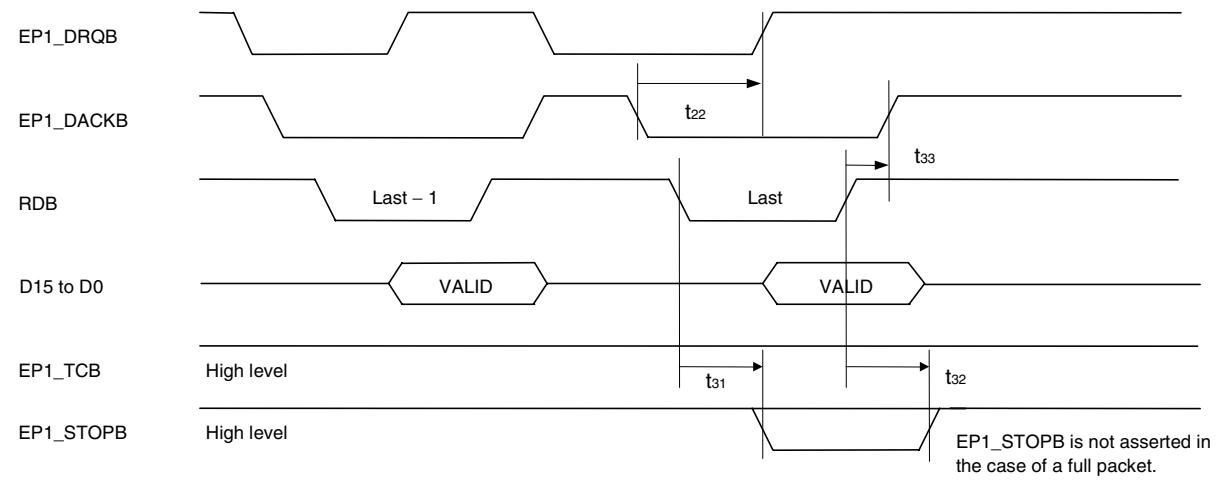
(Overall)



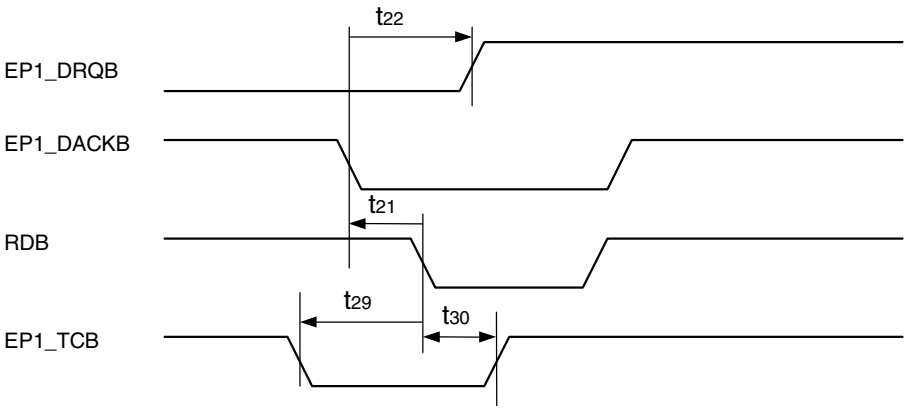
(Start timing)



(End timing)



(TCB timing)



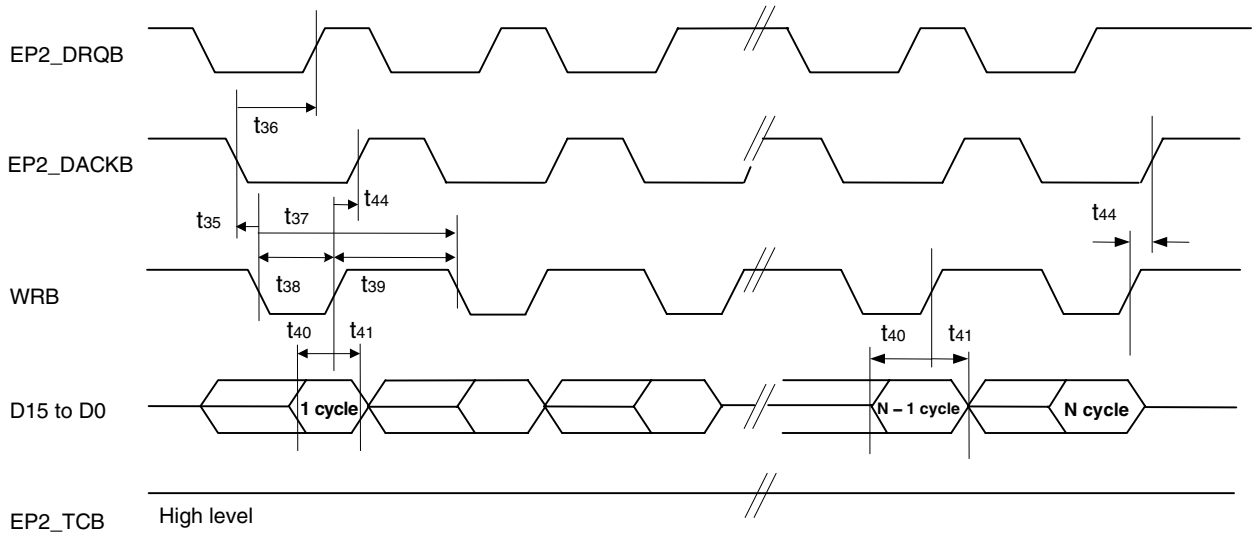
(b) CPU bus DMA single mode write transfer

Symbol	Parameter	Min.	Typ.	Max.	Unit
T35	DMA request acknowledge setup time (WRB↓)	0		∞	ns
T36	DMA request off time (EP2_DACKB↓)	–		54	ns
T37	DMA single mode write transfer cycle time	88		∞	ns
T38	Write command width	54		∞	ns
T39	Write command inactive time	34		∞	ns
T40	Write data setup time (WRB↑)	10		∞	ns
T41	Write data hold time (WRB↑)	0		∞	ns
T42	EP2_TCB setup time (WRB↓)	0		**Note**	ns
T43	EP2_TCB hold time (WRB↓)	17		∞	ns
T44	DMA request acknowledge hold time (WRB↑)	0		∞	ns

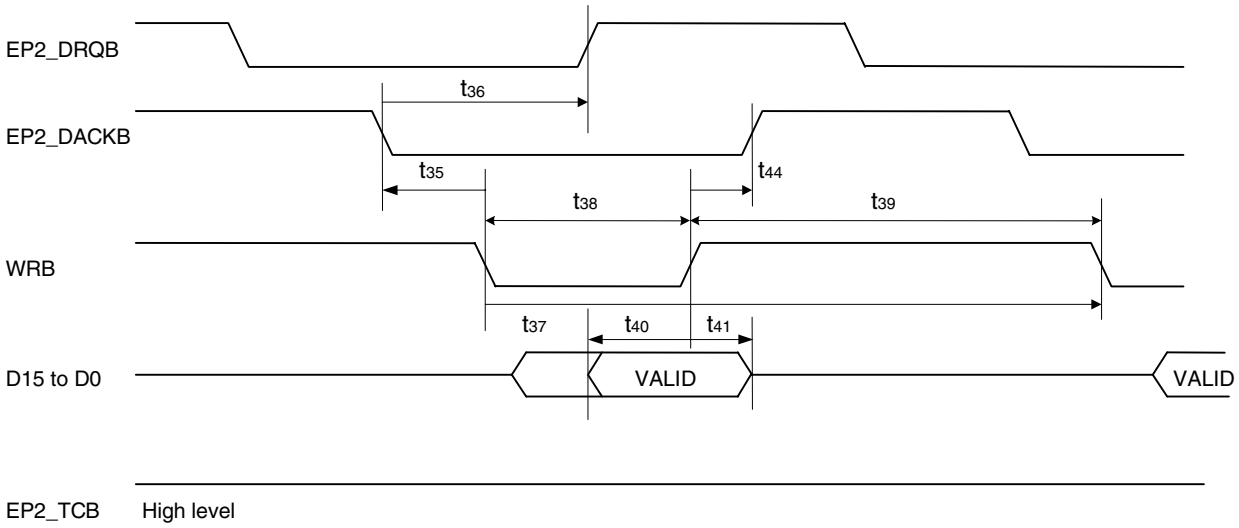
Note Can be input after immediately previous WRB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

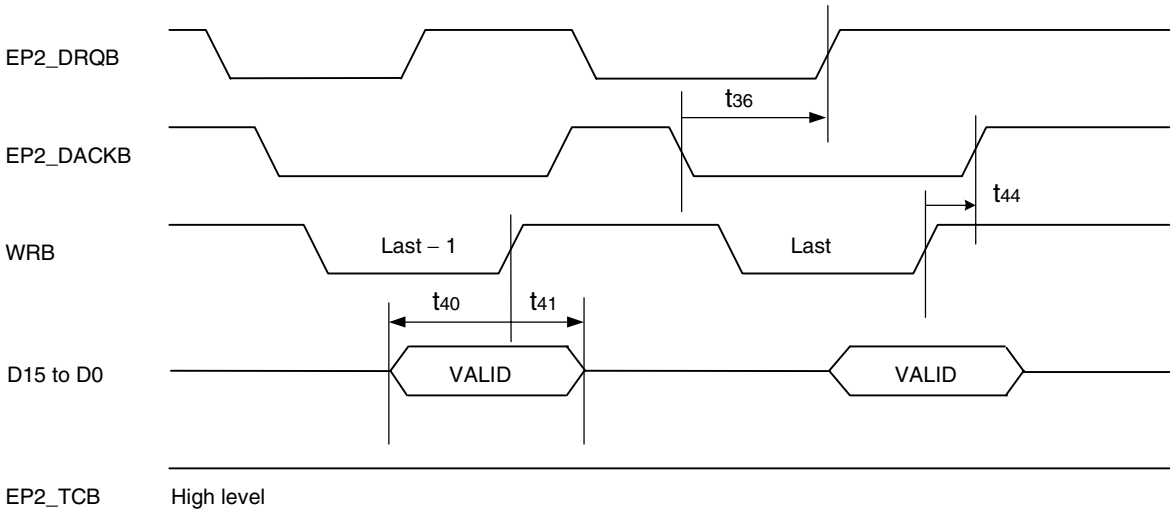
(Overall)



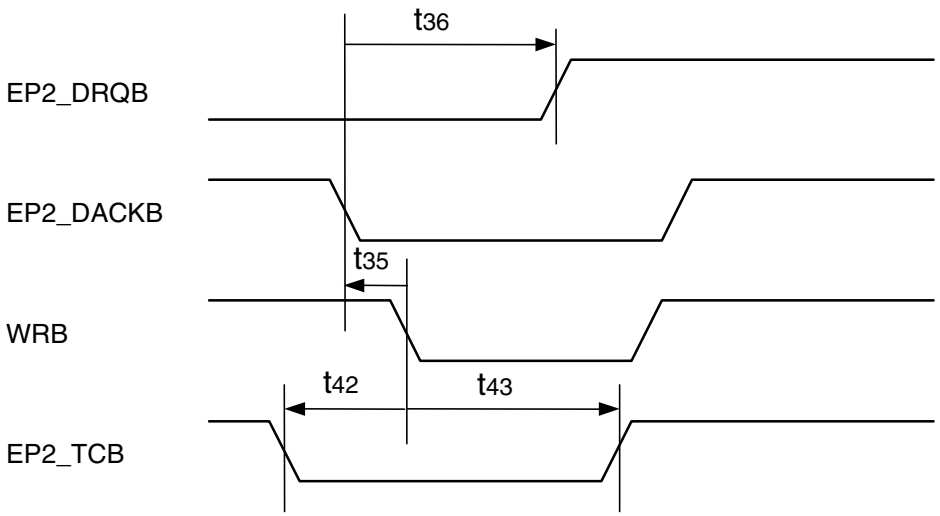
(Start timing)



(End timing)



(TCB timing)



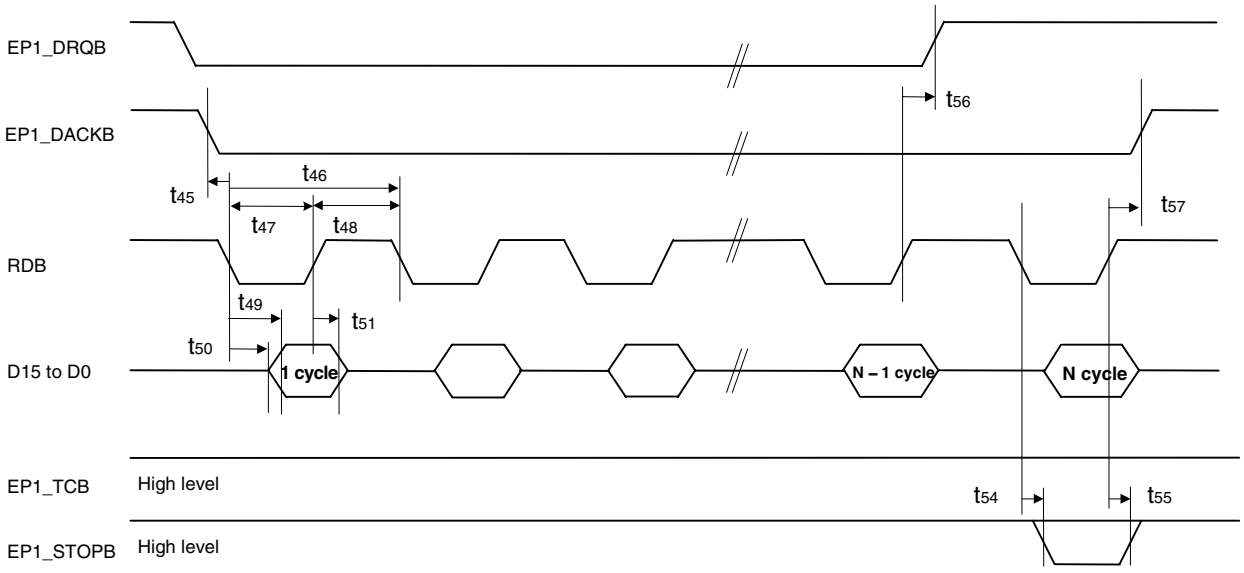
(c) CPU bus DMA demand read transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T45	DMA request acknowledge setup time (RDB↓)	0		∞	ns
T46	DMA demand mode read transfer cycle time	91		∞	ns
T47	Read command width	57		∞	ns
T48	Read command inactive time	34		∞	ns
T49	Read data delay time (RDB↓)	–		57	ns
T50	Buffer direction change time (RDB↓)	–		14	ns
T51	Read data hold time (RDB↑)	4		–	ns
T52	EP1_TCB setup time (RDB↓)	0		**Note**	ns
T53	EP1_TCB hold time (RDB↓)	17		∞	ns
T54	EP1_STOPB delay time (RDB↓)	–		15	ns
T55	EP1_STOPB delay time (RDB↑)	3		–	ns
T56	DMA request off time (RDB↑)	–		59	ns
T57	DMA request acknowledge hold time (RDB↑)	0		∞	ns
T69	DMA request off time (EP1_DACKB↓)	–		38	ns
T71	DMA request off time (EP1_DACKB↓) 1 cycle transfer	–		38	ns
T72	DMA request on time (EP1_DACKB↑)	–		88	ns
T74	DMA request off time (RDB↓)	–		60	ns

Note Can be input after immediately previous RDB↑.

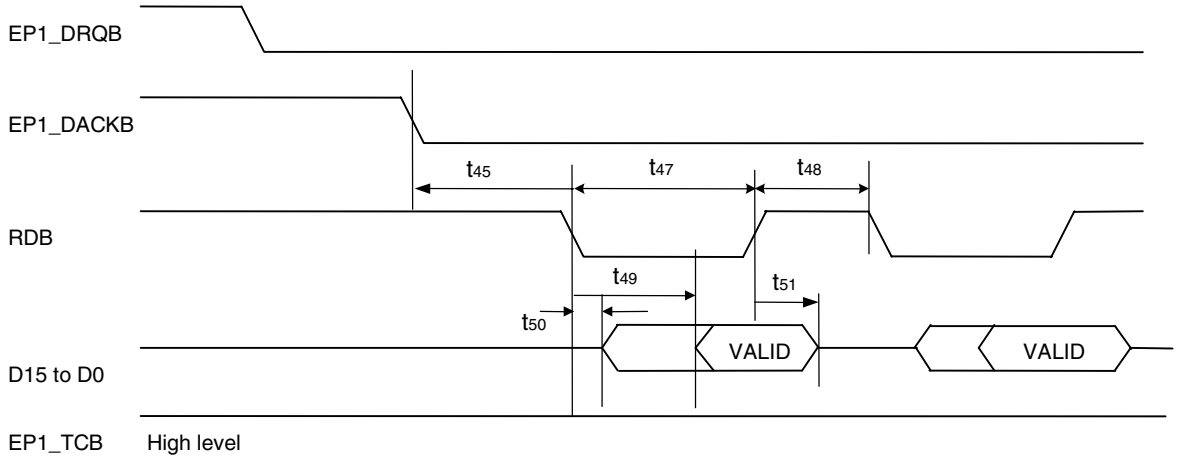
Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

(Overall)

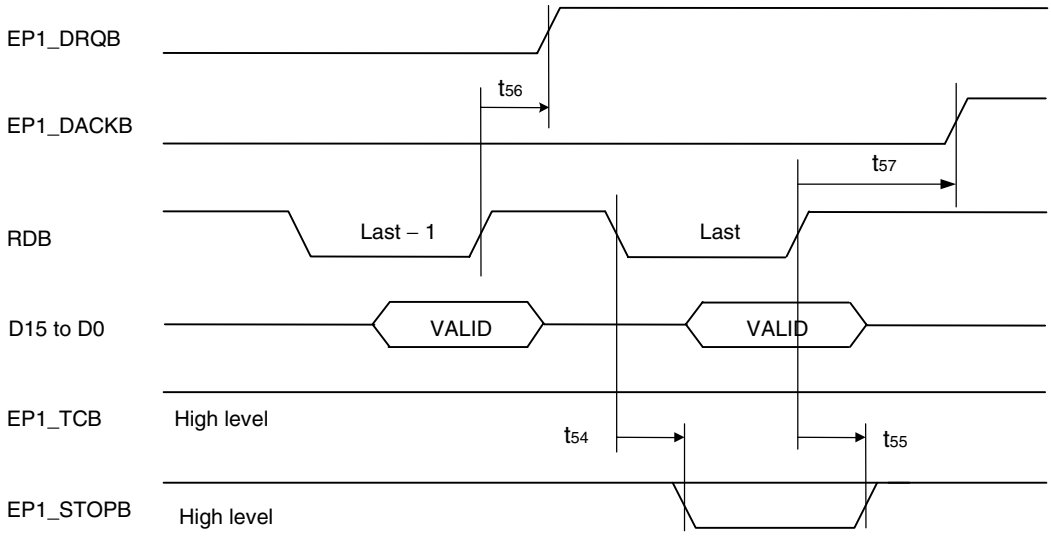


EP1_STOPB is not asserted in the case of a full packet.

(Start timing)

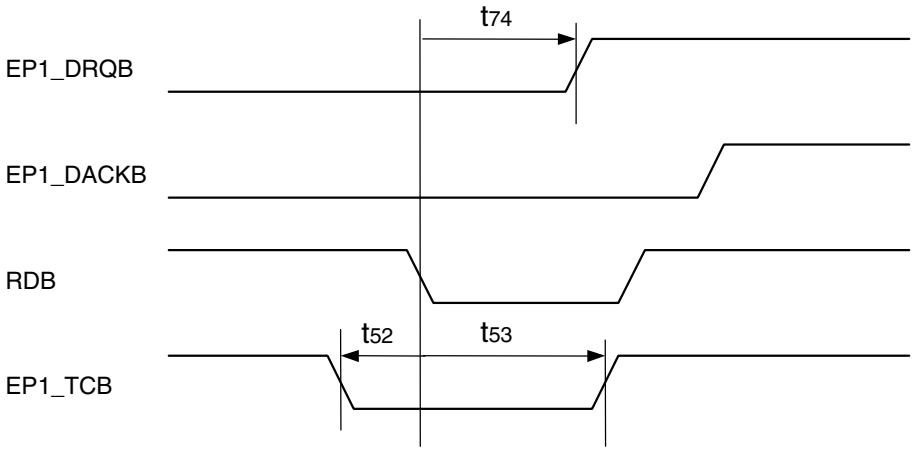


(End timing)

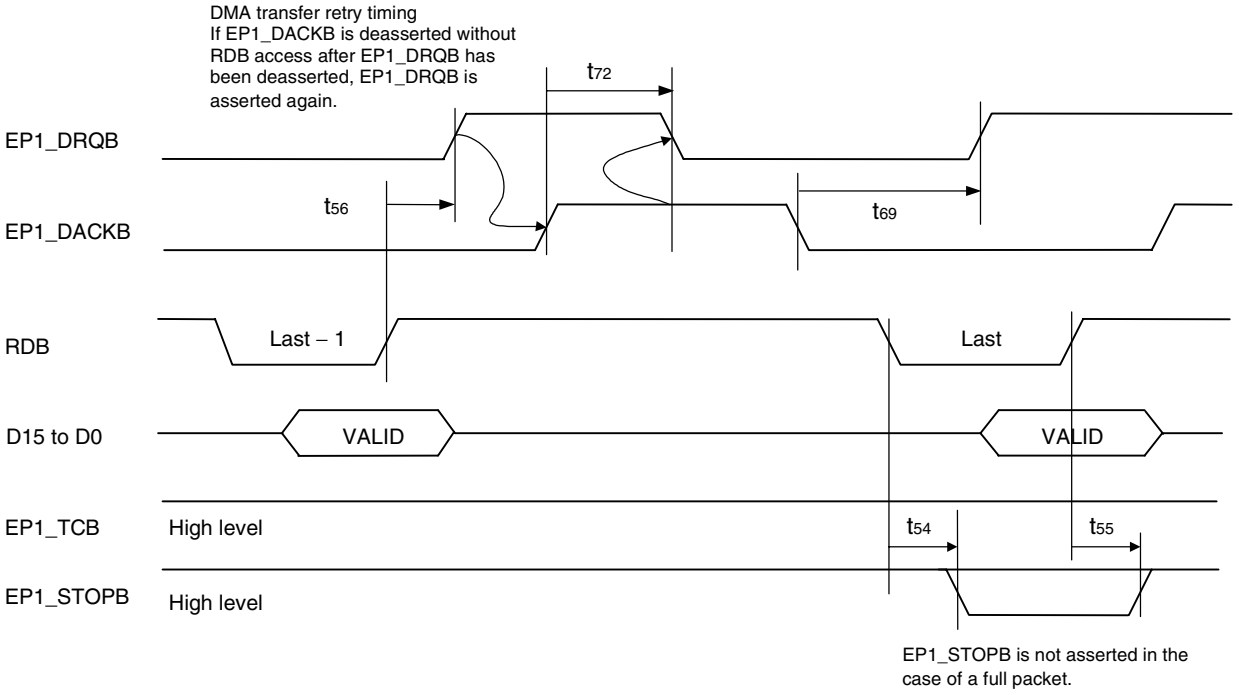


EP1_STOPB is not asserted in the case of a full packet.

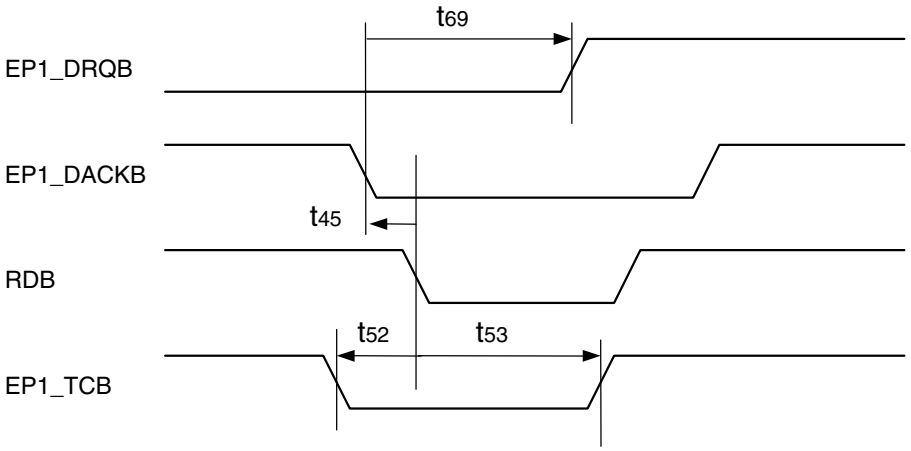
(TCB timing)



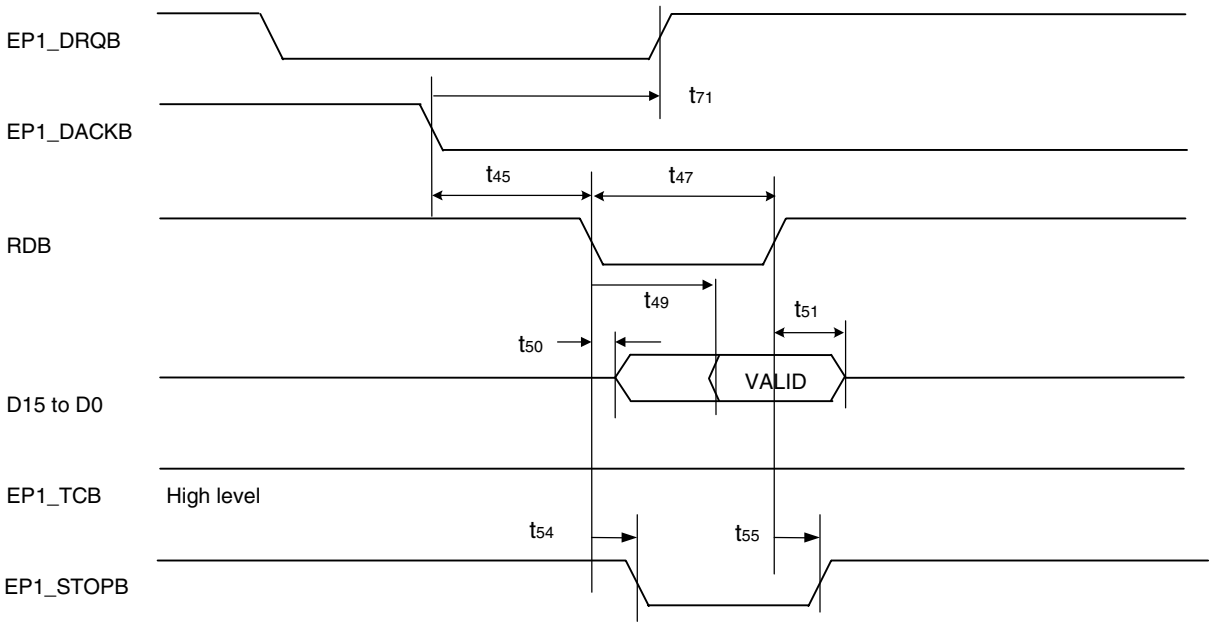
(Retransmission timing)



(If EP1_TCB is input when retransmission is executed)



(One-cycle transfer)



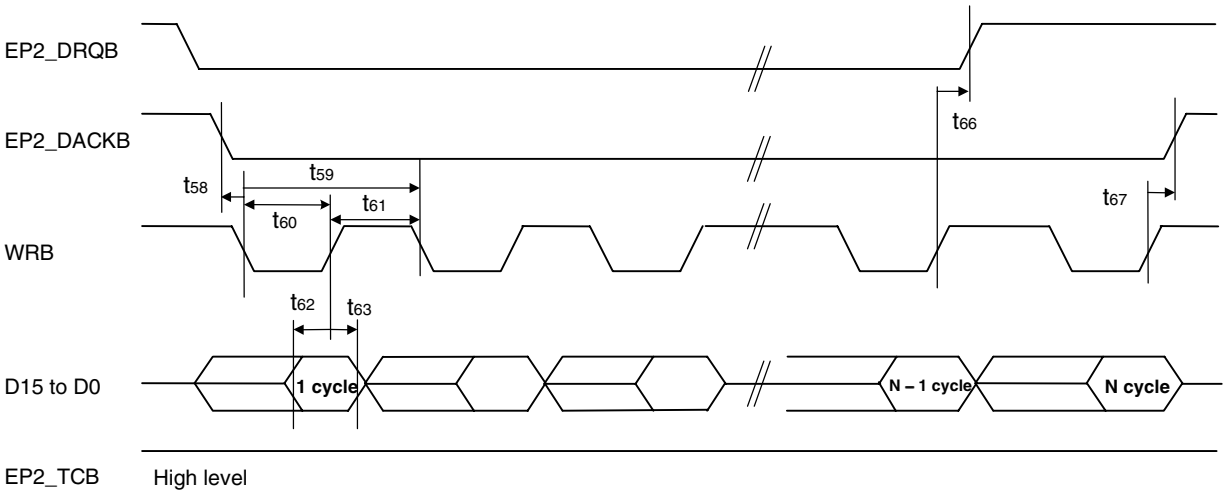
(d) CPU bus DMA demand write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T58	DMA request acknowledge setup time (WRB↓)	0		∞	ns
T59	DMA demand mode write transfer cycle time	72		∞	ns
T60	Write command width	38		∞	ns
T61	Write command inactive time	34		∞	ns
T62	Write data setup time (WRB↑)	10		∞	ns
T63	Write data hold time (WRB↑)	0		∞	ns
T64	EP2_TCB setup time (WRB↓)	0		**Note**	ns
T65	EP2_TCB hold time (WRB↓)	17		∞	ns
T66	DMA request off time (WRB↑)	−		60	ns
T67	DMA request acknowledge hold time (WRB↑)	0		∞	ns
T70	DMA request off time (EP2_DACKB↓)	−		38	ns
T73	DMA request on time (EP2_DACKB↑)	−		88	ns
T75	DMA request off time (WRB↓)	−		60	ns

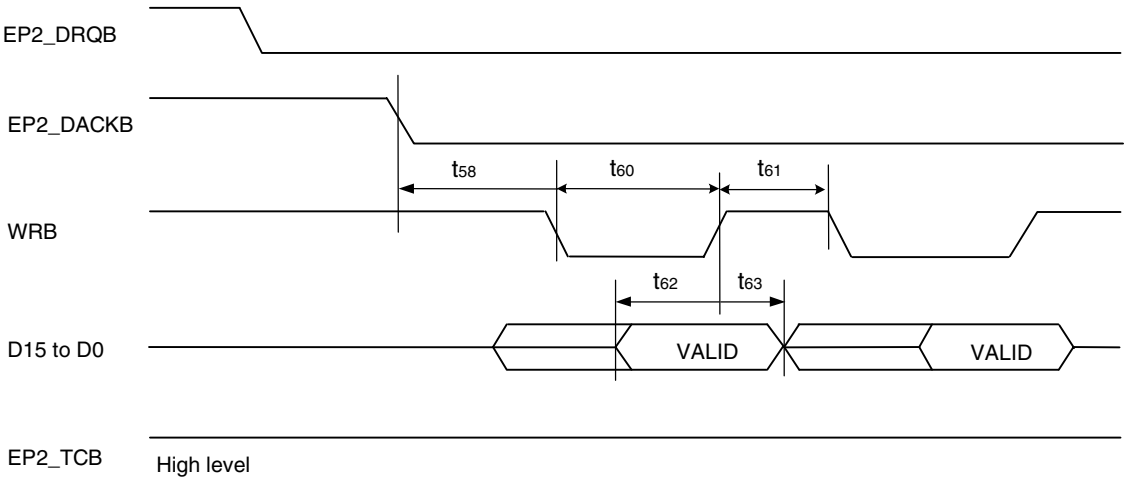
Note Can be input after immediately previous WRB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

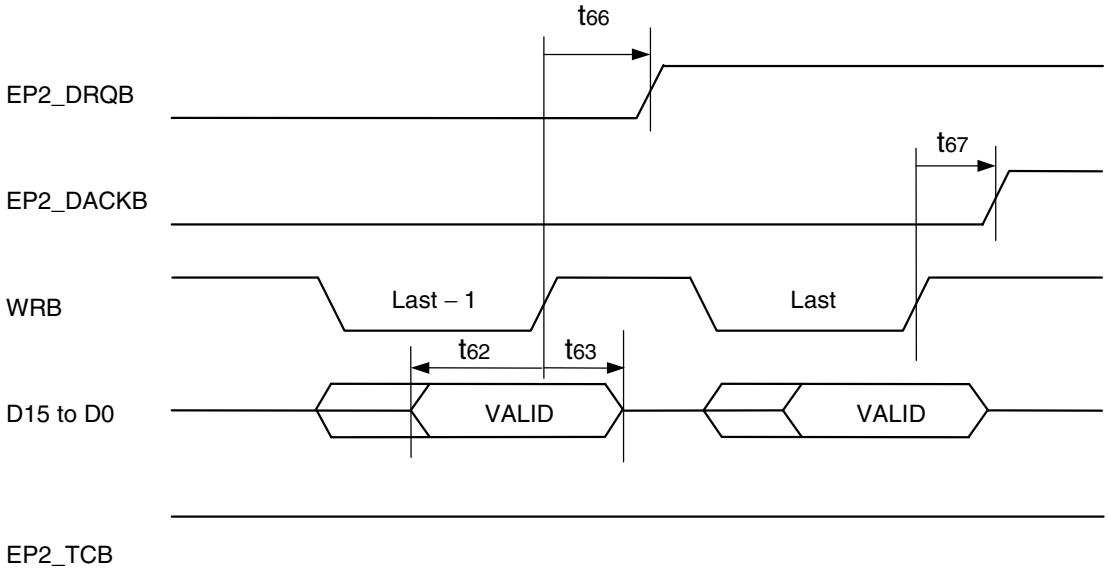
(Overall)



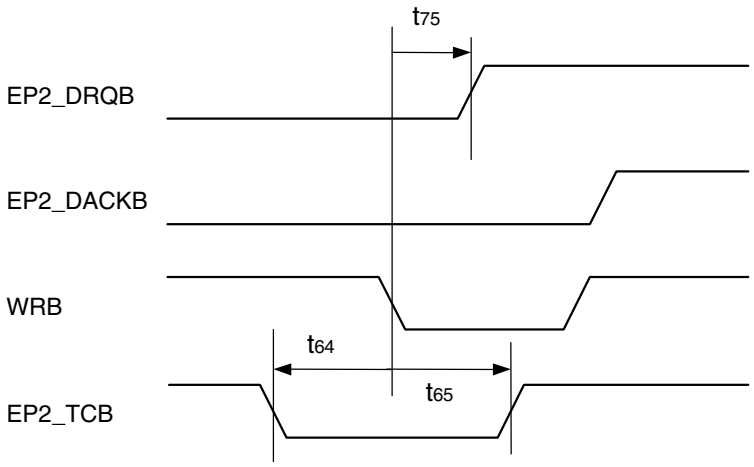
(Start timing)



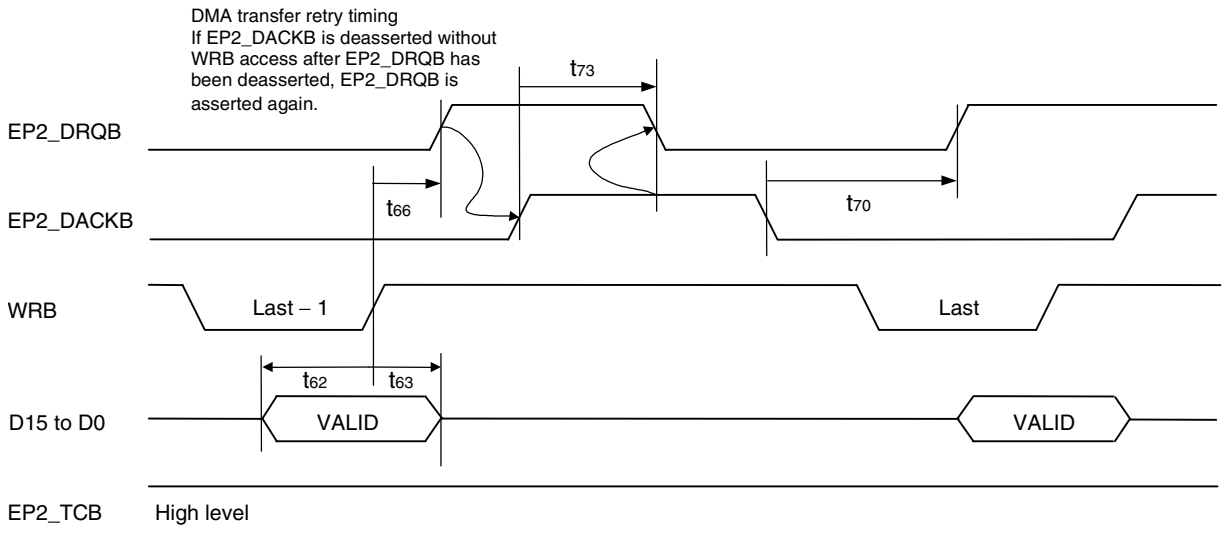
(End timing)



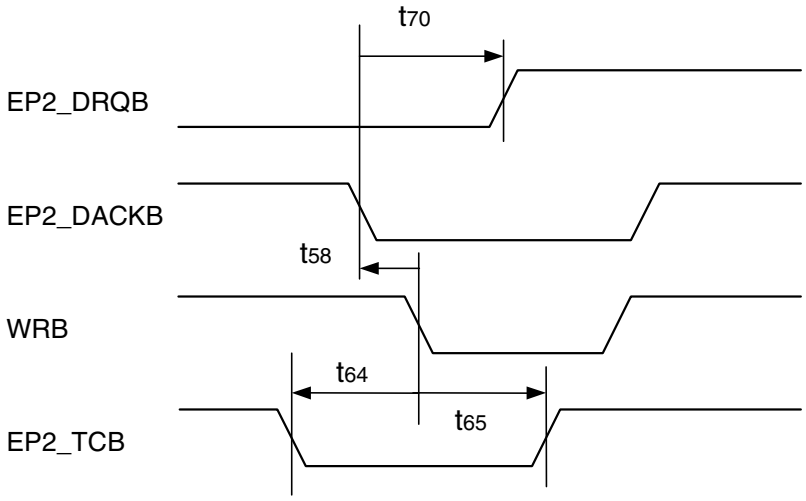
(TCB timing)



(Retransmission timing)



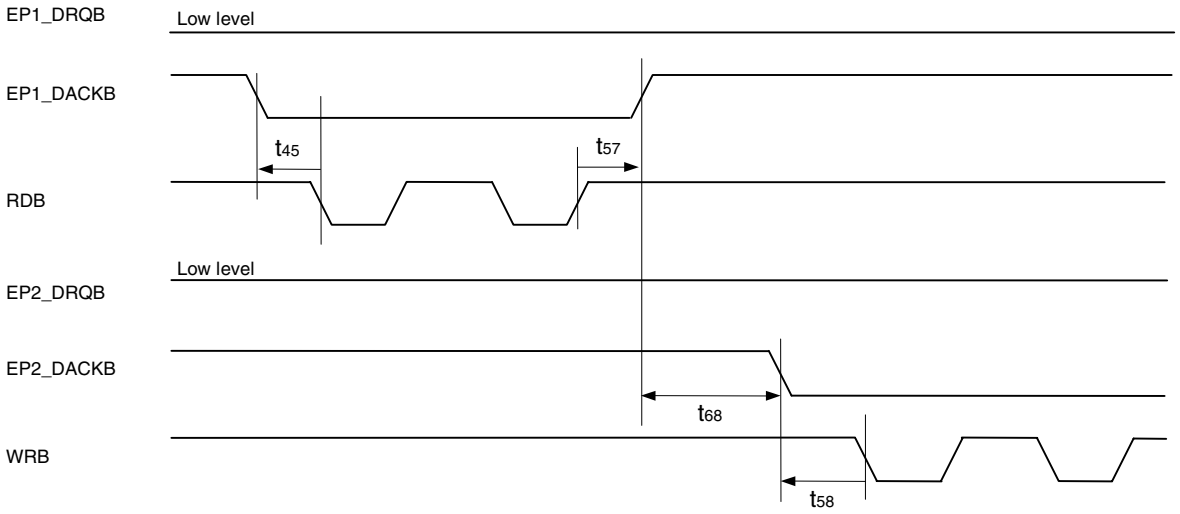
(If EP1_TCB is input when retransmission is executed)



(a) CPU bus DMA read transfer vs. write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T68	RDB vs. WRB command inactive time	34		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).



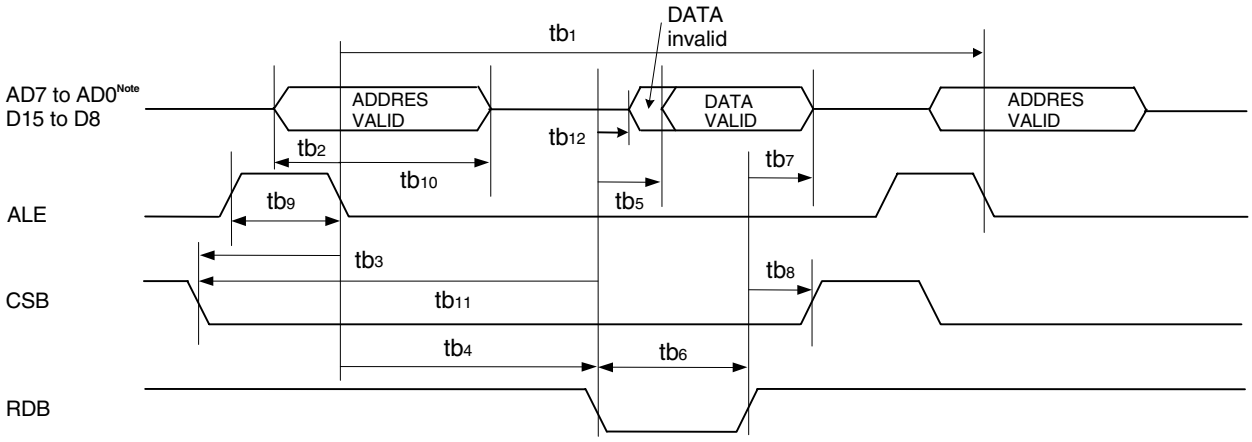
2.6.3 AC characteristics of BIU block with function 2 or 3 selected

(1) CPU bus read operation

Symbol	Parameter	Min.	Typ.	Max.	Unit
TB1	Read cycle time	86		∞	ns
TB2	Address setup time (ALE↓)	10		∞	ns
TB3	Chip select setup time (ALE↓)	17		∞	ns
TB4	Read command delay time (ALE↓)	7		∞	ns
TB5	Output data delay time (RDB↓)	–		57	ns
TB6	Read command width	57		∞	ns
TB7	Output data hold time (RDB↑)	4		–	ns
TB8	Chip select hold time (RDB↑)	5		∞	ns
TB9	ALE width	10		∞	ns
TB10	Address hold time (ALE↓)	0		∞	ns
TB11	Chip select setup time (RDB↓)	5		∞	ns
TB12	Buffer direction change time (RDB↓)	–		14	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

CPU bus read timing



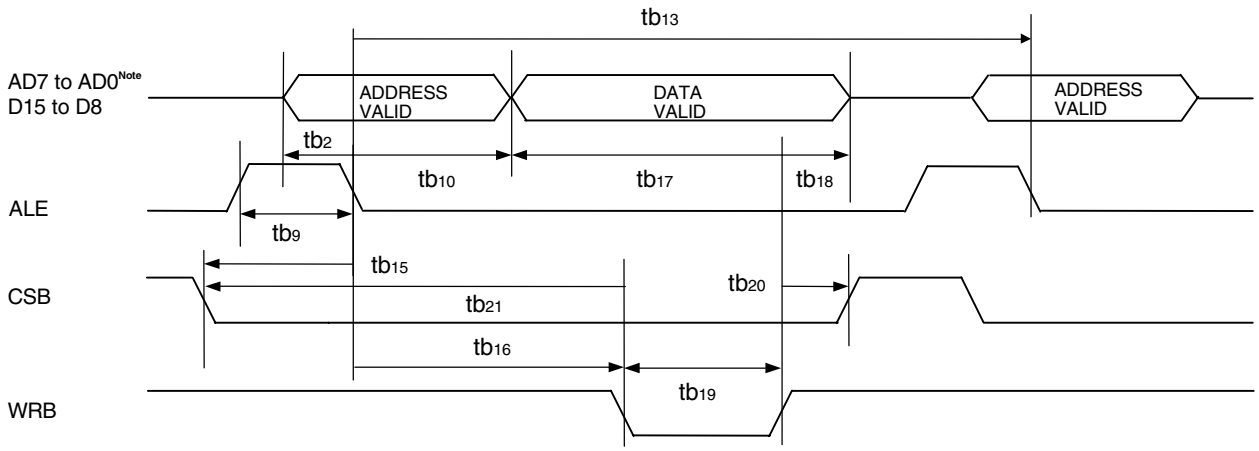
Note D7 to D0 for Function 2

(2) CPU bus write operation

Symbol	Parameter	Min.	Typ.	Max.	Unit
TB13	Write cycle time	58		∞	ns
TB14	Address setup time (ALE↓)	17		∞	ns
TB15	Chip select setup time (ALE↓)	17		∞	ns
TB16	Write command delay time (ALE↓)	7		∞	ns
TB17	Input data setup time (WRB↑)	10		∞	ns
TB18	Input data hold time (WRB↑)	0		∞	ns
TB19	Write command width	34		∞	ns
TB20	Chip select hold time (WRB↑)	0		∞	ns
TB21	Chip select setup time (WRB↓)	5		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

CPU bus write timing



Note D7 to D0 for Function 2

2.6.4 External local bus

(1) External local bus 16-bit mode

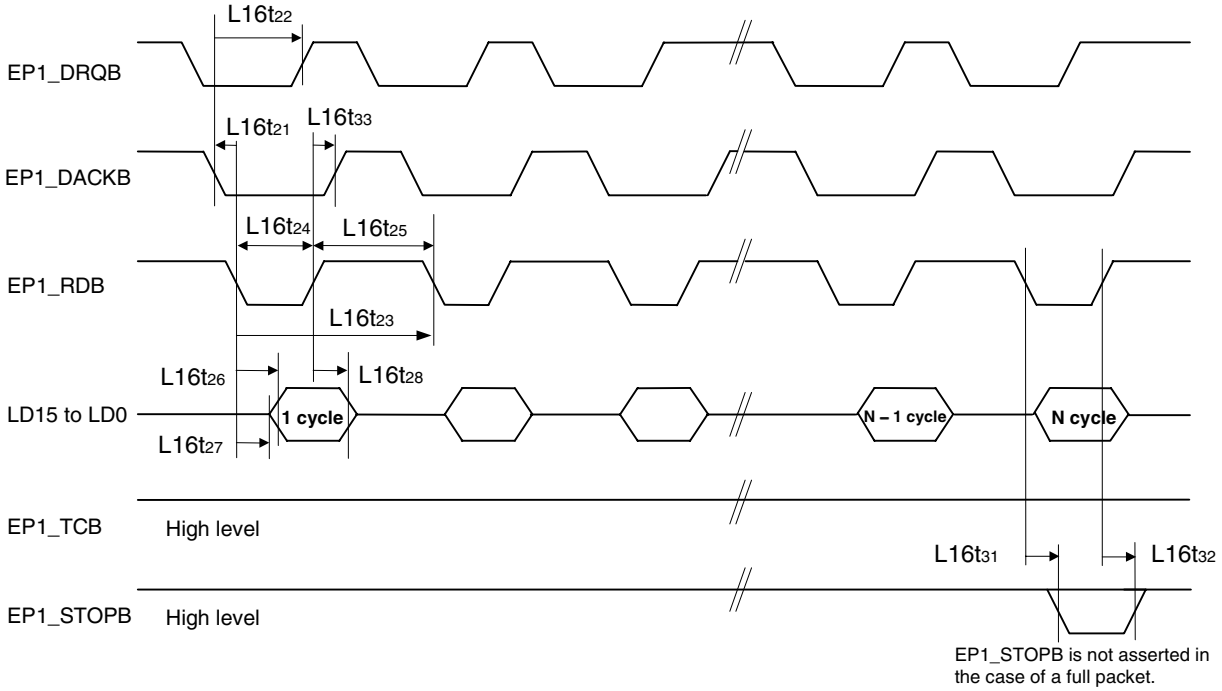
(a) External local bus 16-bit mode DMA single mode read transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T21	DMA request acknowledge setup time (EP1_RDB↓)	0		∞	ns
L16T22	DMA request off time 1 (EP1_DACKB↓)	−		54	ns
L16T23	DMA single mode read transfer cycle time	91		∞	ns
L16T24	Read command width	57		∞	ns
L16T25	Read command inactive time	34		∞	ns
L16T26	Read data delay time (EP1_RDB↓)	−		57	ns
L16T27	Buffer direction change time (EP1_RDB↓)	−		14	ns
L16T28	Read data hold time (EP1_RDB↑)	4		−	ns
L16T29	EP1_TCB setup time (EP1_RDB↓)	0		**Note**	ns
L16T30	EP1_TCB hold time (EP1_RDB↓)	17		∞	ns
L16T31	EP1_STOPB delay time (EP1_RDB↓)	−		15	ns
L16T32	EP1_STOPB delay time (EP1_RDB↑)	3		−	ns
L16T33	DMA request acknowledge hold time (EP1_RDB↑)	0		∞	ns
L16T34	Undefined	−		−	ns

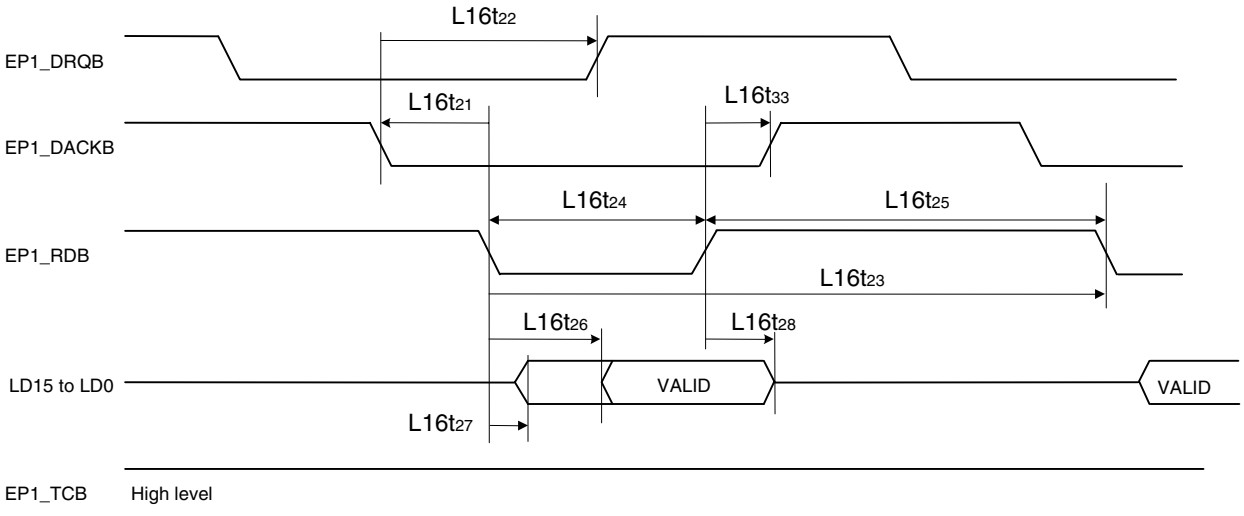
Note Can be input after previous EP1_RDB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

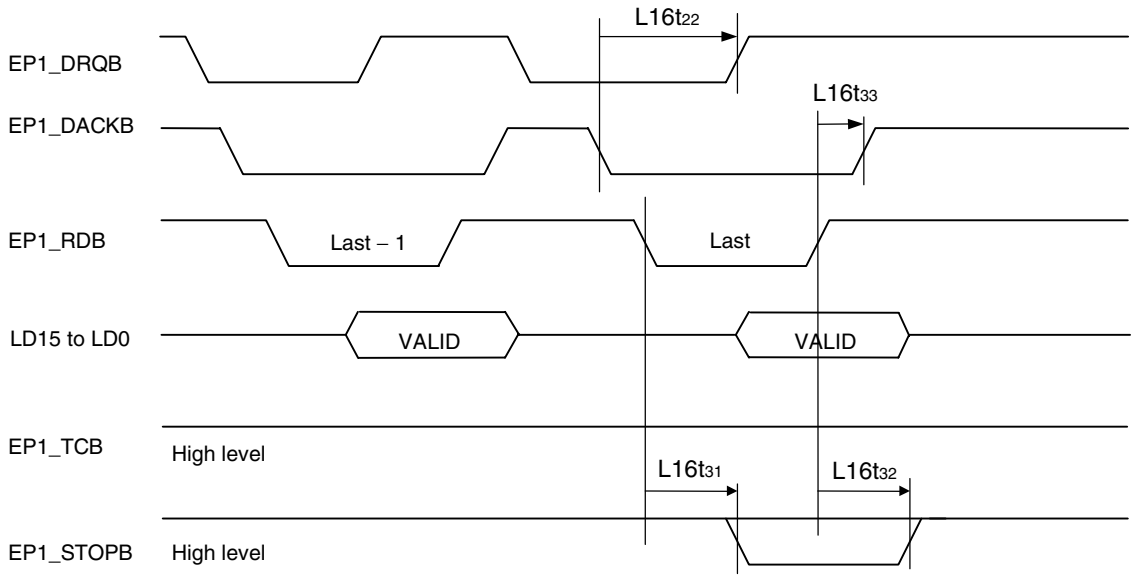
(Overall)



(Start timing)

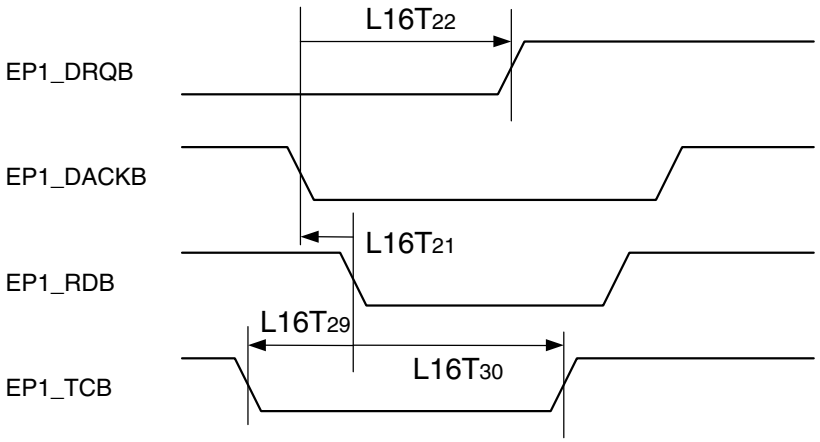


(End timing)



EP1_STOPB is not asserted in the case of a full packet.

(TCB timing)



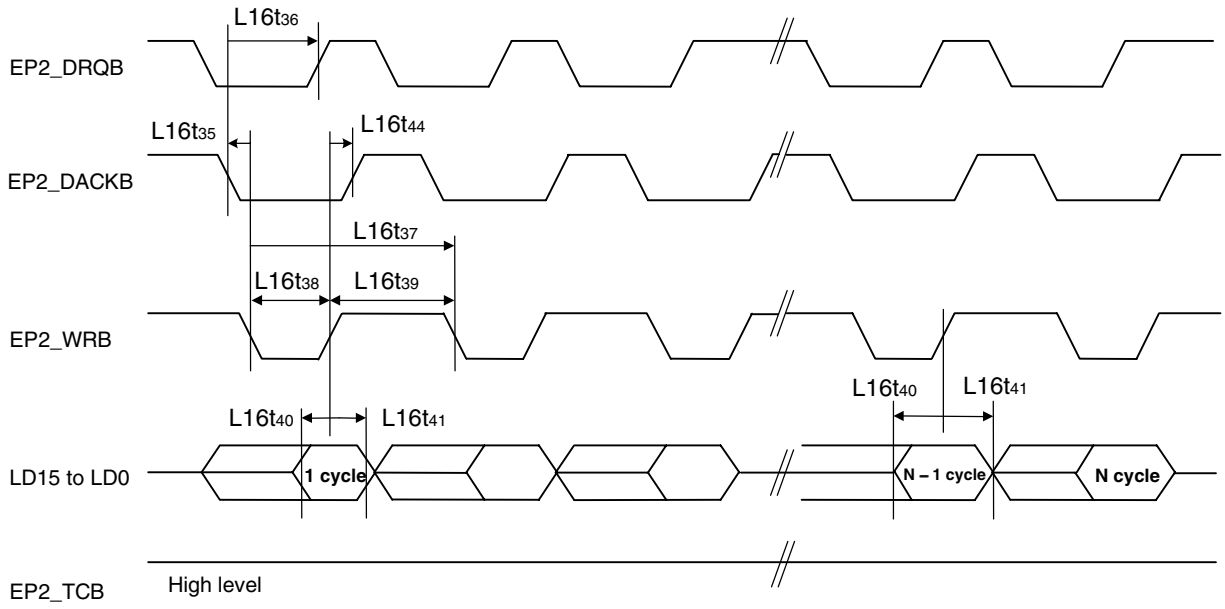
(a) External local bus 16-bit mode DMA single mode write transfer

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T35	DMA request acknowledge setup time (EP2_WRB↓)	0		∞	ns
L16T36	DMA request off time 1 (EP2_DACKB↓)	–		54	ns
L16T37	DMA single mode write transfer cycle time	88		∞	ns
L16T38	Write command width	54		∞	ns
L16T39	Write command inactive time	34		∞	ns
L16T40	Write data setup time (EP2_WRB↑)	10		∞	ns
L16T41	Write data hold time (EP2_WRB↑)	0		∞	ns
L16T42	EP2_TCB setup time (EP2_WRB↓)	0		**Note**	ns
L16T43	EP2_TCB hold time (EP2_WRB↓)	17		∞	ns
L16T44	DMA request acknowledge hold time (EP2_WRB↑)	0		∞	ns

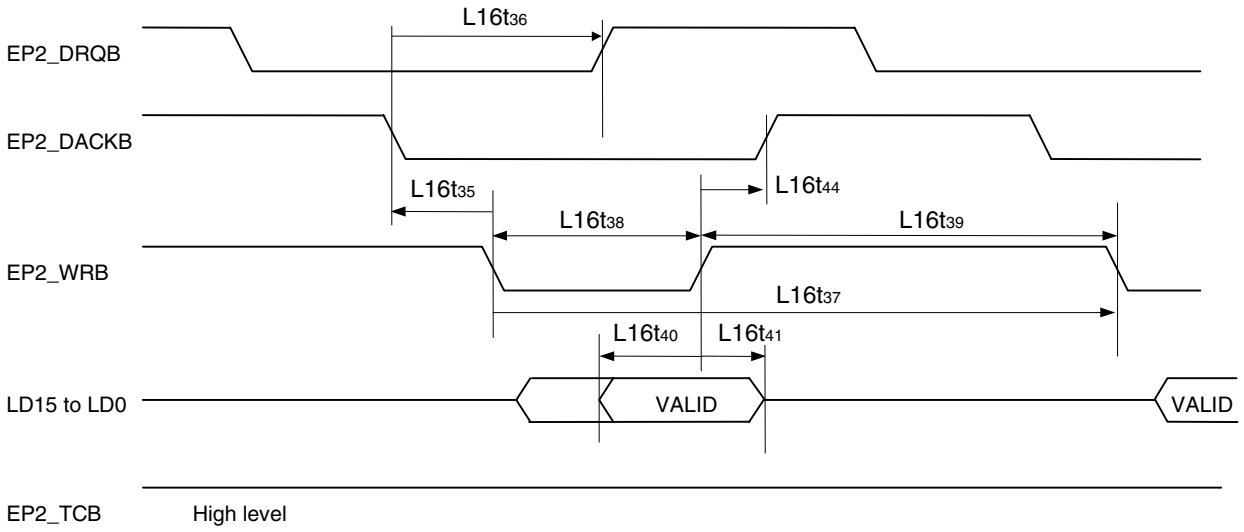
Note Can be input after previous EP2_WRB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

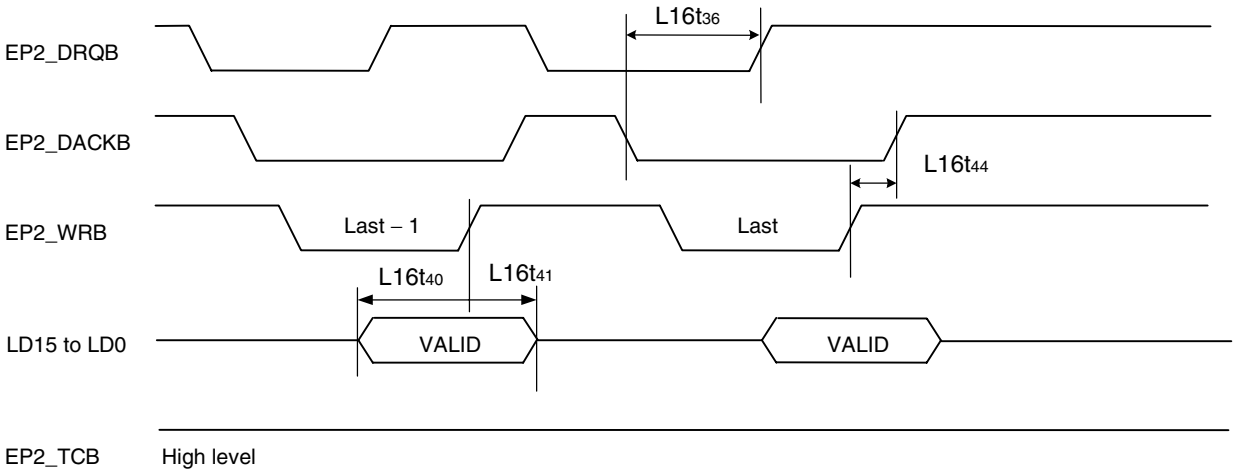
(Overall)



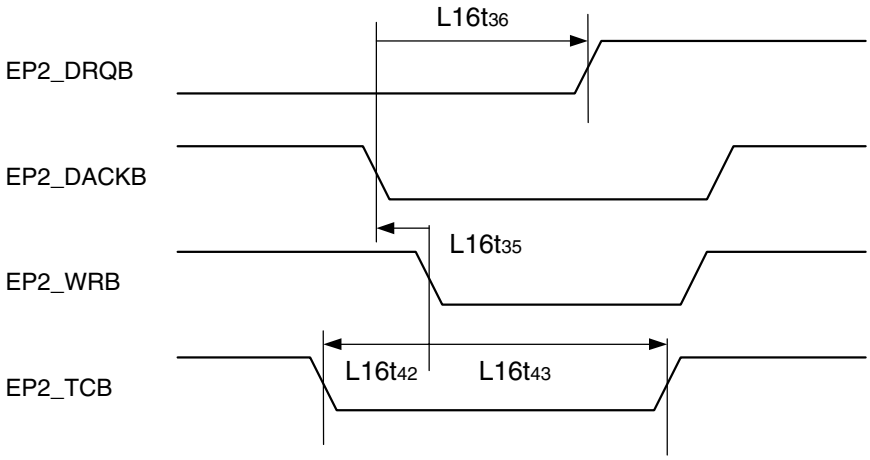
(Start timing)



(End timing)



(TCB timing)


L16t36
EP2_DRQB
EP2_DACKB
L16t35
EP2_WRB
L16t42
L16t43
EP2_TCB

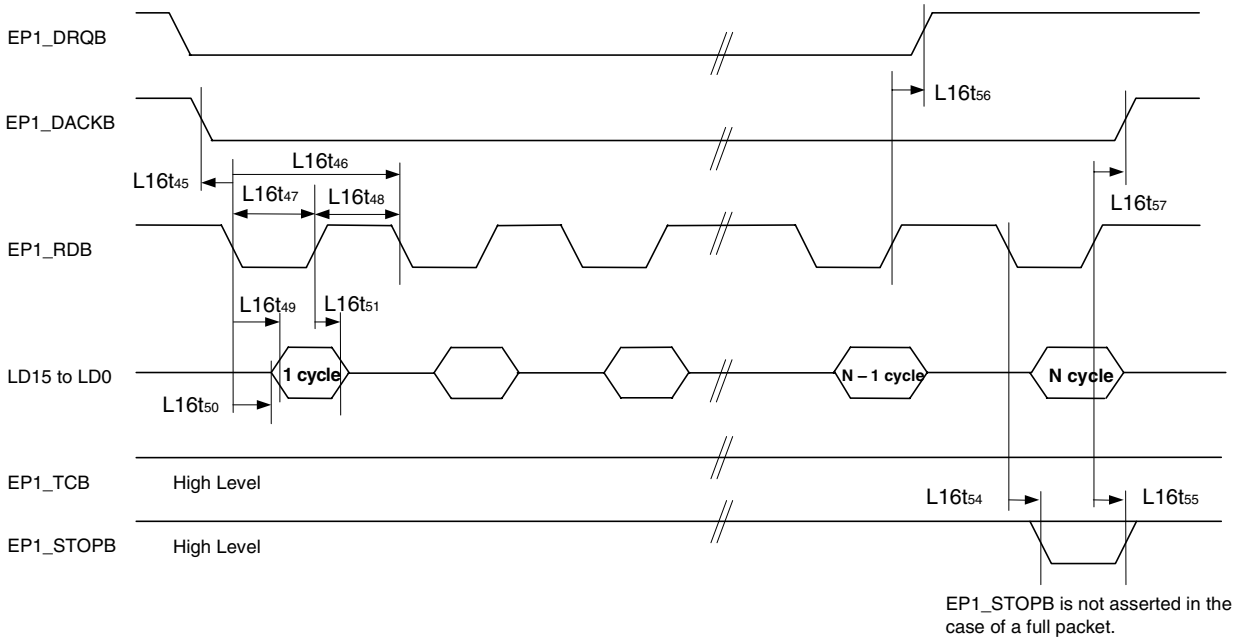
(c) External local bus 16-bit mode DMA demand read transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T45	DMA request acknowledge setup time (EP1_RDB↓)	0		∞	ns
L16T46	DMA demand mode read transfer cycle time	91		∞	ns
L16T47	Read command width	57		∞	ns
L16T48	Read command inactive time	34		∞	ns
L16T49	Read data delay time (EP1_RDB↓)	–		57	ns
L16T50	Buffer direction change time (EP1_RDB↓)	–		14	ns
L16T51	Read data hold time (EP1_RDB↑)	4		–	ns
L16T52	EP1_TCB setup time (EP1_RDB↓)	0		**Note**	ns
L16T53	EP1_TCB hold time (EP1_RDB↓)	17		∞	ns
L16T54	EP1_STOPB delay time (EP1_RDB↓)	–		15	ns
L16T55	EP1_STOPB delay time (EP1_RDB↑)	3		–	ns
L16T56	DMA request off time (EP1_RDB↑)	–		59	ns
L16T57	DMA request acknowledge hold time (EP1_RDB↑)	0		∞	ns
L16T69	DMA request off time (EP1_DACKB↓)	–		38	ns
L16T71	DMA request off time (EP1_DACKB↓) 1 cycle transfer	–		38	ns
L16T72	DMA request on time (EP1_DACKB↑)	–		88	ns
L16T74	DMA request off time (EP1_RDB↓)	–		60	ns

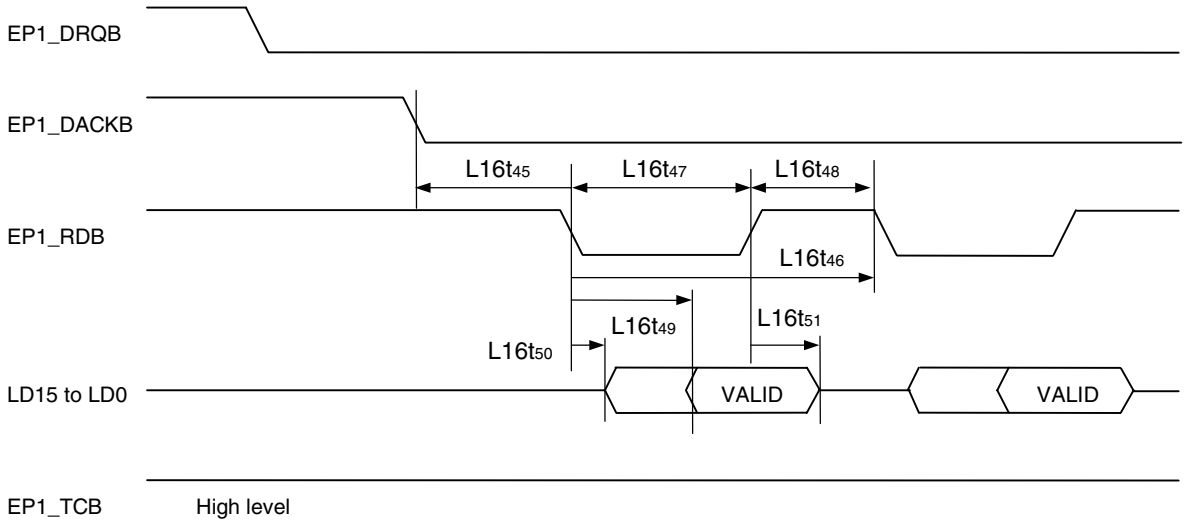
Note Can be input after immediately previous EP1_RDB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

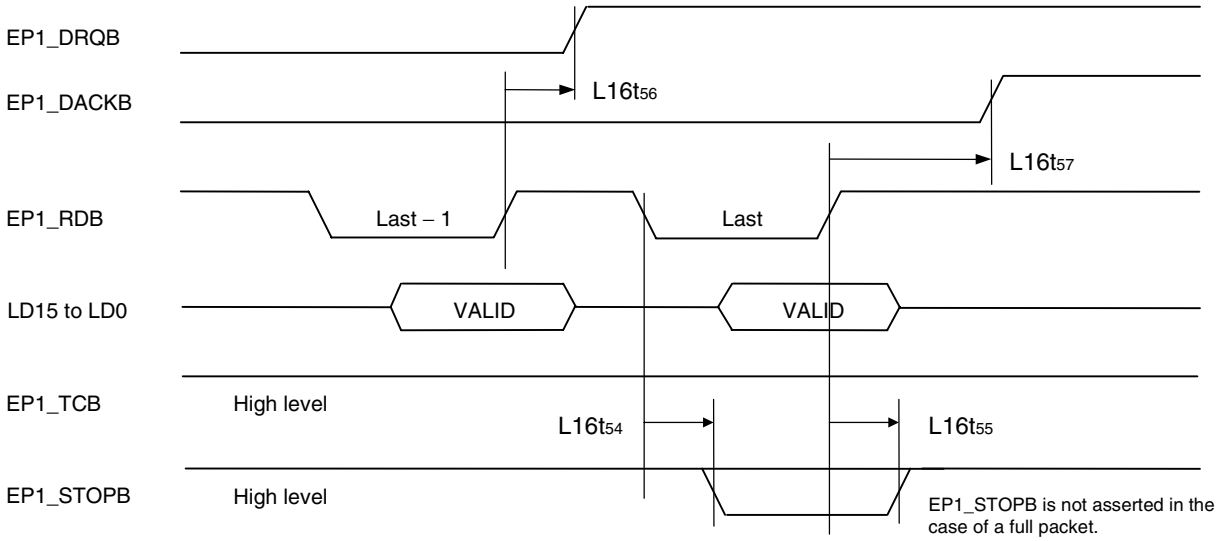
(Overall)



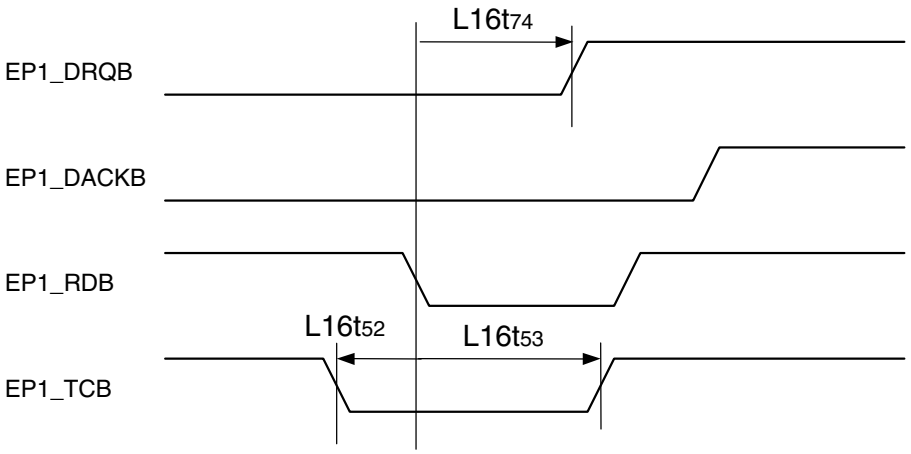
(Start timing)



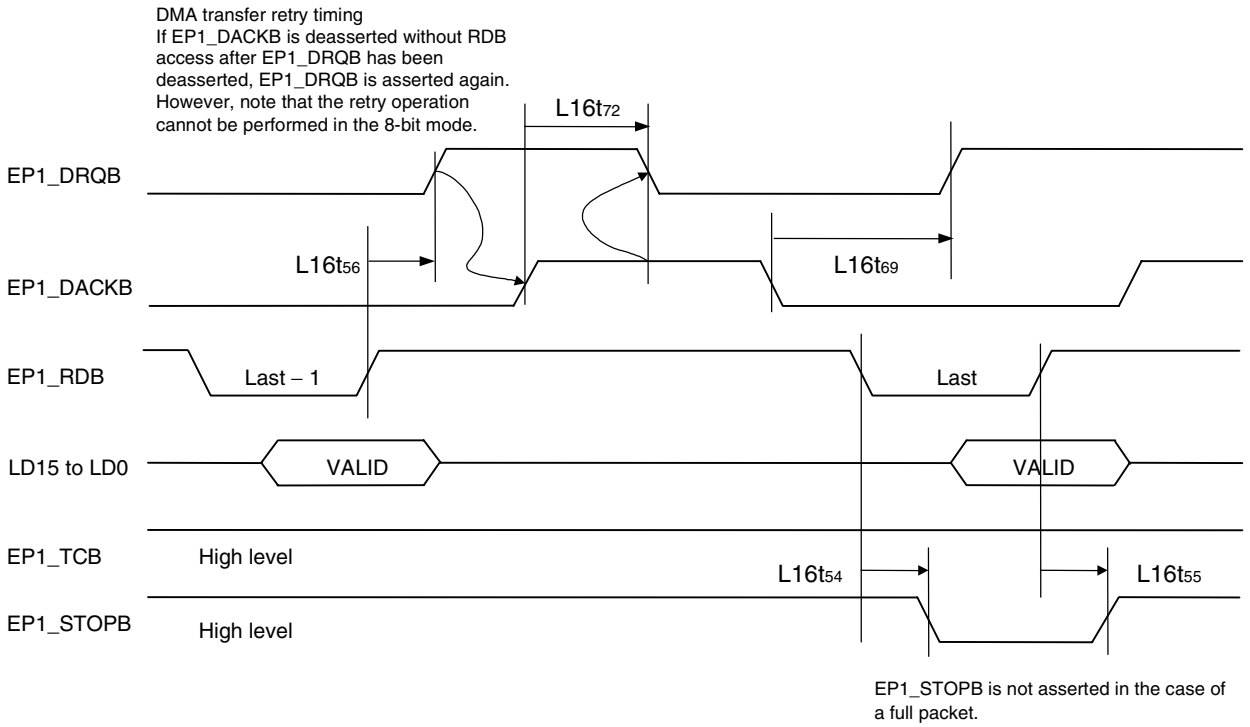
(End timing)



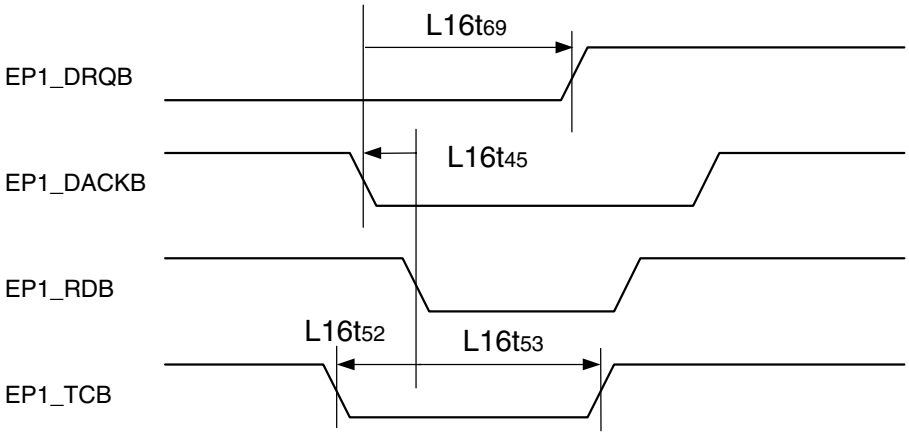
(TCB timing)



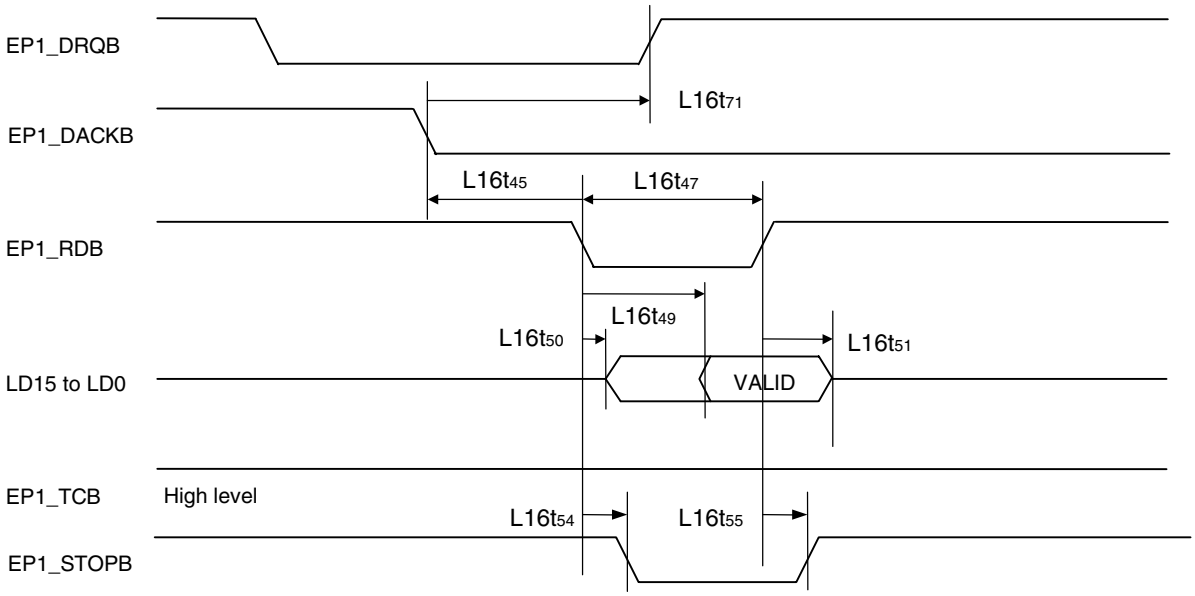
(Retransmission timing)



(If EP1_TCB is input when retransmission is executed)



(One-cycle transfer)



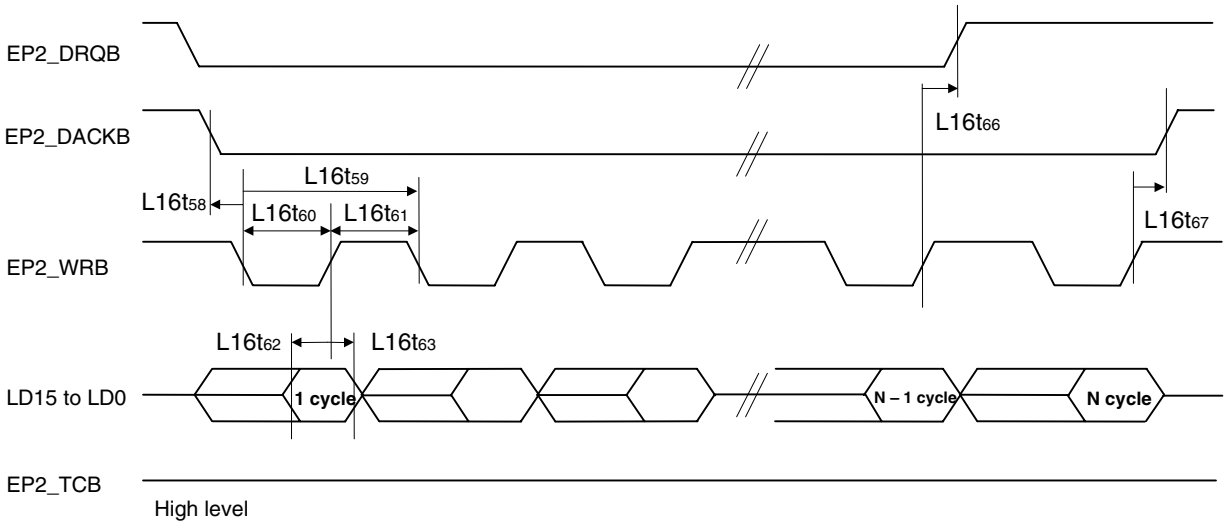
(d) External local bus 16-bit mode DMA demand write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T58	DMA request acknowledge setup time (EP2_WRB↓)	0		∞	ns
L16T59	DMA demand mode write transfer cycle time	72		∞	ns
L16T60	Write command width	38		∞	ns
L16T61	Write command inactive time	34		∞	ns
L16T62	Write data setup time (EP2_WRB↑)	10		∞	ns
L16T63	Write data hold time (EP2_WRB↑)	0		∞	ns
L16T64	EP2_TCB setup time (EP2_WRB↓)	0		**Note**	ns
L16T65	EP2_TCB hold time (EP2_WRB↓)	17		∞	ns
L16T66	DMA request off time (EP2_WRB↑)	−		60	ns
L16T67	DMA request acknowledge hold time (EP2_WRB↑)	0		∞	ns
L16T70	DMA request off time (EP2_DACKB↓)	−		38	ns
L16T73	DMA request on time (EP2_DACKB↑)	−		88	ns
L16T75	DMA request off time (EP2_WRB↓)	−		60	ns

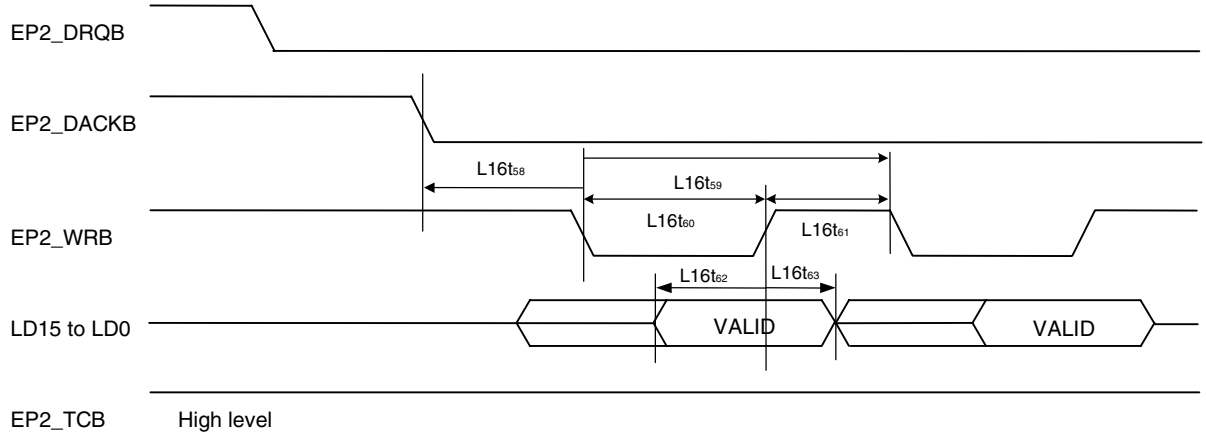
Note Can be input after previous EP2_WRB↑.

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

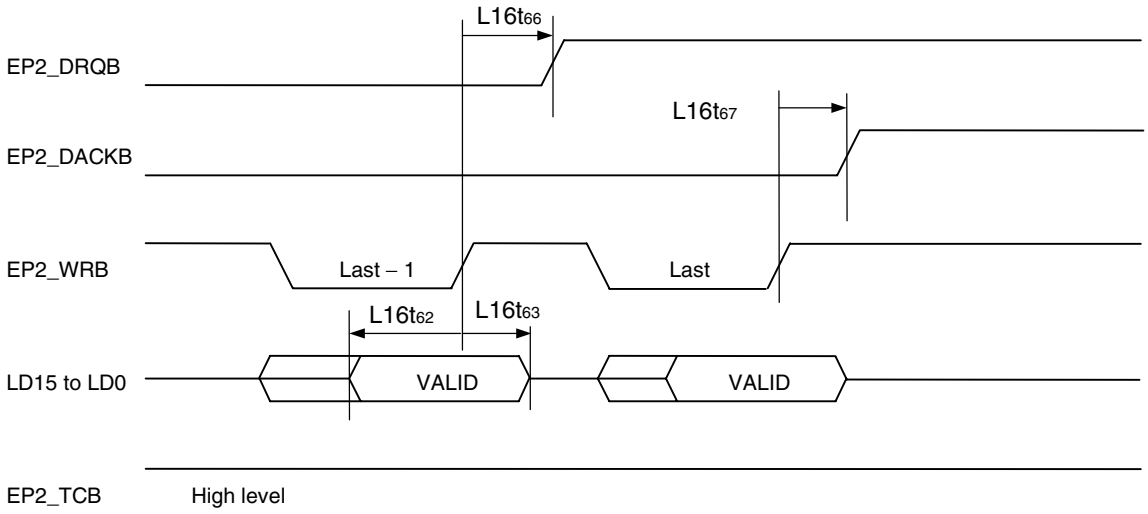
(Overall)



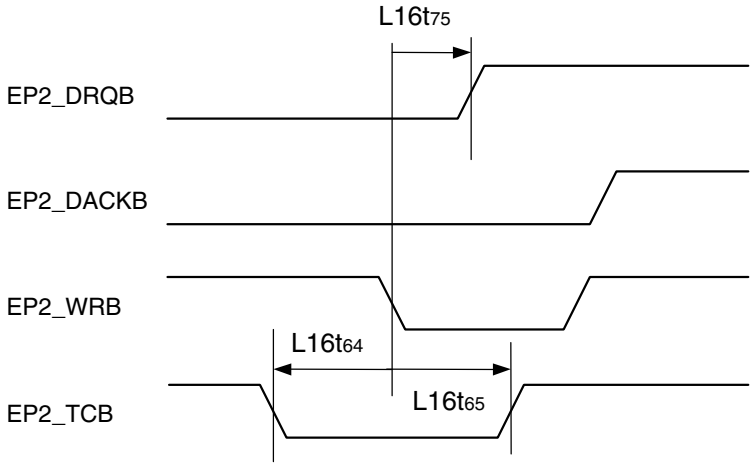
(Start timing)



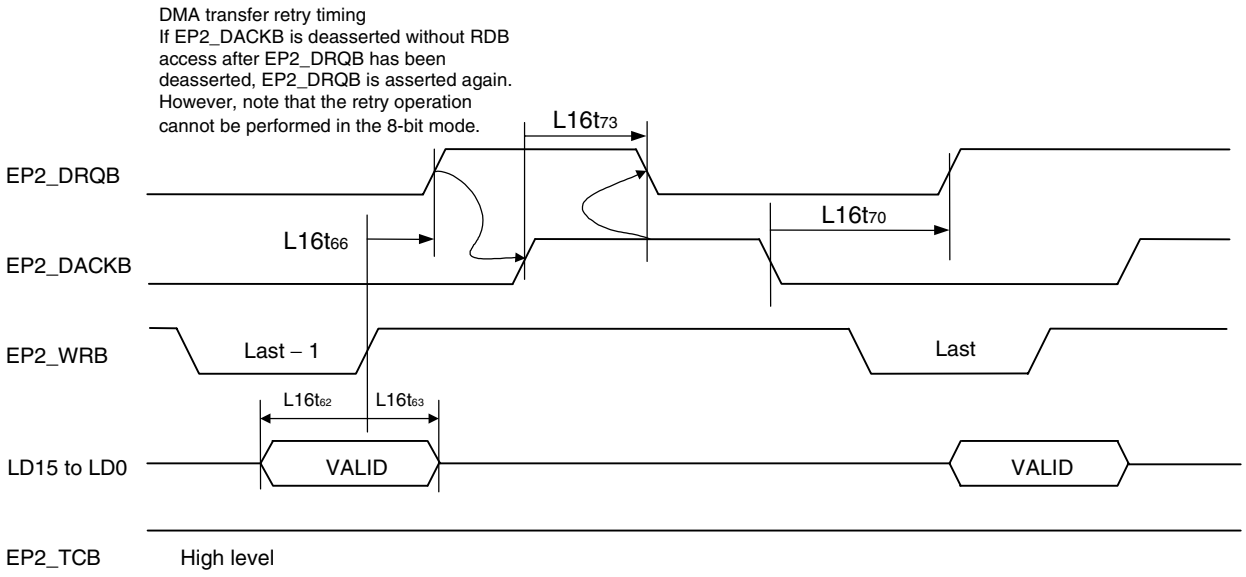
(End timing)



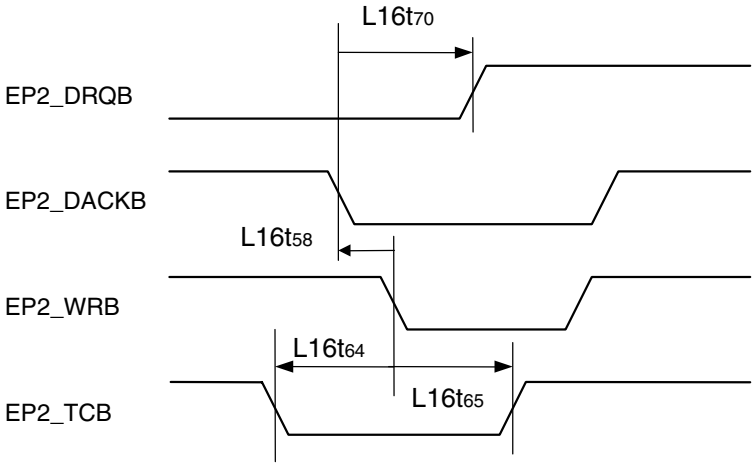
(TCB timing)



(Retransmission timing)



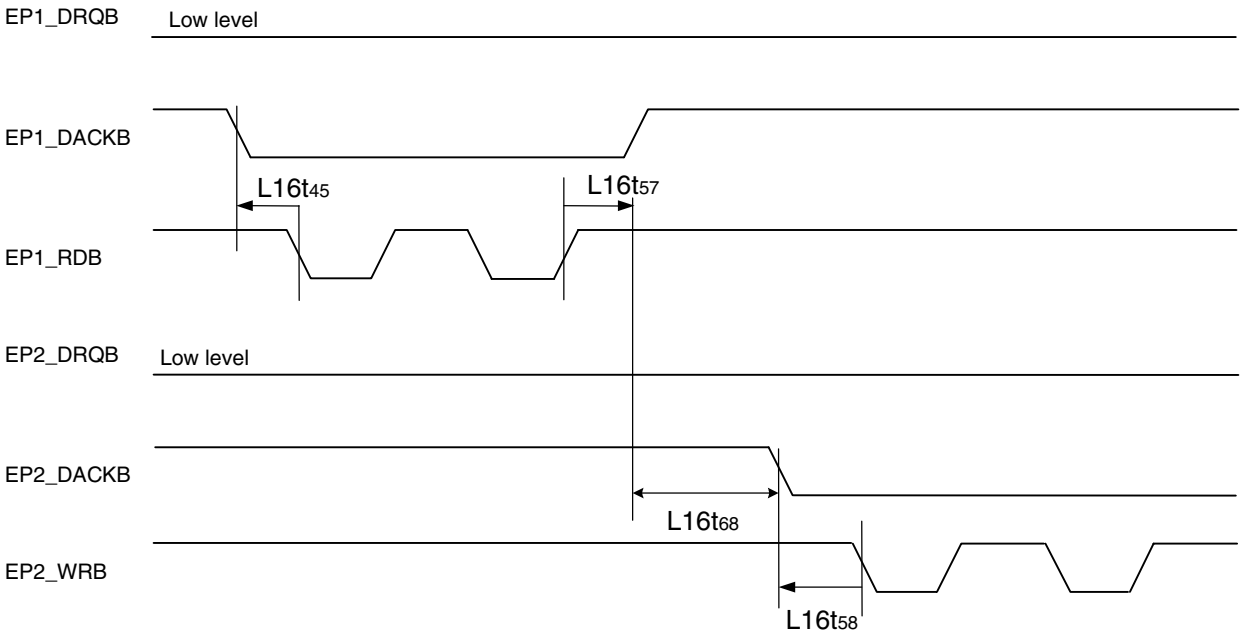
(If EP1_TCB is input when retransmission is executed)



(e) External local bus 16-bit mode DMA EP1_Read transfer vs. EP2_Write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L16T68	EP1_RDB vs. EP2_WRB command inactive time	34		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).



(2) External local bus 8-bit mode

(a) External local bus 8-bit mode DMA single mode read transfer timing

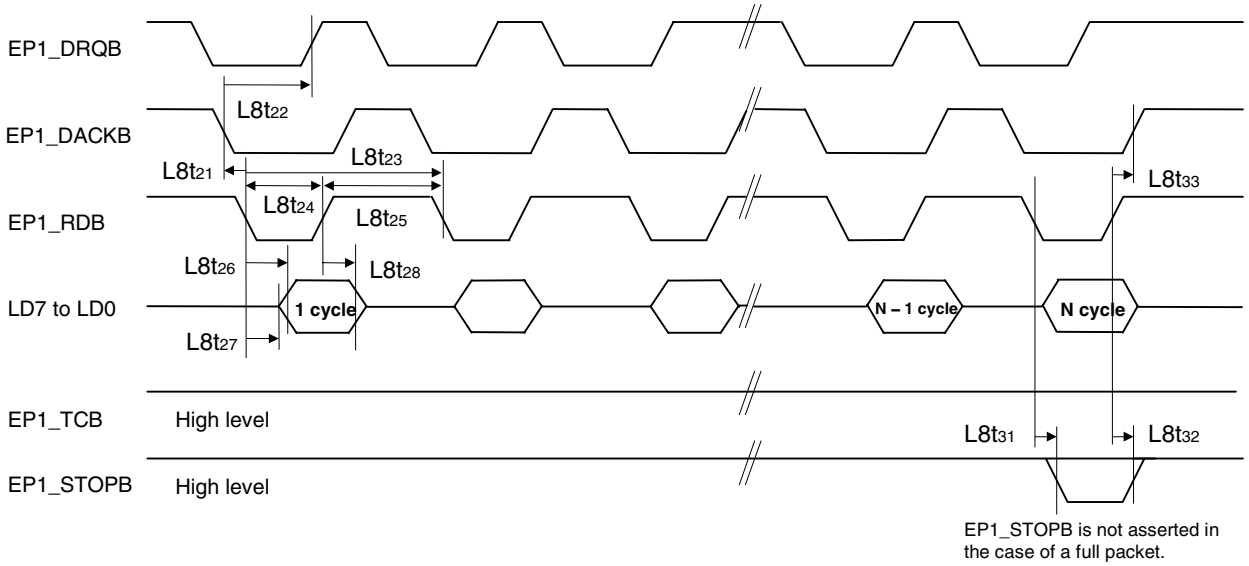
Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T21	DMA request acknowledge setup time (EP1_RDB↓)	0		∞	ns
L8T22	DMA request off time 1 (EP1_DACKB↓)	–		10	ns
L8T23	DMA single mode read transfer cycle time	91		∞	ns
L8T24	Read command width	57		∞	ns
L8T25	Read command inactive time	34		∞	ns
L8T26	Read data delay time (EP1_RDB↓)	–		57	ns
L8T27	Buffer direction change time (EP1_RDB↓)	–		14	ns
L8T28	Read data hold time (EP1_RDB↑)	4		–	ns
L8T31	EP1_STOPB delay time (EP1_RDB↓)	–		15	ns
L8T32	EP1_STOPB delay time (EP1_RDB↑)	3		–	ns
L8T33	DMA request acknowledge hold time (EP1_RDB↑)	0		∞	ns
L8T34	Undefined	–		–	ns

Remarks 1. Use of EP1_TCB is prohibited in the 8-bit external local bus mode. Clamp this signal to the inactive status.

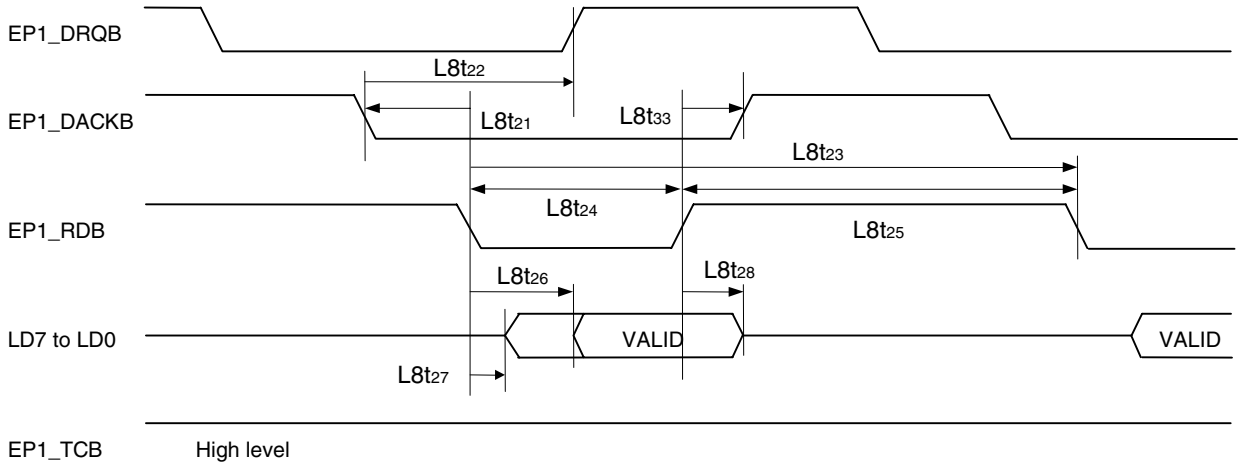
2. LD15 to 8 are undefined in the 8-bit external local bus mode (these signals are invalid when input and undefined when output).

3. It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

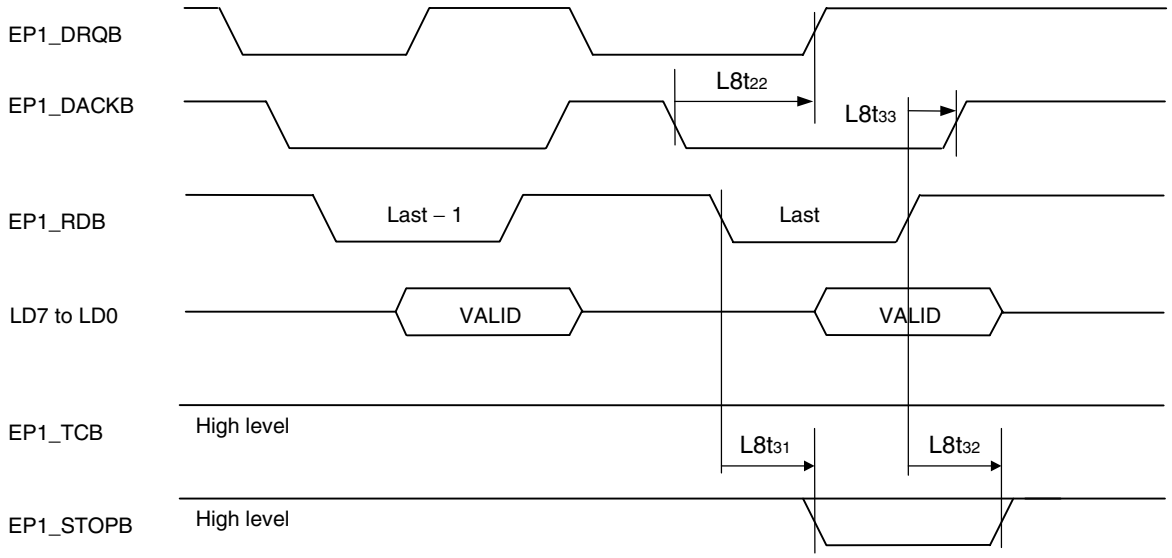
(Overall)



(Start timing)



(End timing)



EP1_STOPB is not asserted in the case of a full packet.

(b) External local bus 8-bit mode DMA single mode write transfer

Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T35	DMA request acknowledge setup time (EP2_WRB↓)	0		∞	ns
L8T36	DMA request off time 1 (EP2_DACKB↓)	–		54[Note]	ns
L8T37	DMA single mode write transfer cycle time	88		∞	ns
L8T38	Write command width	54		∞	ns
L8T39	Write command inactive time	34		∞	ns
L8T40	Write data setup time (EP2_WRB↑)	10		∞	ns
L8T41	Write data hold time (EP2_WRB↑)	0		∞	ns
L8T44	DMA request acknowledge hold time (EP2_WRB↑)	0		∞	ns

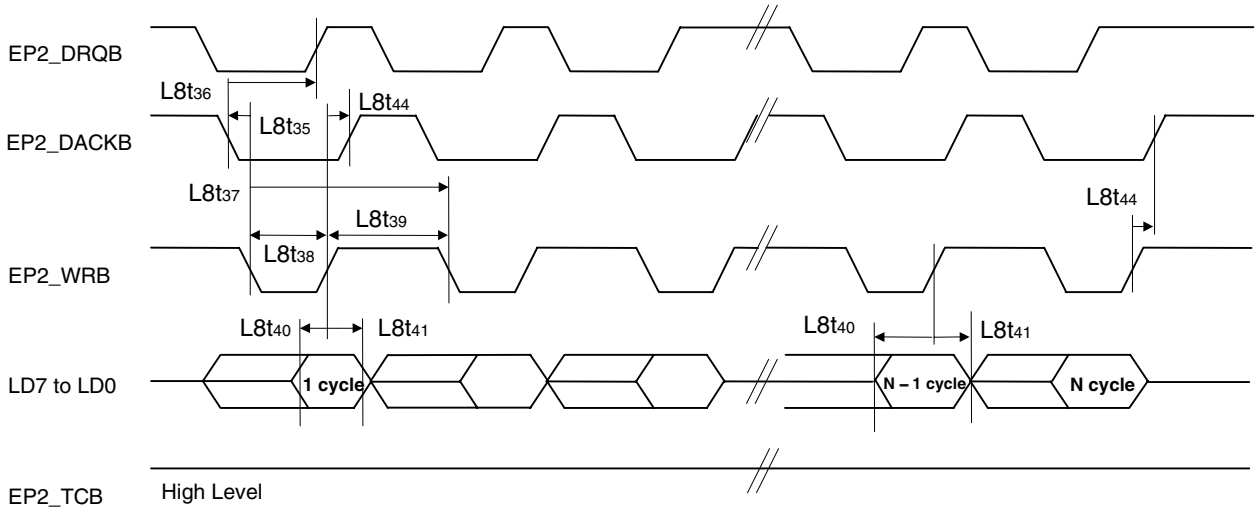
Remarks 1. Use of EP1_TCB is prohibited in the 8-bit external local bus mode. Clamp this signal to the inactive status.

2. LD15 to 8 are undefined in the 8-bit external local bus mode (these signals are invalid when input and undefined when output).

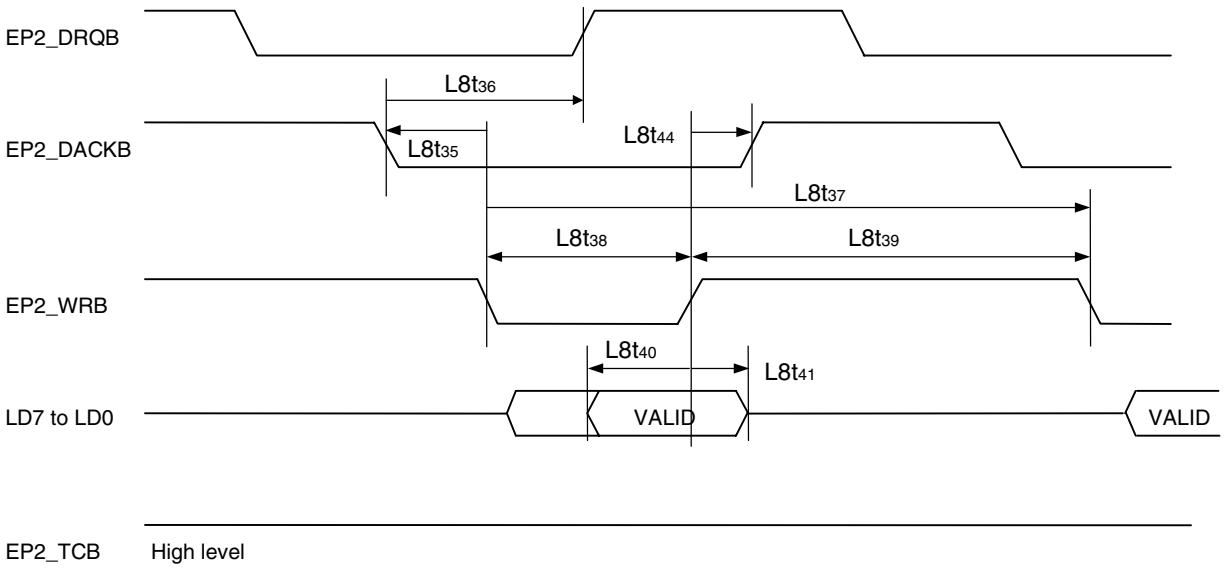
3. It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

Note The difference in specifications when compared with L8T22 is that BIU processing is performed for EP1 and that EPC2 processing is performed for EP2.

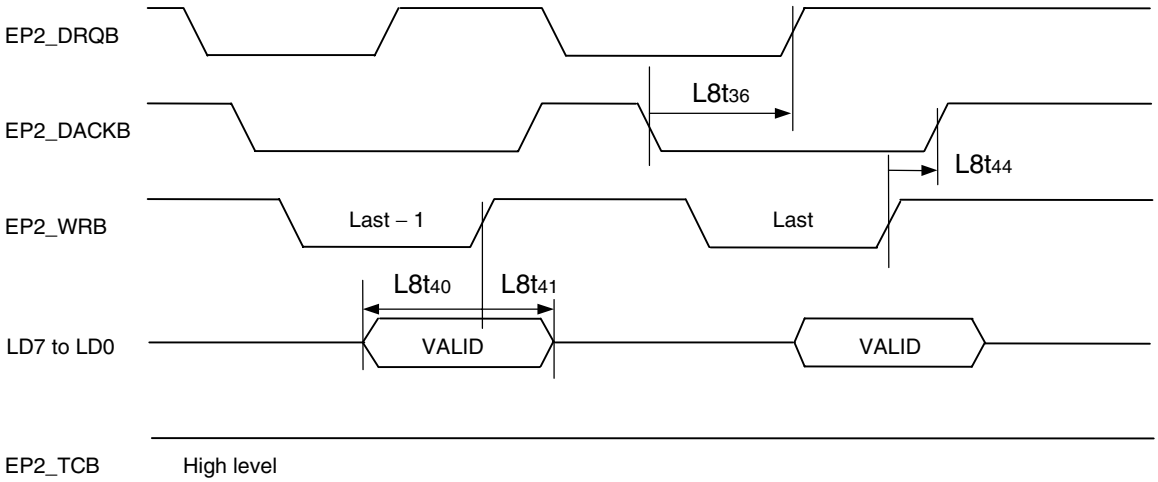
(Overall)



(Start timing)



(End timing)



(c) External local bus 8-bit mode DMA demand read transfer timing

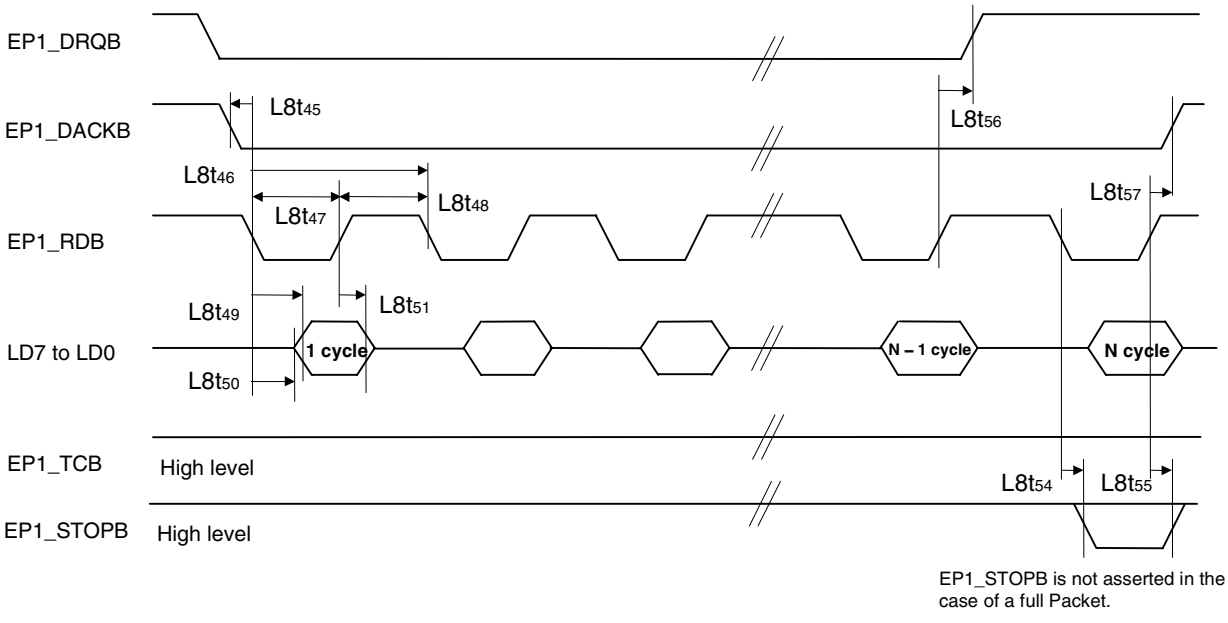
Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T45	DMA request acknowledge setup time (EP1_RDB↓)	0		∞	ns
L8T46	DMA demand mode read transfer cycle time	90		∞	ns
L8T47	Read command width	56		∞	ns
L8T48	Read command inactive time	34		∞	ns
L8T49	Read data delay time (EP1_RDB↓)	–		56	ns
L8T50	Buffer direction change time (EP1_RDB↓)	–		14	ns
L8T51	Read data hold time (EP1_RDB↑)	4		–	ns
L8T54	EP1_STOPB delay time (EP1_RDB↓)	–		15	ns
L8T55	EP1_STOPB delay time (EP1_RDB↑)	3		–	ns
L8T56	DMA request off time (EP1_RDB↑)	–		60	ns
L8T57	DMA request acknowledge hold time (EP1_RDB↑)	0		∞	ns

Remarks 1. Use of EP1_TCB is prohibited in the 8-bit external local bus mode. Clamp this signal to the inactive status.

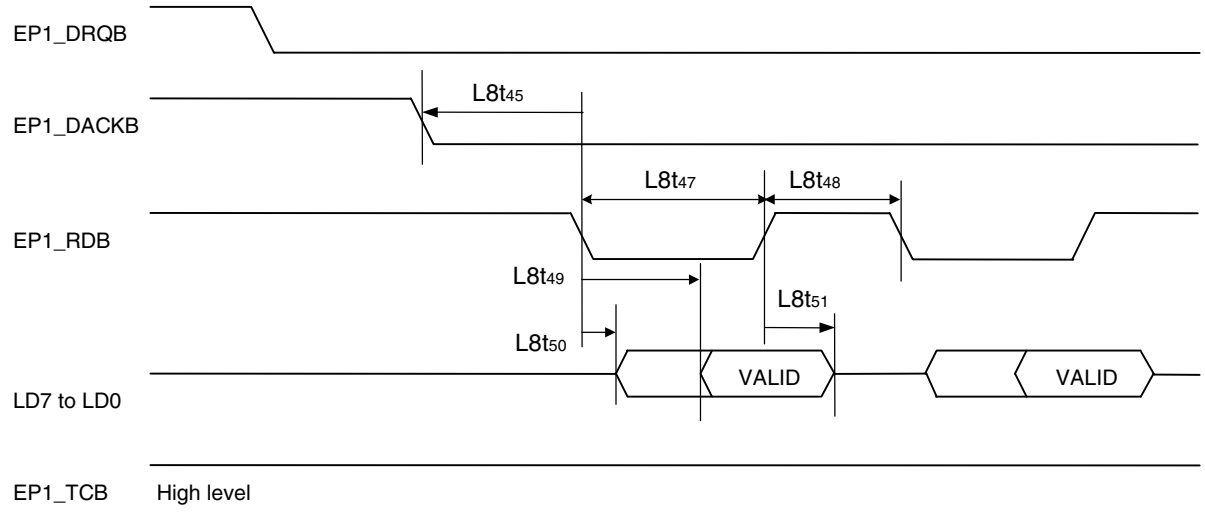
2. LD15 to 8 are undefined in the 8-bit external local bus mode (these signals are invalid when input and undefined when output).

3. It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

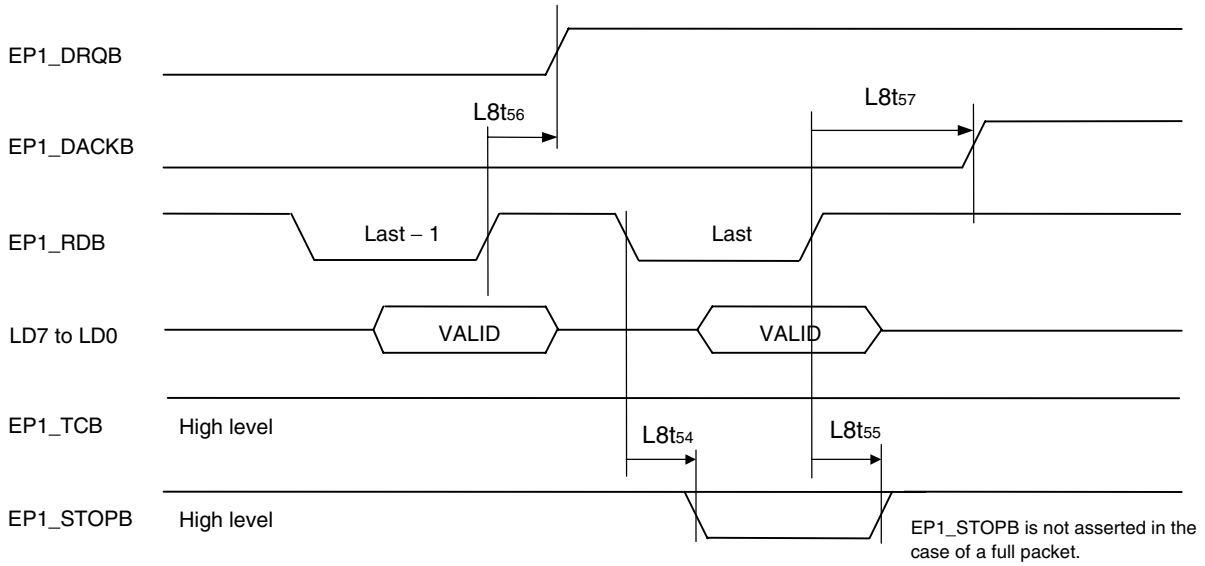
(Overall)



(Start timing)



(End timing)



(d) External local bus 8-bit mode DMA demand write transfer timing

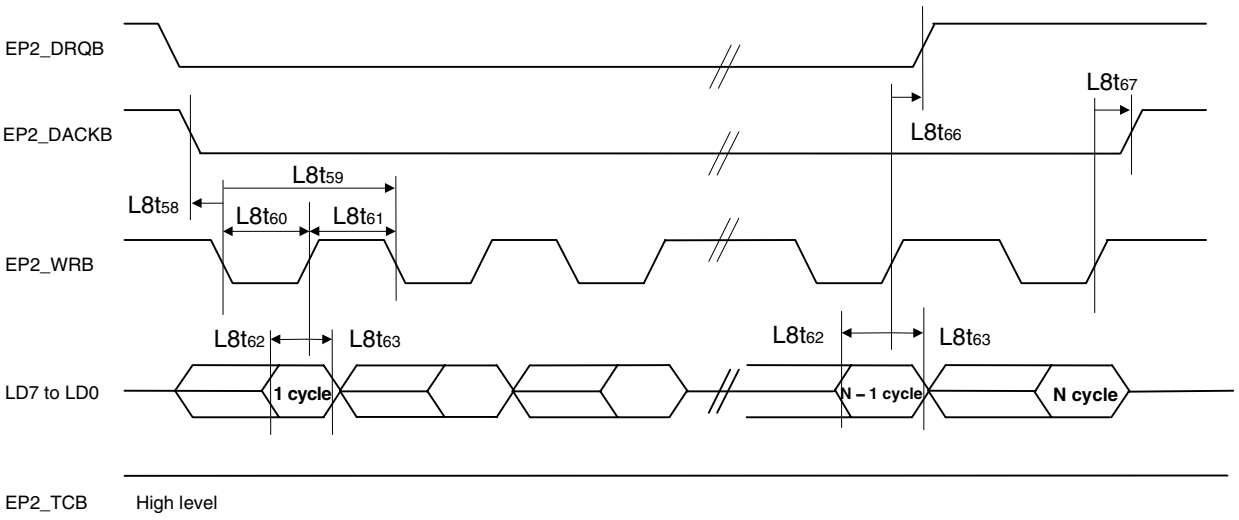
Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T58	DMA request acknowledge setup time (EP2_WRB↓)	0		∞	ns
L8T59	DMA demand mode write transfer cycle time	72		∞	ns
L8T60	Write command width	38		∞	ns
L8T61	Write command inactive time	34		∞	ns
L8T62	Write data setup time (EP2_WRB↑)	10		∞	ns
L8T63	Write data hold time (EP2_WRB↑)	0		∞	ns
L8T66	DMA request off time (EP2_WRB↑)	–		60	ns
L8T67	DMA request acknowledge hold time (EP2_WRB↑)	0		∞	ns

Remarks 1. Use of EP1_TCB is prohibited in the 8-bit external local bus mode. Clamp this signal to the inactive status.

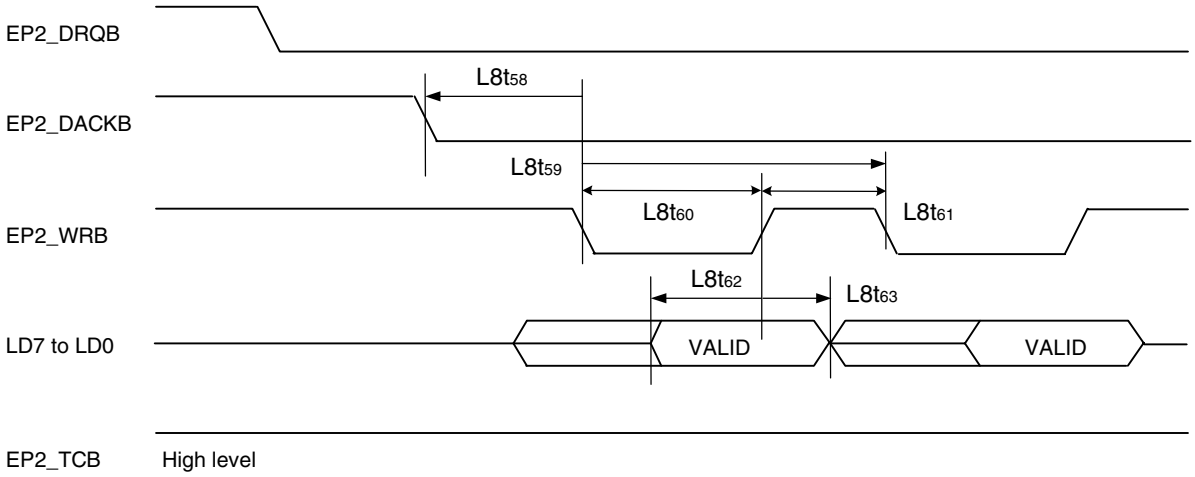
2. LD15 to 8 are undefined in the 8-bit external local bus mode (these signals are invalid when input and undefined when output).

3. It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).

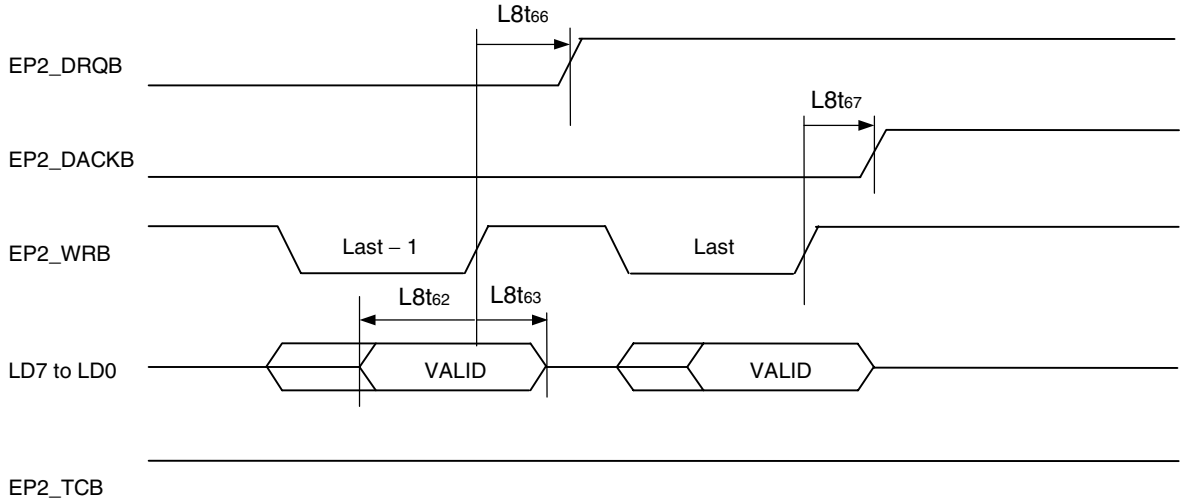
(Overall)



(Start timing)



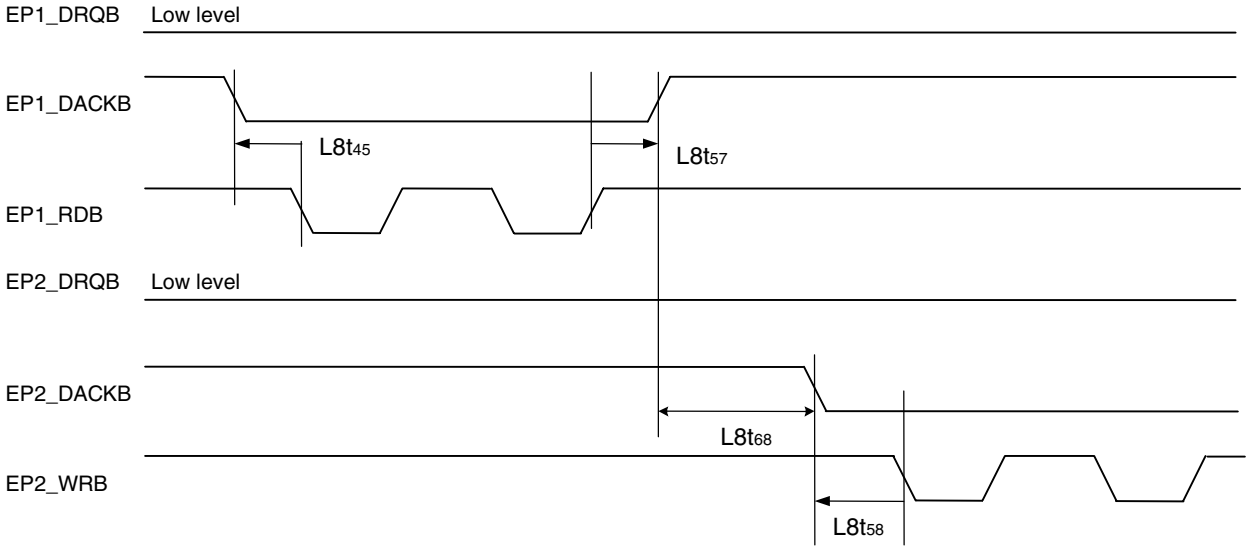
(End timing)



(e) External local bus 8-bit mode DMA EP1_Read transfer vs. EP2_Write transfer timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
L8T68	EP1_RDB vs. EP2_WRB command inactive time	34		∞	ns

Remark It is assumed that the external pin capacitance is 15 pF (data bus = 50 pF).



2.6.5 USB interface timing

Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed source electrical characteristics					
Rise time	T_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time	T_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	T_{FRFM}	(T_{FR}/T_{FF})	90	111.11	%
Full-speed data rate for hubs and devices that are high-speed capable	$T_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mb/s
Frame interval	T_{FRAME}		0.9995	1.0005	ms
Consecutive frame interval jitter	T_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance):					
To next transition	T_{DJ1}		−3.5	3.5	ns
For paired transitions	T_{DJ2}		−4.0	4.0	ns
Source jitter for differential transition to SE0 transition	T_{FDEOP}		−2	5	ns
Receiver jitter:					
To next transition	T_{JR1}		−18.5	18.5	ns
For paired transitions	T_{JR2}		−9	9	ns
Source SE0 interval of EOP	T_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP	T_{FEOPR}		82		ns
Width of SE0 interval during differential transition	T_{FST}			14	ns
High-speed source electrical characteristics					
Rise time (10% to 90%)	T_{HSR}		500		ps
Fall time (10% to 90%)	T_{HSF}		500		ps
Driver waveform requirements	See Figure 2-6				
High-speed data rate	T_{HSDRAT}		479.760	480.240	Mb/s
Microframe interval	T_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	T_{HSRFI}			4 high-speed	Bit times
Data source jitter	See Figure 2-6.				
Receiver jitter tolerance	See Figure 2-4.				

Parameter	Symbol	Conditions	Min.	Max.	Unit
Device event timing					
Time from internal power good to device pulling D+/D– beyond V_{IHZ} (min.) (signaling attach)	T_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach	T_{ATTDB}			100	ms
Inter-packet delay (for low-/full-speed)	T_{IPD}		2		Bit times
Inter-packet delay for device response w/detachable cable for low-/full-speed	$T_{RSPIPD1}$			6.5	Bit times
High-speed detection start time from suspend	T_{SCA}		2.5		μs
Sample time for suspend vs. reset	T_{CSR}		100	875	μs
Power down under suspend	T_{SUS}			10	ms
SUSPEND set time (SPNDOUT)	T_{SSP}		0	–	
SUSPEND clear time (RSUMOUT)	T_{CSP}		0	–	
Reversion time from suspend to high-speed	T_{RHS}			1.333	μs
SUSPEND setup time (RSUMIN)	T_{SRW}		0	–	
RSUMIN active pulse width	T_{RWP}		1	15	ms
Drive chirp K width	T_{CKO}		1		ms
Finish chirp K assertion	T_{FCA}			7	ms
Start sequencing chirp K-J-K-J-K-J	T_{SSC}			100	μs
Finish sequencing chirp K-J	T_{FSC}		–500	–100	μs
Detect sequencing chirp K-J width	T_{CSI}		2.5		μs
Sample time for sequencing chirp	T_{SCS}		1.0	2.5	ms
Reversion time to high-speed	T_{RHA}			500	μs
High-speed detection start time	T_{HDS}		2.5	3000	μs
Reset completed time	T_{DRS}		10		ms

Figure 2-6. Transmit Waveform for Transceiver at D+/D–

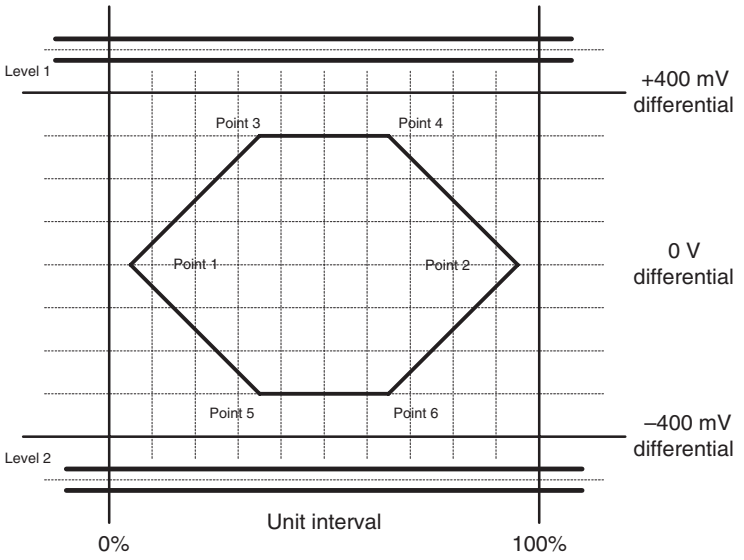
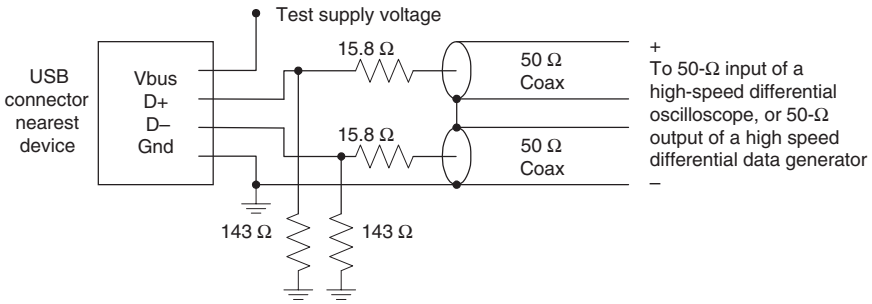
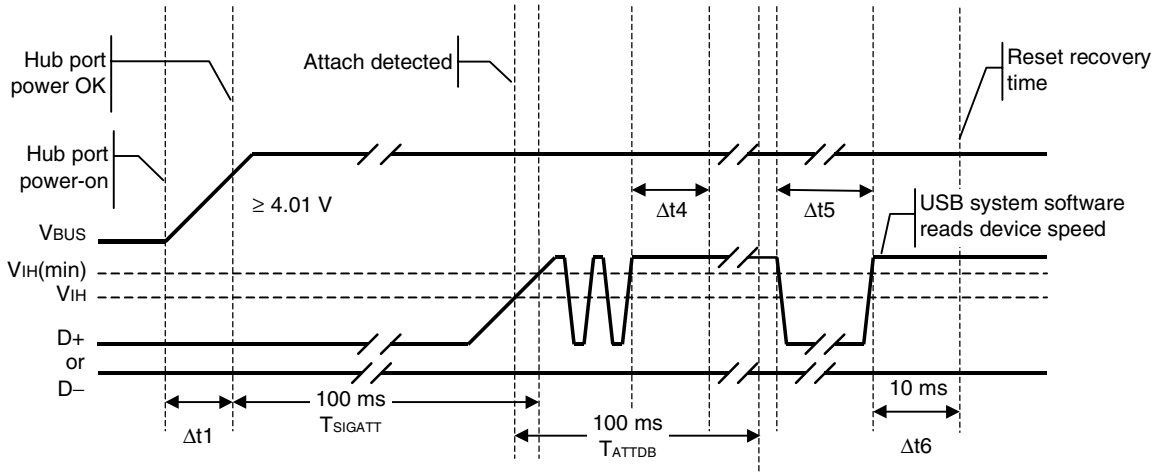


Figure 2-7. Transmitter Measurement Fixtures



(1) Power-on and connection events

Figure 2-8. Power-on and Connection Event Timing



(2) USB signals

Figure 2-9. USB Differential Data Jitter for Full-Speed

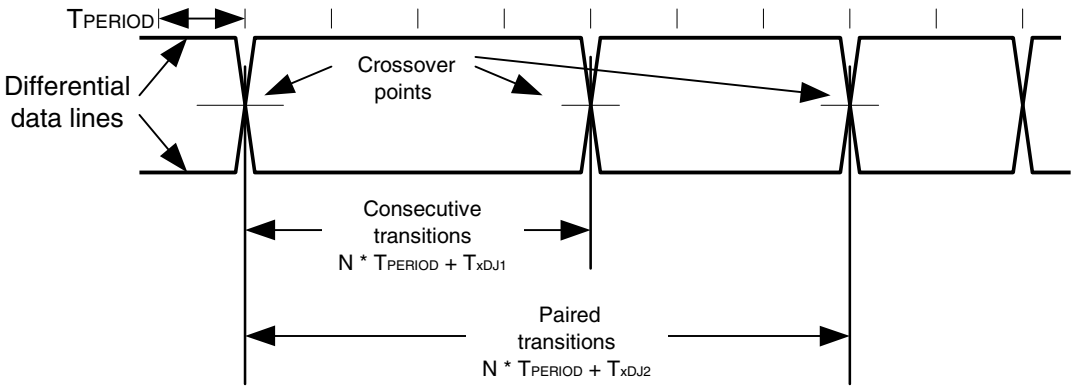


Figure 2-10. USB Differential-to-EOP Transition Skew and EOP Width for Full-Speed

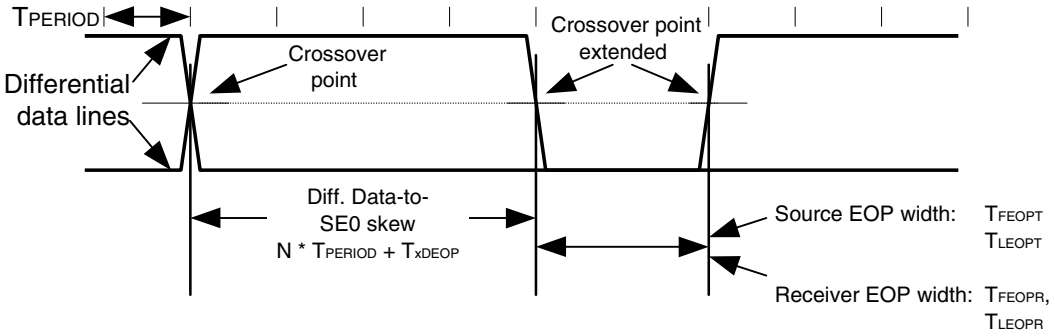
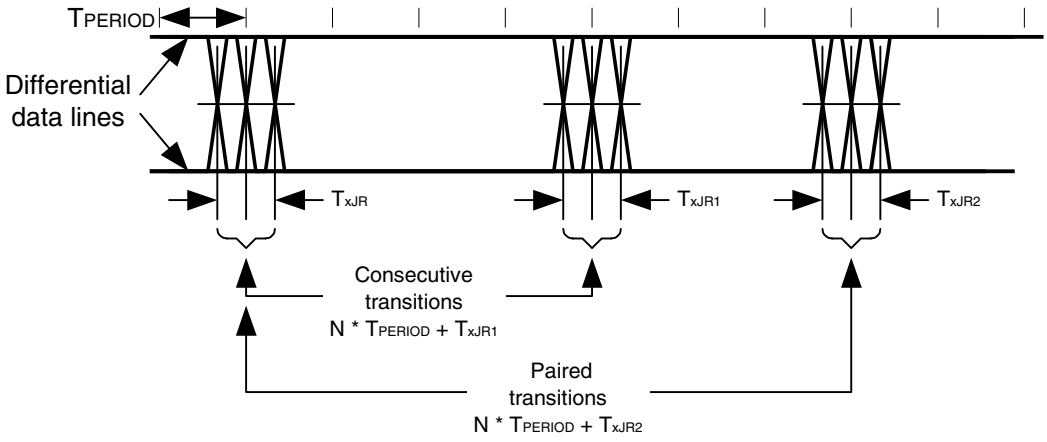


Figure 2-11. USB Receiver Jitter Tolerance for Full-Speed

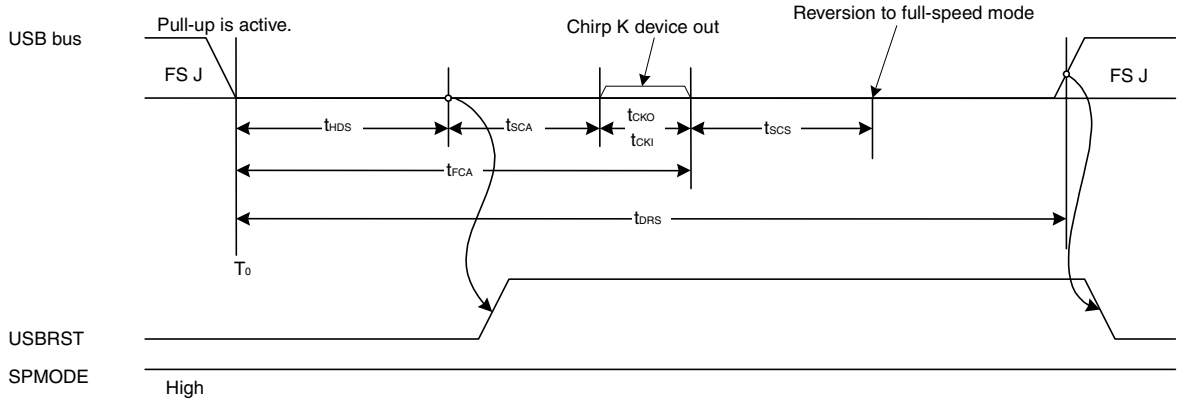


(3) USB connection sequence on USB1.1 bus

The PHY core implemented on the μPD720122 automatically determines the Up port.

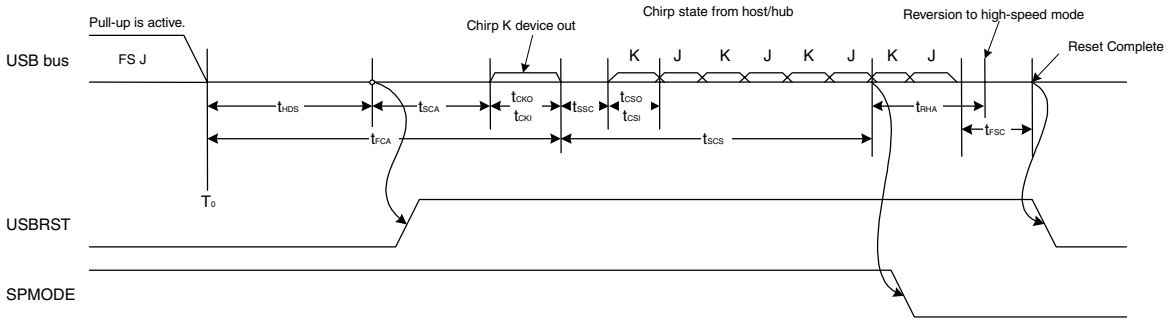
Check the SP_MODE bit (SP_MODE) of the Int Status 2 register after an EPC2_STG bus reset interrupt has occurred to determine whether the USB is connected to FS or HS.

Figure 2-12. USB Connection Sequence on USB 1.1 Bus



(4) USB connection sequence on USB 2.0 bus

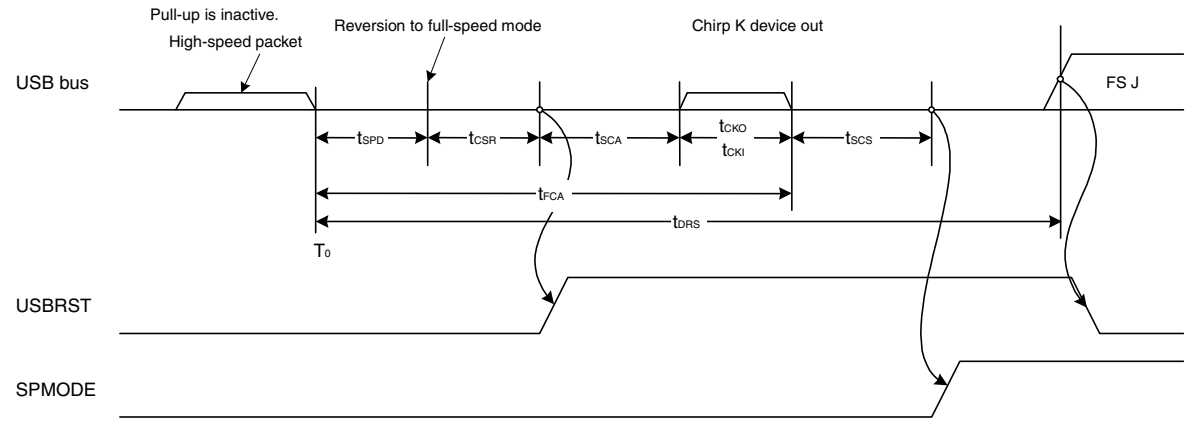
Figure 2-13. USB Connection Sequence on USB 2.0 Bus



(5) Bus reset sequence (1)

The bus reset sequence when connected to a USB 1.1 bus is shown below.

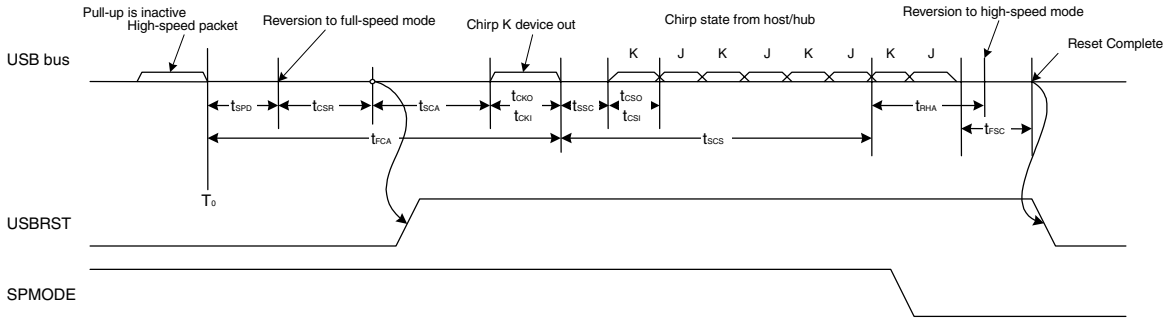
Figure 2-14. Bus Reset Sequence (1)



(6) Bus reset sequence (2)

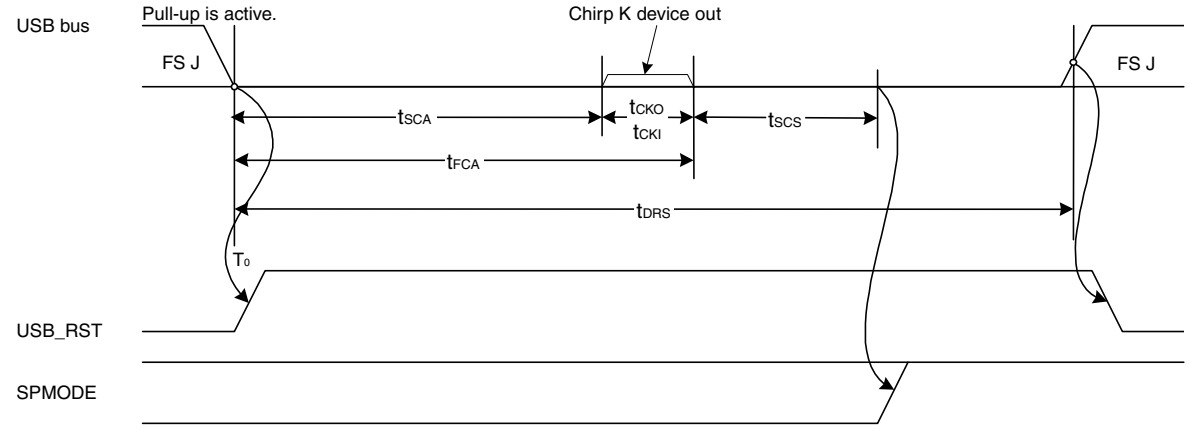
The bus reset sequence when connected to a USB 2.0 bus is shown below.

Figure 2-15. Bus Reset Sequence (2)



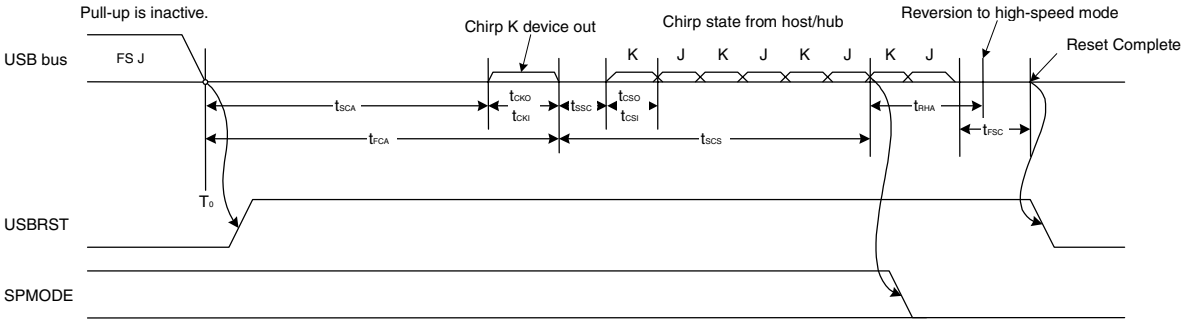
(7) USB reset from suspend state (1)

Figure 2-16. USB Reset from Suspend State (1)



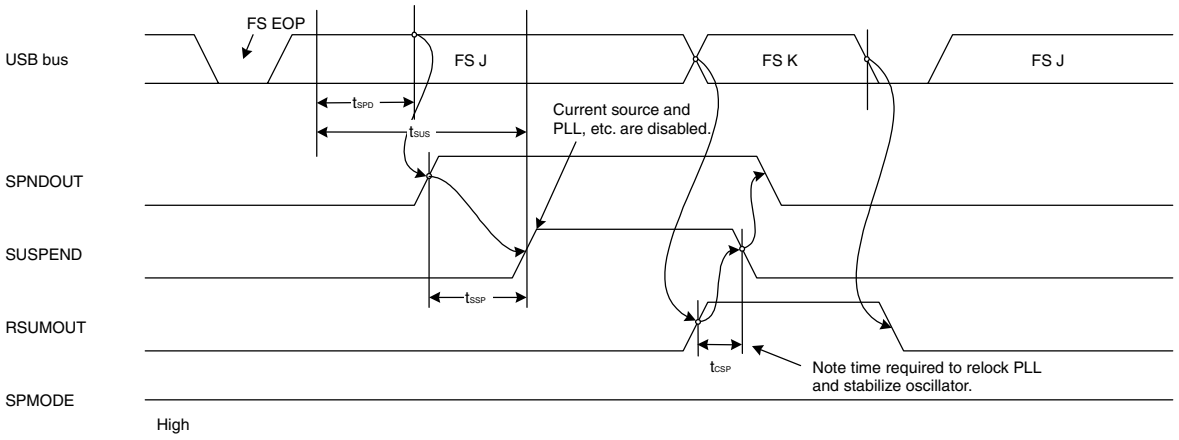
(8) USB reset from suspend state (2)

Figure 2-17. USB Reset from Suspend State (2)



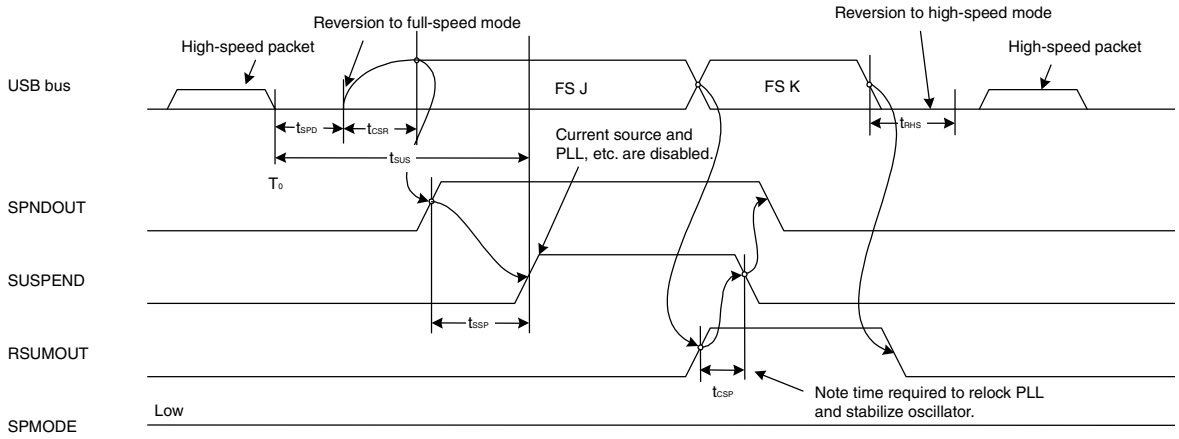
(9) Suspend and resume on USB1.1 bus

Figure 2-18. Suspend and Resume on USB 1.1 Bus



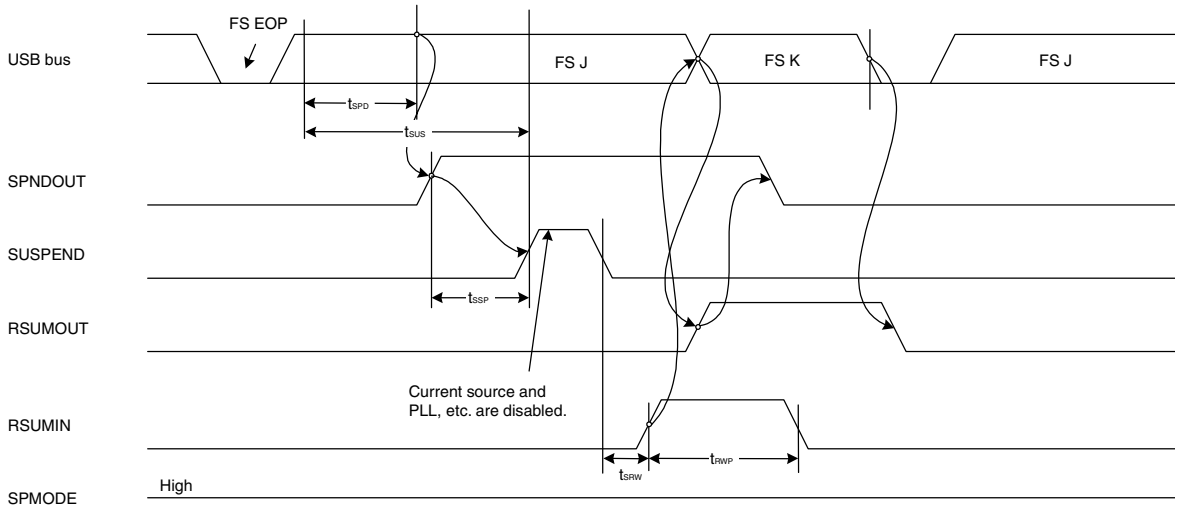
(10) Suspend and resume on USB2.0 bus

Figure 2-19. Suspend and Resume on USB 2.0 Bus



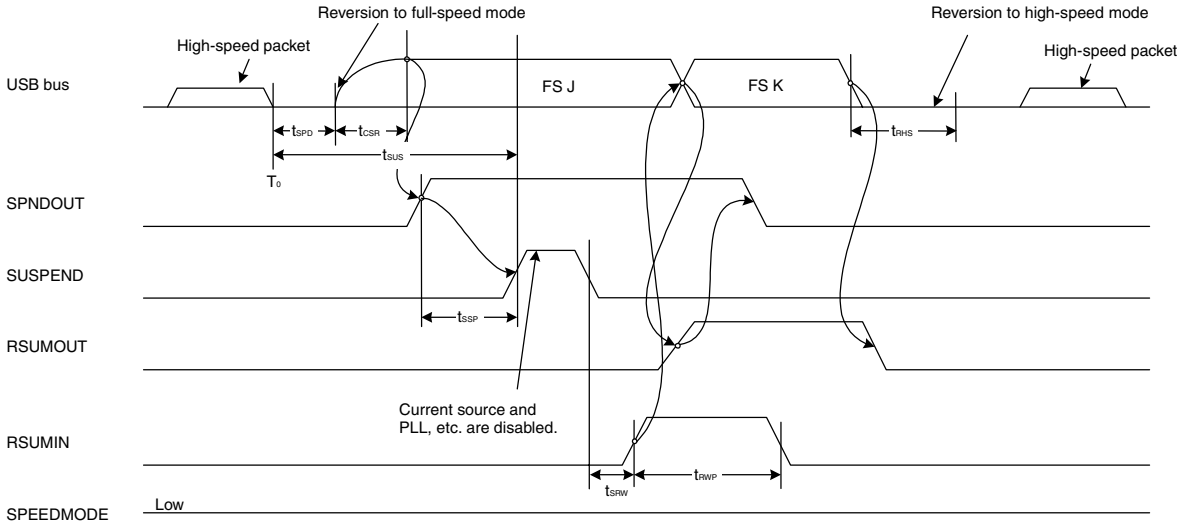
(11) Remote wakeup on USB1.1

Figure 2-20. Remote Wakeup on USB 1.1



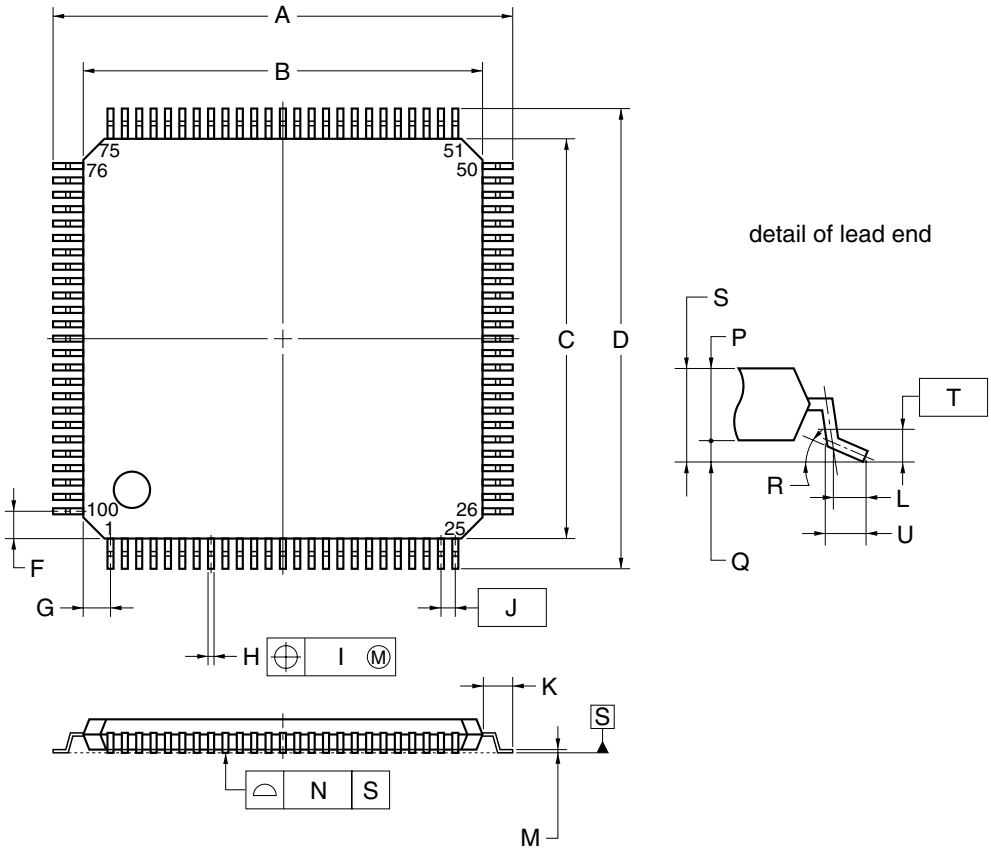
(12) Remote wakeup on USB2.0

Figure 2-21. Remote Wakeup on USB 2.0



3. PACKAGE DRAWING

★ **100-PIN PLASTIC TQFP (FINE PITCH) (14x14)**



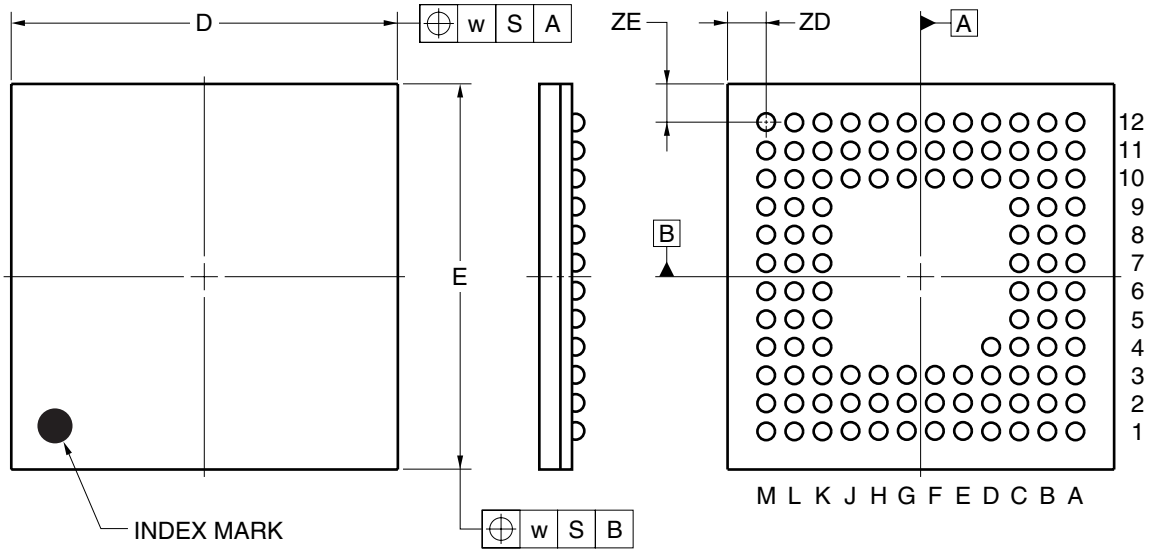
NOTE

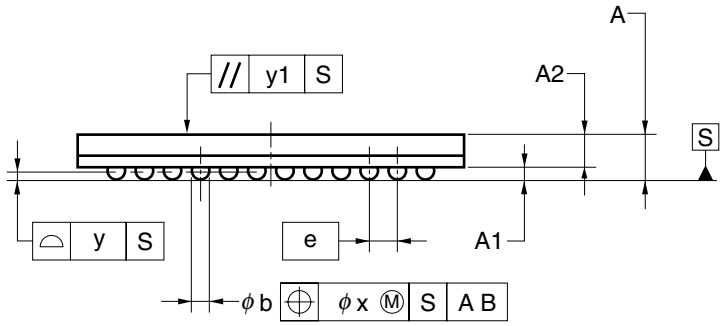
Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.2
C	14.0±0.2
D	16.0±0.2
F	1.0
G	1.0
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P100GC-50-9EU

109-PIN PLASTIC FBGA (11x11)





(UNIT:mm)

ITEM	DIMENSIONS
D	11.00±0.10
E	11.00±0.10
w	0.20
A	1.28±0.10
A1	0.35±0.06
A2	0.93
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.10
ZE	1.10

P109F1-80-DN2

4. RECOMMENDED SOLDERING CONDITIONS

The μPD720122 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact your NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

• μ PD720122GC-9EU : 100-pin plastic TQFP (Fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

• μ PD720122F1-GN2 : 109-pin plastic FBGA (11 × 11)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-3
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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USB logo is a trademark of USB Implementers Forum, Inc.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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