GDC21D701C
(Video Display Processor)

Version 1.0

LG Semicon

The information contained herein is subject to change without notice.

The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by LG for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of LG or others.

These LG products are intended for usage in general electronic equipment (office equipment, communication equipment, measuring equipment, domestic electrification, etc.).
Please make sure that you consult with us before you use these LG products in equipment which require high quality and/or reliability, and in equipment which could have major impact to the welfare of human life (atomic energy control, airplane, spaceship, traffic signal, combustion control, all types of safety devices, etc.). LG cannot accept liability to any damage which may occur in case these LG products were used in the mentioned equipment without prior consultation with LG.

Purchase of LG I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

TABLE OF CONTENTS

1. General Description

The Video Display Processor(GDC21D701C) converts digital image data into analog image data for HDTV display. The VDP receives all Grand Alliance input image formats(including HD and SD) and converts them into 1080x1920 60I HD display formats. The VDP also converts digital NTSC image format(480x768 60I, 480x768 60P) or VGA input format(480x640 60P or 768x1024 60P) into HD display format. During the display format conversion, the VDP converts 4:2:0 or 4:2:2 chrominance format into 4:4:4 chrominance one. The VDP supports bit-mapped-type On-screen Display(OSD) function, and OSD data can be loaded by DMA operation.

In the GBR display mode, the VDP converts YCbCr color space into GBR color space using the digital dematrix function. The VDP has two sets of user programmable Lookup Tables for customer control and special video effects. Finally, the VDP converts digital GBR/YCbCr signal into analog GBR/YPbPr signal and generates associated video sync signals for high-definition display.

The VDP can directly interface with MPEG2 MP@HL Video Decoder(GDC21D401B).

2. Features

Format Conversion

- Supports all HD, SD(4:2:0), and digital NTSC(4:2:2) and VGA(4:2:2) input format
  - -720x1280(60P,30P,24P)
  - -1080x1920(60I,30P,24P)
  - -480x704(60P,30P,24P,60I)
  - -480x720(60P,30P,24P,60I)
  - -480x640(60P,30P,24P,60I)
  - -480x768(60I, 60P) : digital NTSC and double scanned NTSC
  - -480x720(60I) : NTSC
  - -480x640(60P) : VGA
  - -768x1024(60P) : VGA
- 1080x1920(60I) Interlaced display format
- 3-D de-interlacing
  - -Motion compensated de-interlacing
  - -Use 3 field memories
  - -Applied to NTSC 60I / SD 60I input
- Chrominance format conversion
  - -4:2:0 => 4:4:4(ATV)
  - -4:2:2 => 4:4:4(digital NTSC or VGA)
- 9-tap FIR filter for horizontal filtering (Luminance part only)
- 2-tap Linear Interpolation filter for vertical filtering

PIP & Display Control

- Supports ATV main display and NTSC PIP and vice versa
- Supports two selectable PIP sizes
- Supports programmable PIP positions
- Supports 4:3 display and 16:9 display for 4:3 input format(SD and NTSC case)
- x4 zoom at 9 selectable positions for HD input formats
- Multi-PIP display(16 Multi-PIPs)
- Freeze function

On-screen Display

- Display Format : 1080 x 1920(4:4:4, 60I, 74.25MHz)
- Supports transparency and 16-level blending
- Multiple layers : cursor, two OSD layers above video
- 2, 4, 8 bitmap bits per cell
- Top and bottom fields share the same OSD data
- Linked-list memory management
- Supports full OSD screen
- Supports maximum four OSD buffers
- 32 x 32-pixel 4-color cursor movable all over the screen
- Animation function

Color Space Conversion

- Supports programmable color space conversion function (including YCbCr => GBR, YCbCr => YPbPr)
- Three channels, 8-bit color space conversion
- Uses 9 parallel multipliers to process high resolution image
- Uses 9 10-bit matrix coefficients(integer range: 1023/2 ~ -1024/2)

Customer Controls

- Two swappable sets of RGB tables
- 8-bit 256-level Lookup Table (RAM)

Output Formats

- GBR / YCbCr 10-bit digital output
- GBR / YPbPr analog output (10-bit D/A conversion)
- Provides external sync signals - HDOUT_N, VDOUT_N
- Supports SMPTE 274M digital/analog output formats
- Provides 7 built-in test patterns

Host Interface (Use digital output ports)

- Supports 16-bit host bus interface
- Supports DMA operation(up to 36Mbyte/sec) for OSD data loading.
- Supports I^2C Interface

3. Pin Description

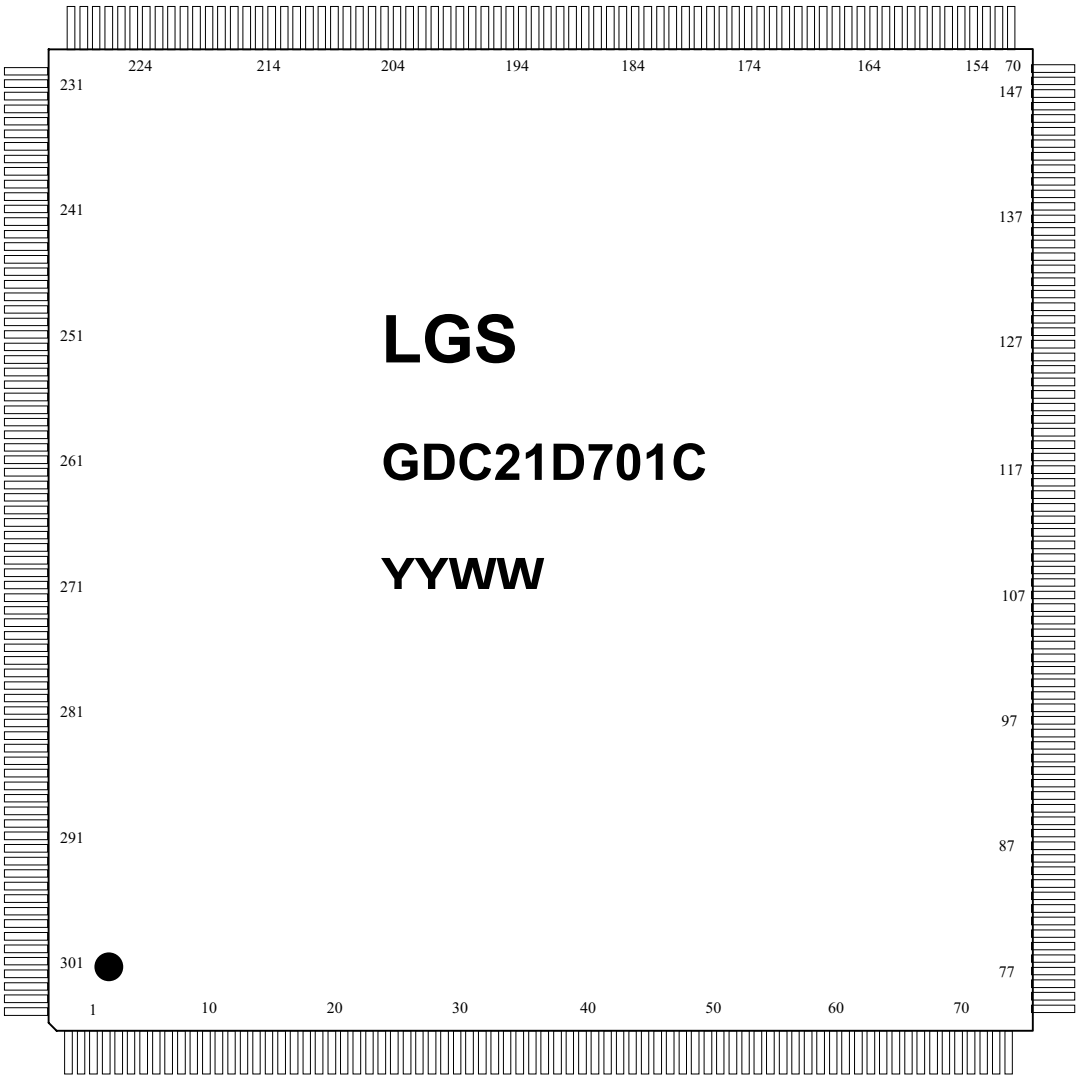


Figure 1. Pin Configuration

(Package: 304 PQ2)

NAME	PIN	TYPE	DESCRIPTIONS
Clocks			
CLKNV	2	I	NTSC/VGA Interface Clock. Its operating clock frequency depends on the NV_MODE input and it can be 14MHz, 25MHz, 28MHz, or 65MHz.
CLKVD	221	I	Video Decoder Interface Clock. Its operating clock frequency is the same as that of Video Decoder and it can be up to 54MHz.
CLK74	224	I	VDP Display Clock. Its operating clock frequency can be 74.25MHz or 74.175MHz.
CLK74IN	161	I	Additional Clock for SDRAM Interface. This clock outputs clk74out signal for SDRAM interface. Its operating clock frequency is the same as that of VDP display clock.
CLK74OUT	159	O	Additional Clock for SDRAM Interface. For stable data transfer between SDRAM and VDP, VDP provides the additional clock for SDRAM interface. Its operating clock frequency is the same as that of clk74in.
Resets			
RESET_N	235	I	Global Reset(active-low). This signal asynchronously resets the VDP IC.
RESETS_N	236	I	Display Sync Reset. This signal asynchronously resets the display sync signal.
I^2C-Bus Interface			
SCL	104	I	I^2C-Bus Serial Clock. The maximum operation clock is 400KHz.
SDA	102	I/O	I^2C-Bus Serial Data. Bi-directional data.
SDRAM Interface			
SDRAM_DATA [63:0]	46,45,43,42,41,39,38, 36,35,34,33,31,30,28, 27,26,25,23,22,21,20, 18,17,15,14,13,12,10, 9,7,6,4,282,281,280, 278,277,275,274,273, 270,269,268,265,264, 263,261,260,259,257, 256,254,253,252,251, 249,248,246,245,244, 243,241,240,238	I/O	SDRAM Data Bus. Bi-directional data.
SDRAM_ADDR [10:0]	297,296,294,293,292, 291,289,288,287,286, 284	O	SDRAM Address.
BANK	298	O	SDRAM Bank Selection Signal.
WE_N	300	O	SDRAM Write Enable Signal(active-low).
CAS_N	301	O	SDRAM Column Address Strobe Signal(active-low).
RAS_N	302	O	SDRAM Row Address Strobe Signal(active-low).
CS_N	303	O	SDRAM Chip Selection Signal(active-low).

Pin Description*(continued)*

NAME	PIN	TYPE	DESCRIPTION
Video Decoder Interface			
PDATA[31:0]	172,173,175,176,178, 179,181,182,183,185, 186,187,188,190,191, 192,194,195,197,198, 200,201,203,204,206, 207,209,210,212,213, 215,216	I	Video Decoder Output Data. These ports can be directly connected to the Video Decoder PDATA output.
PSTR[1:0]	218,219	I	Picture Structure Information. These ports can be directly connected to the Video Decoder PSTR output.
PDWIN	226	I	Picture Data Window. This port can be directly connected to the Video Decoder PDWIN output.
FFP_N	230	I	First Field Parity(active-low). This port can be directly connected to the Video Decoder FFPN output.
MBFI	231	I	Macro Block IDCT Type. '0' means frame IDCT and '1' means field IDCT. This port can be directly connected to the Video Decoder MBFI output.
MBWIN	233	I	Macro Block Data Window. This port can be directly connected to the Video Decoder MBCLK output.
SWIN	234	I	Slice Data Window. This port can be directly connected to the Video Decoder SCLK output.
D_INFO_WIN	227	I	Picture Format Data Window. This port can be directly connected to the Video Decoder D_INFO_WIN output.
DIS_INFO	228	I	Picture Format Data. The picture information is coded in serial format and this port can be directly connected to the Video Decoder DIS_INFO output.
P_FRM	167	I	Progressive Frame Information. This port can be directly connected to the Video Decoder P_FRM output. If not, this port should be connected to VSS.
P_WAIT	170	O	PDATA Wait Signal. This port can be directly connected to the Video Decoder P_WAIT input.
NTSC/VGA Interface			
NV_Y[7:0]	58,57,55,54,52,51,49, 48	I	Luminance Data Input of NTSC or VGA.(4:2:2 format)
NV_C[7:0]	70,69,67,66,64,63,61, 60	I	Chrominance Data Input of NTSC or VGA.(4:2:2 format)
NTSC_VGA	72	I	Select NTSC or VGA Input. NTSC input set to "0" and VGA input set to "1".
NV_MODE	73	I	Select NTSC and VGA Input Mode. NTSC input or VGA input set to "0" and double scan NTSC or SVGA input set to "1".
NV_HD_N	74	I	Horizontal Drive or Horizontal Sync Input.
NV_VD_N	75	I	Vertical Drive or Vertical Sync Input.
NV_FIELD	91	I	NTSC Field Signal. It is set to '0' that present input is top field and set to "1" that is bottom field. This is used in the NTSC input mode.

Pin Description*(continued)*

NAME	PIN	TYPE	DESCRIPTION
Display			
ROUT/PROUT	82	O	Analog Output - Red /Pr Signal.
GOUT/YOUT	84	O	Analog Output - Green /Y Signal.
BOUT/PBOUT	86	O	Analog Output - Blue /Pb Signal.
ADJ	80	I	Full-scale Adjustment. It controls the magnitude of analog video signal.
REF	78	I	Voltage Reference Input.
HDOUT_N	92	O	Horizontal Drive Output.
VDOUT_N	93	O	Vertical Drive Output.
HSYNCOUT_N	97	O	Horizontal Sync Output. This signal represents active data window.
VSYNCOUT_N	98	O	Vertical Sync Output. This signal represents active data window.
FIELDSYNC	99	O	Field SYNC Output. It is set to '1' that present display is top field and set to '0' that is bottom field. This port can be directly connected to the Video Decoder PIC_DIS_SYNC input.
H60_N	100	O	Clock Selection Signal. It is set to '0' that VDP requires 74.25MHz clock and set to '1' that VDP requires 74.175MHz clock.
RDOUT[9:0] / CRDOUT[9:0]	106,107,109,110,111, 113,114,116,89,95	I/O	10-bit Digital Output-Red/Cr Component. 74MHz data rate. These pins can be used by host interface signals
GDOUT[9:0] / YDOUT[9:0]	117,119,120,122,123, 125,126,128,142, 150	I/O	10-bit Digital Output–Green/Y Component. 74MHz data rate. These pins can be used by host interface signals
BDOUT[9:0] / CBDOUT[9:0]	129,131,133,134,135, 137,138,140,151,153	I/O	10-bit Digital Output-Blue/Cb Component. 74MHz data rate. These pins can be used by host interface signals
Host Bus Interface (Shared RGB Digital Outputs)			
HOST_SEL	76	I	Host Select Signal. It is set to "1" that digital output signals are activated for digital interface and set to "0" that host interface address and data signals are used in digital output ports.
D_STB_N	151	I	Data Strobe (active-low) : Asynchronous. Used by the host processor to access this chip. When D_STB_N signal is active, H_ADDR[8:1], H_DATA[15:0], and H_CS_N should be valid.
H_RW_N	150	I	Read/Write (active-low) : Asynchronous. The state of the signal defines the data transfer type. 0 = Write to the device 1= Read from the device
H_CS_N	142	I	Chip Selection (active-low). This signal is used to activate and access to the internal registers and memories of the GDC21D701C.
READY_TYPE	153	I	It is set to "1" that ready signal is active-high and set to "0" that ready signal is active-low
H_ADDR[8:1]	129,131,133,134,135, 137,138,140	I	Host Address Bus. These signals are connected to the address bus of the host processor interfaced with the GDC21D701C.

Pin Description*(continued)*

NAME	PIN	TYPE	DESCRIPTION
Host Bus Interface (Shared RGD Digital Outputs)			
H_DATA[15:0]	106,107,109,110,111, 113,114,116,117,119, 120,122,123,125,126, 128	I/O/Z	Data Bus. These signals are connected to the address bus of the external host processor.
READY	88	O/Z	Data Acknowledge
DMA_REQ_N	89	O	DMA Request Signal (active-low)
DMA_ACK_N	95	I	DMA Acknowledge Signal (active-low)
Power / Ground			
VDD	3,8,16,24,32,40,50, 56,62,68,94,101,105, 112,118,127,132,136, 141,154,171,177,184, 193,199,205,211,217, 222,223,229,237,242, 250,258,266,267,276, 285,295, 299	PWR	Digital Power - 3.3V
Power / Ground			
VSS	1,5,11,19,29,37,44, 47,53,59,65,71,90,96, 103,108,115,121,124, 130,139,143,152,174, 180,189,196,202,208, 214,220,225,232,239, 247,255,262,271,272, 279,283, 290, 304	GND	Digital Ground
VDDA	79, 83, 87	PWR	Analog Power - 3.3V
VSSA	77, 81, 85	GND	Analog Ground
Scan Test			
SCAN_IN[6:1] Test Mode Input	162, 160, 158, 157, 156,155, 163, 164, 165, 166	I	Test Input. These pins are only used for test mode. For normal function, these pins are connected to GND
SCAN_OUT[6:1] Test Mode Output	149, 148, 147, 146, 145,144, 168, 169	O	Test Output. These pins are only used for test mode. For normal function, these pins are not connected.

4. Block Diagram

The Video Display Processor offers a solution for the design of display systems for Grand Alliance DTV applications. Figure 2. shows the internal block diagram of the VDP. It consists of Format Conversion, PIP function, On-Screen Display, Color Space Conversion, Lookup tables for Customer Controls, and D/A Conversion. The Format Conversion requires 8Mbytes external SDRAMs (four 2Mbytes SDRAM: GM72V161621AT or same type). Figure 3. shows one DTV solution by using VDP chip.

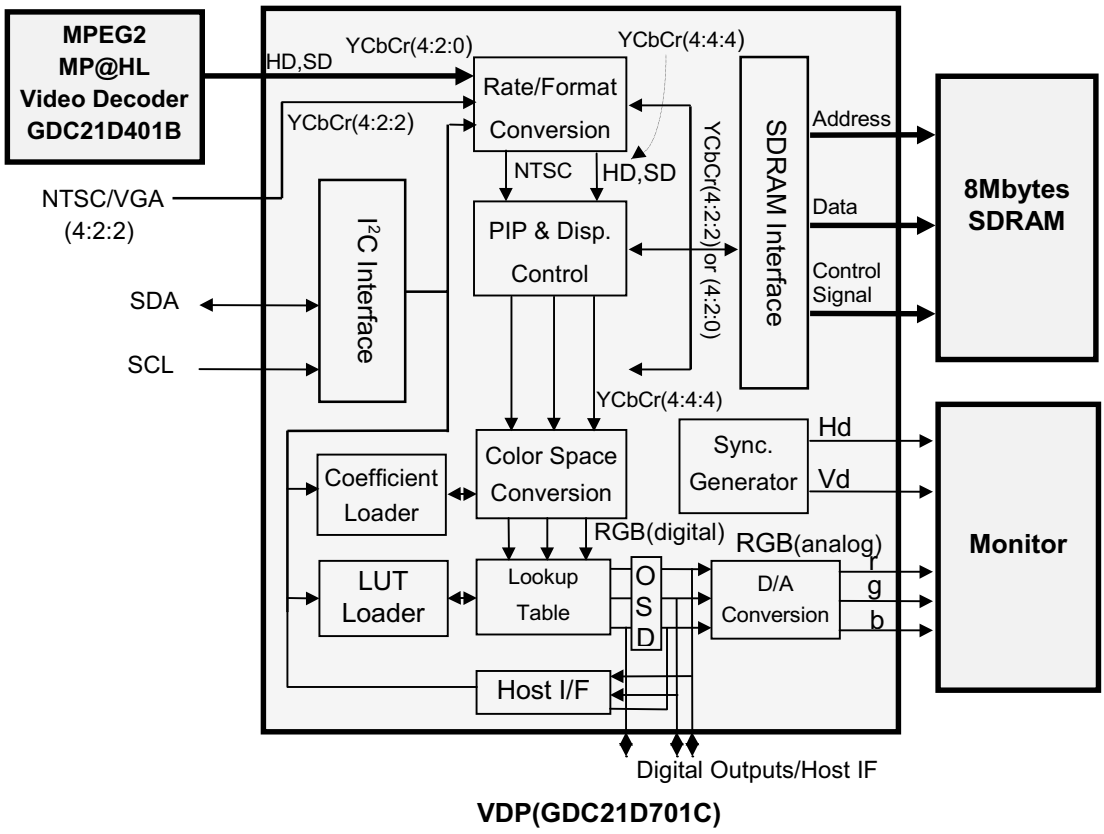


Figure 2. Block Diagram of Video Display Processor

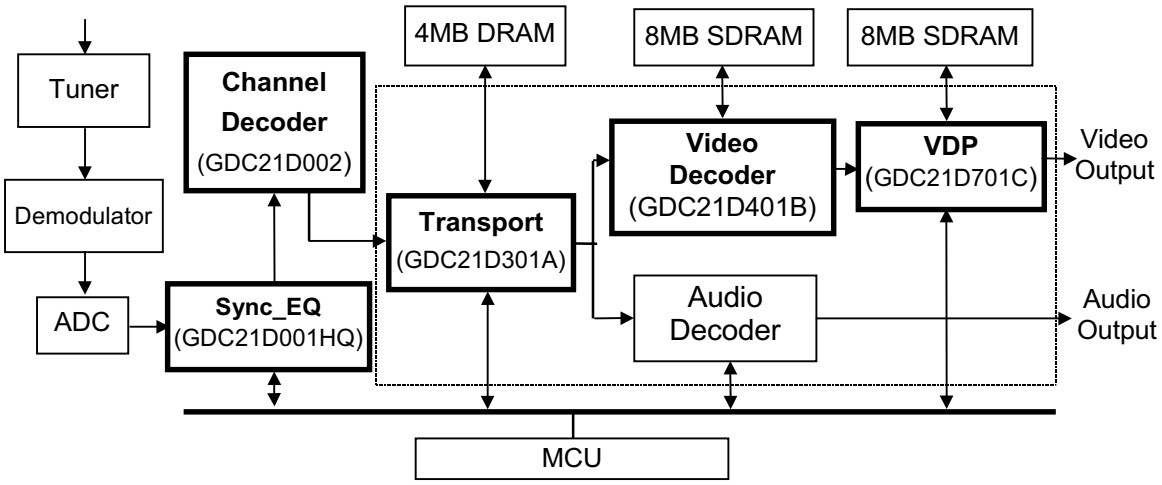


Figure 3. DTV Solution Diagram

5. Functional Description

5.1 Format Conversion

The Format Conversion Block receives all Grand Alliance input image formats, 480x720 image format, two digital NTSC image formats, and VGA/SVGA input formats and converts them into 1080x1920 interlaced display format. The followings are specifications of the format conversion functions of the VDP.

Table 1. HD Input Formats (Chrominance Format 4:2:0, Aspect Ratio 16:9)

Video Resolutions (Vertical lines x Horizontal Pixels)	FRAME RATES	SCAN TYPES
1080x1920	30Hz	Progressive
1080x1920	24Hz	Progressive
1080x1920	30Hz	Interlaced
720x1280	60Hz	Progressive
720x1280	30Hz	Progressive
720x1280	24Hz	Progressive

Table 2. SD Input Formats (Chrominance Format 4:2:0)

VIDEO RESOLUTIONS (Vertical lines x Horizontal Pixels)	FRAME RATES	ASPECT RATIOS	SCAN TYPES
480x704	60Hz	4:3 or 16:9	Progressive
480x704	30Hz	4:3 or 16:9	Progressive
480x704	24Hz	4:3 or 16:9	Progressive
480x704	30Hz	4:3 or 16:9	Interlaced
480x720	60Hz	4:3 or 16:9	Progressive
480x720	30Hz	4:3 or 16:9	Progressive
480x720	24Hz	4:3 or 16:9	Progressive
480x720	30Hz	4:3 or 16:9	Interlaced
480x640	60Hz	4:3	Progressive
480x640	30Hz	4:3	Progressive
480x640	24Hz	4:3	Progressive
480x640	30Hz	4:3	Interlaced

Table 3. Digital NTSC and VGA Input Formats (Chrominance Format 4:2:2, Aspect Ratio 4:3)

VIDEO RESOLUTIONS (Vertical lines x Horizontal Pixels)	FRAME RATES	SCAN TYPES
480x720	30Hz	Interlaced
480x768	30Hz	Interlaced
480x768	60Hz	Progressive
480x640	60Hz	Progressive
768x1024	60Hz	Progressive

Table 4. Display Output Format (Chrominance Format 4:4:4, Aspect Ratio 16:9)

VIDEO RESOLUTIONS (Vertical lines x Horizontal Pixels)	FRAME RATES	SCAN TYPES
1080x1920	30Hz	Interlaced

16x9 Image Display Mode

Two HD size images are converted into 1080x1920 display size. But SD size images are converted into 960x1760 or 1080x1920 active image size and displayed in the 1080x1920 display as shown in Figure 4. Therefore, there is some black area at the outer part of the display in the Mode I. The active display position can be moved by '**sd_pos_x**', '**sd_pos_y**' registers. The resolution of active display is shown in Table 5.

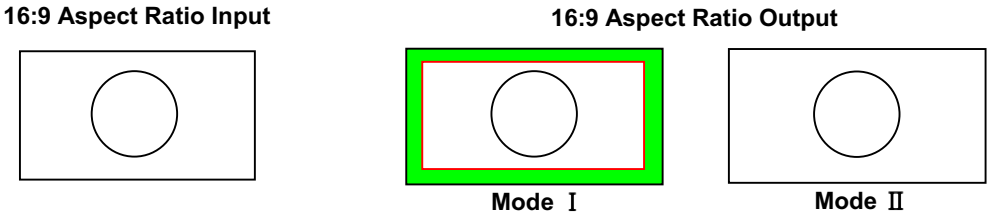


Figure 4. Display Modes

Table 5. Main Picture Display Resolution(16:9 Input Image)

INPUT FRAME RESOLUTIONS (Vertical Lines x Horizontal Pixels)	ACTIVE DISPLAY RESOLUTION (Vertical Lines x Horizontal Pixels)
1080x1920	1080x1920
720x1280	1080x1920
480x704	960x1706, 1080x1920
480x720	960x1706, 1080x1920

4x3 Image Display Modes

The 4x3 SD input and NTSC input can be displayed into 4x3 aspect ratio image or 16x9 aspect ratio one. The display mode can be selected by '**arc_mode**' register. Mode I, the default display mode, generates 4x3 active display. Mode Ⅲ and Mode Ⅳ generates 16x9 active display.

The active display resolution in each mode is shown in Table 6. In the mode Ⅴ display, active display area can be controlled by **'v_offset'** value of '**arc_mode**' register.

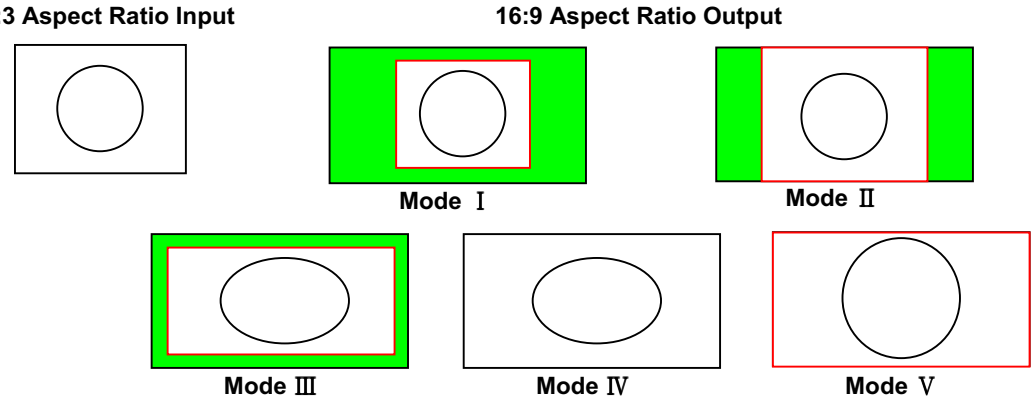


Figure 5. Display Mode

Table 6. Active Display Resolution for Each Mode

MODE	ACTIVE DISPLAY RESOLUTION
Mode Ⅰ	960x1280
Mode Ⅱ	1080x1440
Mode Ⅲ	960x1706
Mode Ⅳ	1080x1920
Mode Ⅴ	1080(1440)x1920

Table 7. Possible Display Modes for Progressive Frame Input Formats

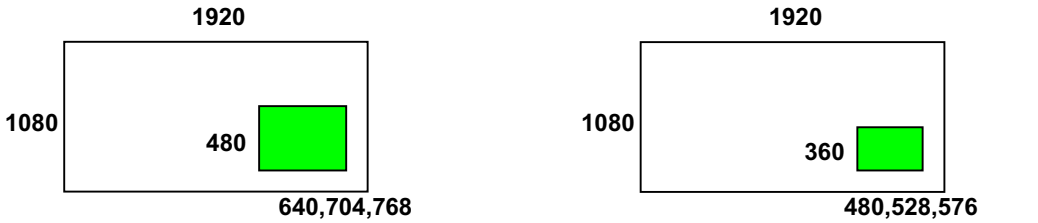
INPUT FRAME RESOLUTIONS (Vertical lines x Horizontal Pixels)	DISPLAY MODES
480x640	mode Ⅰ,Ⅱ,Ⅲ,Ⅳ,Ⅴ
480x704	mode Ⅰ,Ⅱ,Ⅲ,Ⅳ,Ⅴ
480x720	mode Ⅰ,Ⅱ,Ⅲ,Ⅳ,Ⅴ
480x768	mode Ⅰ,Ⅱ,Ⅲ,Ⅳ,Ⅴ

Table 8. Possible Display Modes for Interlaced Frame Input Formats

INPUT FRAME RESOLUTIONS (Vertical Lines x Horizontal Pixels)	DISPLAY MODES
480x640	mode Ⅰ,Ⅱ,Ⅲ,Ⅳ,Ⅴ
480x704	mode Ⅰ,Ⅱ,Ⅲ,Ⅳ,Ⅴ
480x720	mode Ⅰ,Ⅱ,Ⅲ,Ⅳ,Ⅴ
480x768	mode Ⅰ,Ⅱ,Ⅲ,Ⅳ,Ⅴ

PIP Specification

The VDP supports two selectable PIP sizes. Each PIP can be located in the arbitrary positions. The size of each PIP window is slightly different depending on the input format size. The VDP cannot run two ATV or two NTSC images simultaneously by PIP operation.
As shown in the Figure 6. and Figure 7. only "ATV main, NTSC PIP" mode or "NTSC main, ATV PIP" mode is possible. The PIP size and location can be controlled by '**pip_mode**' and p**ip_pos_x**' and '**pip_pos_y**' registers. The PIP border line width and color can be controlled by '**pip_mode**' register and '**pip_brdr_clr**' register.
The boundary part of PIP can be 5%, 10% cropped to remove the noisy boundary part images.



Large PIP(PIP ratio : approximately 4/27) **Small PIP(PIP ratio : approximately 1/12)**

Figure 6. PIP Modes - 4:3 PIP Mode (Main ATV, PIP NTSC or Main NTSC, PIP:SD)

Large PIP(PIP ratio : 1/4) **Small PIP(PIP ratio : 1/9, 1/16)**

Figure 7. PIP Modes - 16:9 PIP Mode (Main:NTSC, PIP:ATV)

Table 9. PIP Conversion Size(Main: NTSC, 16:9 PIP)

INPUT FRAME SIZE (Vertical Lines x Horizontal Pixels)	LARGE PIP SIZE	SMALL PIP SIZE
1080x1920	540x960	270x480
720x1280	540x960	360x640
480x704	480x880	360x704
480x720	480x880	360x704

Table 10. PIP Conversion Size(Main: HD or NTSC, 4:3 PIP)

FRAME SIZE (Vertical Lines x Horizontal Pixels)	LARGE PIP SIZE	SMALL PIP SIZE
480x640	480x640	360x480
480x704	480x704	360x528
480x720	480x704	360x528
480x768	480x768	360x576

Multi-PIP Specification

The VDP supports 16 channel Multi-PIP operation. The only one of the 16 PIPs is motion picture and the other images are in the frozen status. The '**display mode**' register is used for selecting Multi-PIP mode. The '**multi_chnl_pos**' register is used to select motion picture position among 16 PIP positions.
ATV input and NTSC input can be displayed in the Multi-PIP window. The border colors of Multi-PIP and PIP can be programmed independently. If the border colors of Multi-PIP and PIP are different, the border of motion picture window can be moved by programming '**pip_pos_x**' and '**pip_pos_y**' register to synchronize with "**multi_chnl_pos**" register.
Multi-PIP operation only operates when ATV input signal is valid.
The required position register values are listed in the register description section. Setting FIR Filter coefficients can enhance display quality. Low pass Filtering can reduce the aliasing effect in the multi-PIP display mode.

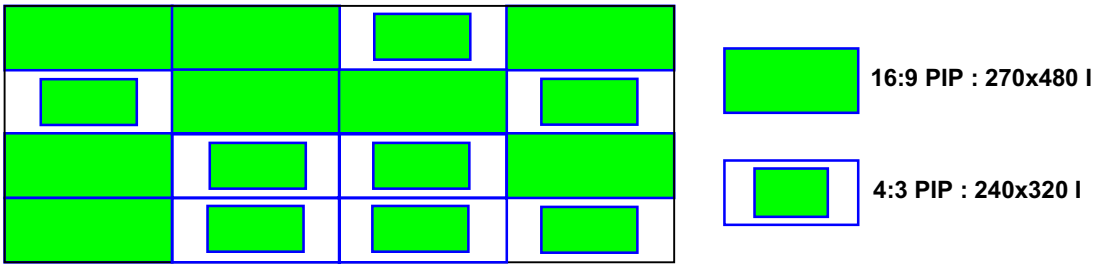


Figure 8. Multi-PIP(16 PIPs)

Table 11. PIP Conversion Size for Multi-PIP(16:9 PIP)

INPUT FRAME SIZE (Vertical Lines x Horizontal Pixels)	PIP SIZE
1080x1920	270x480
720x1280	270x480
480x704	240x352
480x720	240x352

Table 12. PIP Conversion Ratio for Multi-PIP(4:3 PIP)

INPUT FRAME SIZE (Vertical Lines x Horizontal Pixels)	PIP SIZE
480x640	240x320
480x704	240x352
480x720	240x352
480x768	240x384

Zoom Specification

The VDP supports x4 zoom operation for 1080x1920 or 720x1280 input format. The nine zoom positions(upper left, upper center, upper right, medium left, medium center, medium right, lower left, lower center, and lower right part) can be selected and zoomed into 1080x1920 image size. Zoom operation can also be used after the freeze operation. After the freeze operation, the picture quality can be enhanced or changed by lookup table and FIR filter control. In the zoom operation mode, PIP operation is not supported.

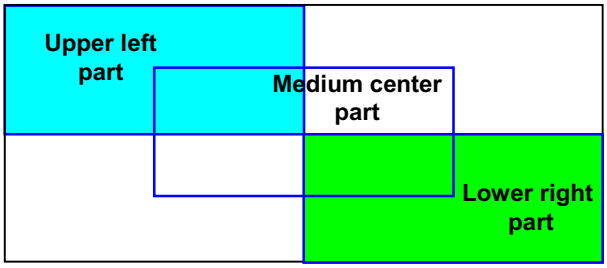


Figure 9. Zoom Operation

5.2 I²C bus interface

The I²C bus interface is used for host data interface. It operates only as a Slave. The Chip-ID(dev address) of the VDP is '1000111' b(0x8e). The data on the I²C-bus can be transferred at the rate up to 100 Kbit/s in the standard mode, or up to 400 Kbit/s in the fast mode. The I²C bus data Read/Write(R/W) formats of the VDP are shown in Figure 10. and Figure 11. Normal register R/W uses this R/W cycle. The OSD, palette, and the lookup table data write operation use the I²C burst write (incremental address) mode. I²C Burst Write Cycle is shown in Figure 12. For more I²C bus information, refer to the I²C bus standard.

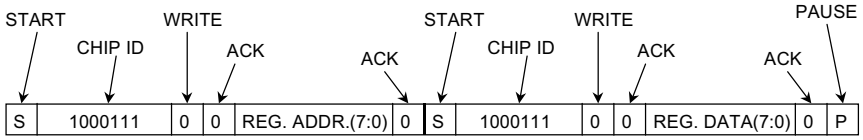


Figure 10. Write Cycle Diagram

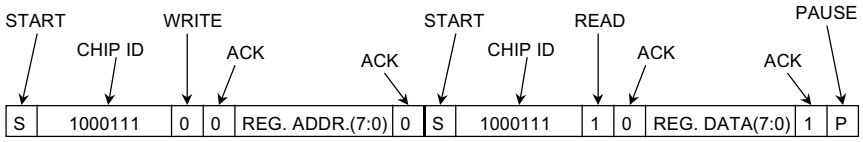


Figure 11. Read Cycle Diagram

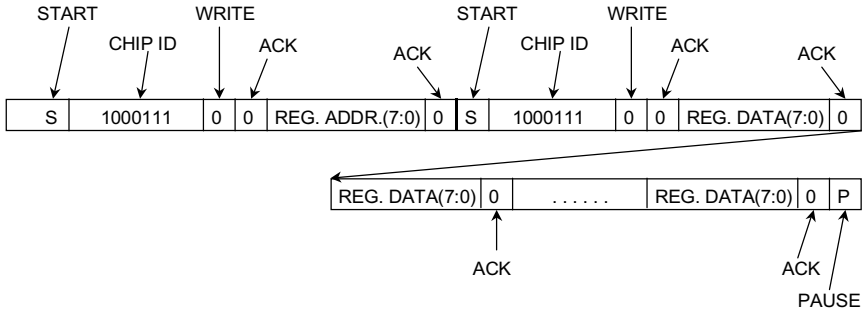


Figure 12. Burst Write Cycle Diagram

5.3 Host Interface

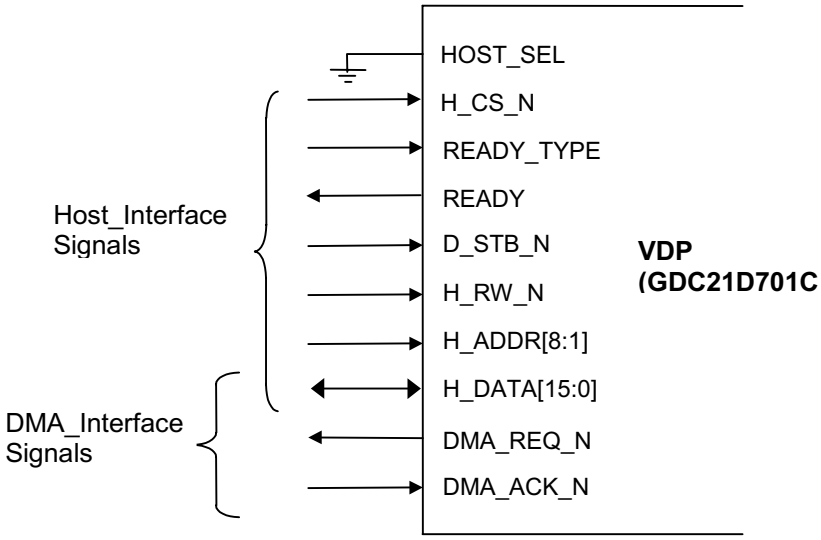


Figure 13. Host Interface

5.3.1. Host Interface Signal Description

H_CS_N	Host Chip Select	If this signal is set to '0', the host interface of the GDC21D701C is selected. According to H_RW_N signal status, microprocessor performs write/read operation. If this signal is '1', the host interface doesn't answer to external microprocessor address and dataline, databus is on 3-state mode.
READY-TYPE	Ready Type	If this signal is set to '0', Ready signal status is Active LOW, if this is '1', it is Active HIGH.
H_ADDR[8:1]	Host Address	This 8-bit address bus is used when external host processor approaches to the GDC21D701C internal register or external SDRAM through the GDC21D701C. One bus cycle is generated when H_CS_N signal is activated. This address supports only 16-bit word approach.
READY	Data Ready	When H_CS_N signal is not activated, the Ready signal goes to high-impedance output. It informs the host processor of termination of the GDC21D701C internal operation.
H_DATA[15:0]	Data Bus	This 16-bit data bus sends or takes the data from the host processor. When the host processor is reading, the GDC21D701C drives this data bus, and it is writing, the host processor drives this. If it isn't in any bus cycle, this data bus goes to 3-state.
D_STB_N	Data Strobe	When the host processor is writing, this signal indicates that the data is ready. When it is reading, this indicates that the data is read at the moment of change from LOW to HIGH.
H_RW_N	Read/Write	If this signal is LOW, it indicates that the host processor is writing. If this is HIGH, it indicates that the host processor is reading. When writing, data should be valid at the moment that the D_STB_N signal is changed from '1' to '0'.
HOST_SEL	Host Select	If this signal is '0', the host interface in the GDC21D701C is activated. If this is '1', pins related to the host interface are used as digital output.

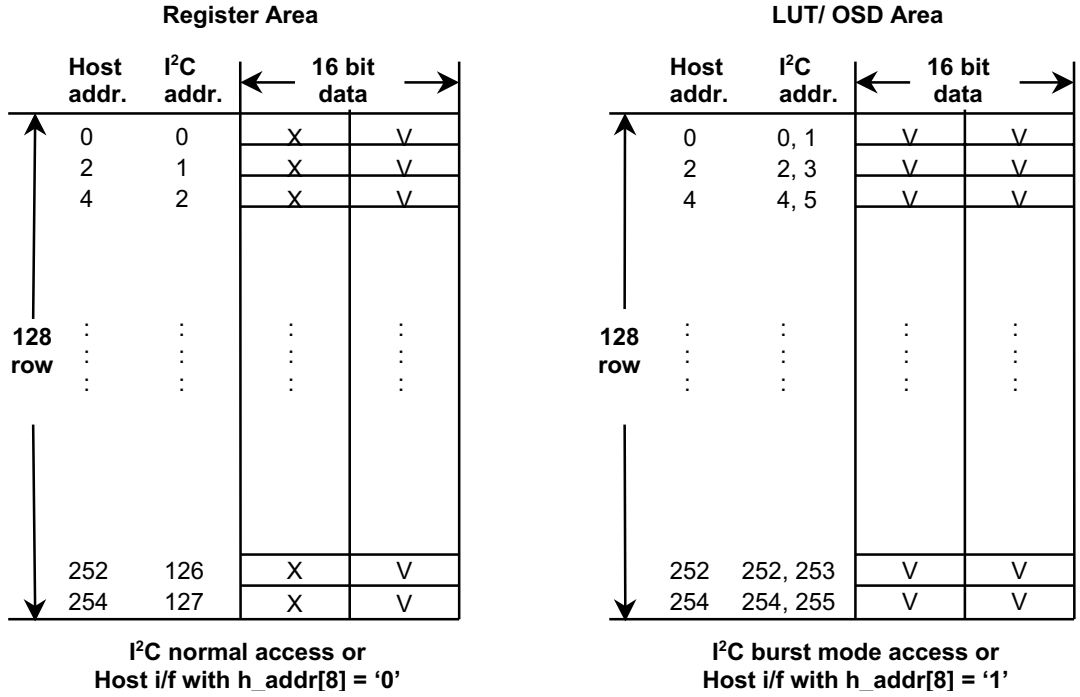


Figure 14. Address Map

Figure 14. shows address map of registers and LUT and OSD blocks in I^2C mode operation and parallel host interface operation. In parallel host interface mode, each LUT data elements can be changed individually.

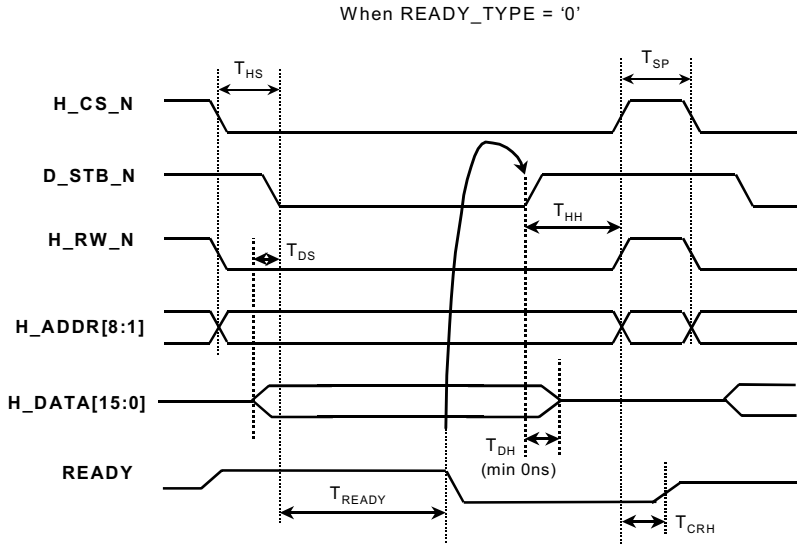
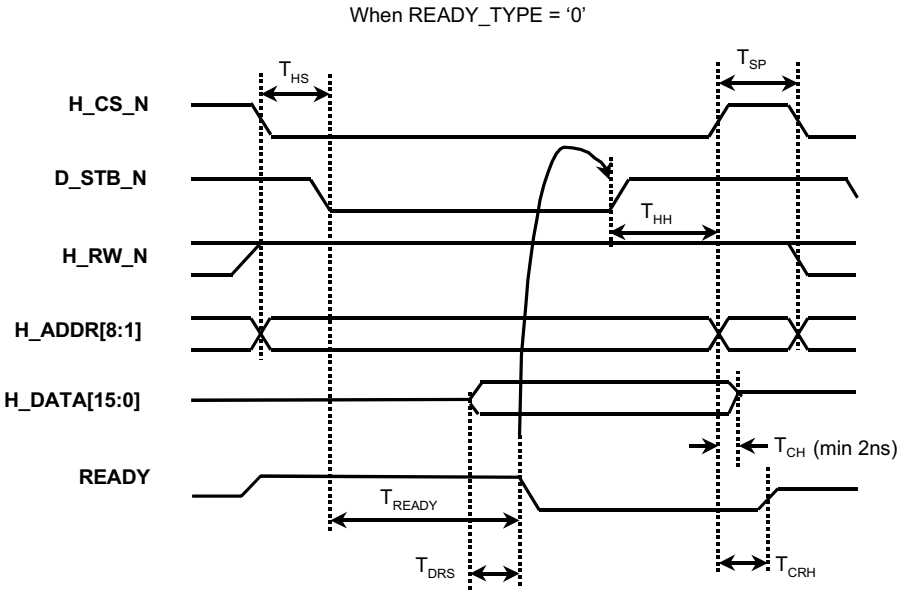


Figure 15. Host Write Timing



	MIN	MAX		MIN	MAX
T_{HS}	0		T_{CRH}	18.5	
T_{SP}	18.5		T_{READY}	130	User setting
T_{HH}	0		T_{DRS}	18.5	

Figure 16. Host Read Timing

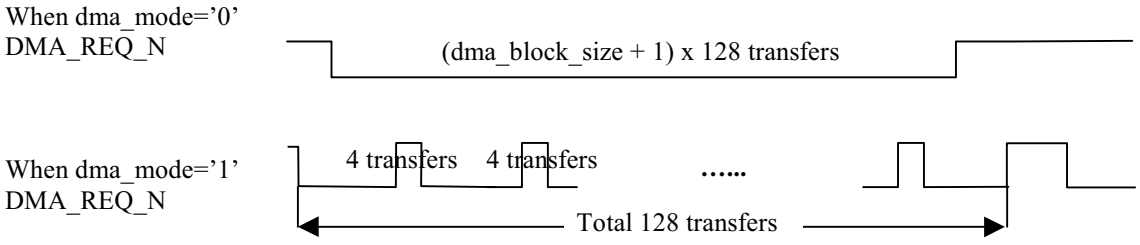
5.3.2 DMA Operation

DMA Start

If dma_start field of dma_mode register is set to '1', DMA_REQ_N signal is asserted to '0' and the VDP demands to DMAC the OSD data transmission.

DMA operation mode

dma_mode field of dma_mode register decides the assertion duration of DMA_REQ_N signal.



DMA Idle time

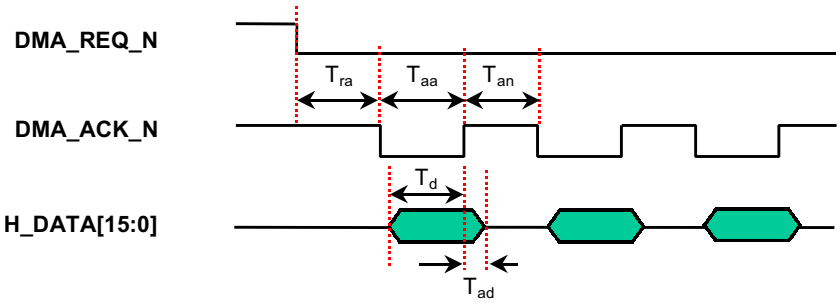
DMA operation is that 128 transfers compose 1 block, which total block number is set at dma_block_size register. After all blocks are transmitted, DMA_REQ_N signal is deasserted.

DMA_REQ_N timing

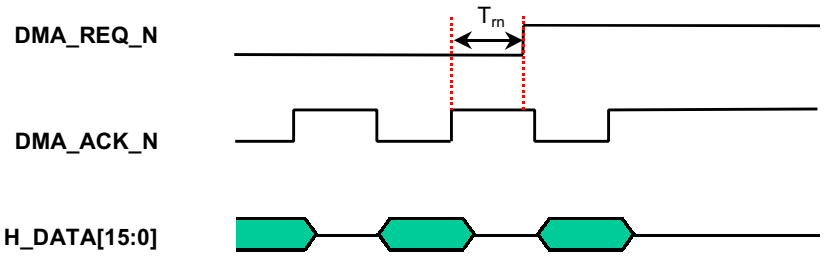
DMA_REQ_N signal deasserts maximum 55.5ns after deassertion of DMA_ACK_N signal at the end of transmission in case that dma_mode='0' and in every 3rd in case that dma_mode='1'.

DMA End

DMA operation is ended after it transfers the blocks as many as the blocks which are set at dma_block_size register.



DMA Start



DMA End

Figure 17. DMA Timing

SYMBOL	DESCRIPTION	MIN	MAX
T_{ra}	DMA_REQ_N Assertion to DMA_ACK_N Assertion	0 ns	-
T_{aa}	DMA_ACK_N Assertion	18.5 ns	-
T_{an}	DMA_ACK_N Negation	18.5 ns	-
T_{d}	H_DATA Start to DMA_ACK_N Negation	18.5 ns	-
T_{ad}	DMA_ACK_N Negation to H_DATA End	0 ns	-
T_{rn}	DMA_ACK_N Negation to DMA_REQ_N Negation		55.5 ns -

5.4 On-screen Display

The VDP supports On-screen Display(OSD) function. The OSD block gets 4:4:4 format video signal and sends converted video to the color-space converter. The input video signal is overlaid by user-defined OSD data including characters, symbols, and/or any other kind of graphic image.
The OSD data is described as a collection of rectangular blocks as shown in Figure 18. Two blocks can not be defined in the same row. As shown in Figure 19, a block is composed of a header and a bitmap data. The header contains positional information and the number of color used in the block.
There are 3 OSD layers in addition to the video layer; on the top is a cursor and below the cursor are 2 OSD layers and video. The mouse cursor, 32x32 pixels, can be moved just by programming the actual position. View ports are used for the layers to get OSD data seamlessly from external memory.

Main features are as follows:

- Multiple layers: cursor, two OSD layers above video
- Unlimited number of OSD regions per video field
- Capable of horizontal doubling
- Color resolution of 2/4/8 bits per pixel using pseudo color or 16 bits per pixel using true color
- Mouse cursor (32x32 pixel bitmap, 4 colors) movable all over screen
- Alpha keying factor variable between 0 and 1 in steps of 1/16
- Linked-list memory management
- Ease of animation

Control Registers

Control registers are checked for their values during every vertical blanking interval.

ADDRESS	BIT FIELD	FUNCTION
40h	7 : 0	Start Address of Cursor Bitmap, LSB
41h	7 : 0	Start Address of Cursor Bitmap, MSB
42h	7 : 0	Start Address of the First Header of OSD Layer 0, LSB
43h	7 : 0	Start Address of the First Header of OSD Layer 0, MSB
44h	7 : 0	Start Address of the First Header of OSD Layer 1, LSB
45h	7 : 0	Start Address of the First Header of OSD Layer 1, MSB
48h	0 1 2 4 5	Cursor Enable OSD Layer 0 (top) Enable OSD Layer 1 Enable OSD Layer 0 Animation Enable OSD Layer 1 Animation Enable
4Ah	7:0	Cursor Position X, LSB
4Bh	2:0	Cursor Position X, MSB
4Ch	7:0	Cursor Position Y, LSB
4Dh	2:0	Cursor Position Y, MSB
4Eh	0	OSD Register Update

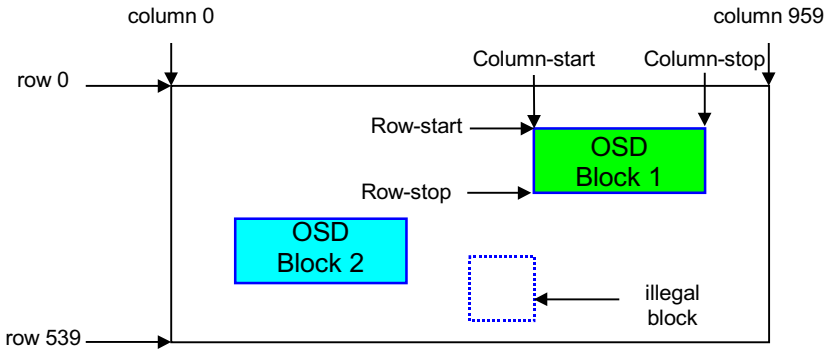


Figure 18. OSD Blocks in Video Display

OSD Data Addressing

The I²C bus address block of the VDP uses 8-bit programmable address and 8-bit incremental address. The only programmable address is used for VDP register access. But both programmable address and incremental address are used in lookup table write operation and in OSD data and palette write operation.

Lookup table access and OSD data write operation uses 0x80 ~ 0xff programmable address and 8-bit incremental address. Before the lookup table access, palette access, or OSD data write operation, each register must be set to the proper value. For lookup table access, '**lutw_en**' bit of '**lut_sel**' register must be set to '1', and '**osdw_en**' bit of '**osd_mode**' register must be set to '0'. For OSD data write operation, '**lutw_en**' bit of '**lut_set**' register and must be set to '0', '**lutwrgb**' register must be set to '1' and '**osdw_en**' bit of '**osd_mode**' register must be set to '1'. The '**osd_en**' flag in '**osd_mode**' register enables or disables the OSD function.

The four OSD buffers of SDRAM can be accessed by the 4-bit '**wr_ptr**' value of '**osd_mode**' register, 8-bit programmable address(0x80~0xff), and 8-bit incremental address(0x00~0xff). The 8-bit incremental address covers 32 column address of SDRAM(32 column x 8 byte/column = 256 byte). The 8-bit programmable address(0x80 ~ 0xff) covers 8 row of SDRAM(8 access/bank x 2 x 8 row = 128). As full I²C address range covers a quarter of OSD data buffer, the 4-bit 'wr_ptr' is used for addressing four OSD data buffers. Before the OSD data write, proper 'wr_ptr' must be set.

The VDP uses these register values for proper OSD address generation. In incremental addressing mode, 256 sequential data must be written to the VDP. If there is no sufficient data, zero padding to 256-byte is necessary for the proper operation of the VDP. When the digital output part of the VDP isn't be used, parallel host interface is used to load OSD data fast. In case that the host interface is used, as mentioned in chapter 5.3, register access, LUT and OSD data can be accessed, and OSD data can be loaded via DMA. When OSD is loaded through the host interface, the address corresponding to I²C programmable address uses 'osd_base' register value, and when via DMA, the OSD data start address refers to this register.

Memory Map

OSD data is organized in regions. Each region consists of a header and a bitmap. The header contains a pointer to the next OSD region, which is displayed at a lower screen position. The header of the first region is directed by a control register. To indicate that this is the last region, header pointer value must be all '0's.

In a layer of OSD, OSD regions cannot be overlapped in a horizontal row of pixels. A region can be placed anywhere on the screen if it doesn't exceed display area and row position (y) is greater than 1. For the interlaced raster scanning, top field lines have even numbers from 0 while bottom field lines have odd numbers from 1.

The number of bits per pixel (<nbits>) in the associated bitmap data can be 2, 4, or 8; therefore, <R> cannot be 2. It also defines the maximum number of colors within the image, and the maximum number of elements in the following color map table, if it follows. For the layer under video, <nbits> is restricted to just 2 or 4, yielding maximum 16 color image using a color map table.

In case a new color map exists, it follows right after the header definition. A color map entry comprises blending bit B and 6-bit Y, 2x4 bit Cb/Cr as described below.

The 4-bit alpha makes 16 steps of blending of video and OSD. Alpha value 0 produces completely transparent OSD and value 15 produces completely opaque OSD. Y component value 0 also makes the color transparent regardless of Cb and Cr. Before an OSD color is mixed, it is left justified to produce 8 bits each of Y, Cb and Cr with the lower bits padded with zeros.

The format of the actual image is defined as the series of pixel color index values that make up the image. The pixels are stored left to right and top to bottom sequentially. The first pixel within an OSD region begins at the most significant bit of the first bitmap word. If true color mode is used, the image is defined as either 4:2:2 format CbYCrY or YCbCrAlpha (6:3:3:4 bits), both yielding 16 bits per pixel. In this case, the horizontal size of image should be a multiple of two.

Bits																Word
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	No.
T	P	R				A		0	0	F						1
H	0	0	0	L												2
Reserved																3
Next OSD Header Pointer																4
Upper-left Corner Position X																5
Upper-left Corner Position Y																6
Lower-right Corner Position X																7
Lower-right Corner Position Y																8
Reserved																9
Top Field Bitmap Pointer																10
Reserved																11
Bottom Field Bitmap Pointer																12
Reserved																13
Animation Up Pointer																14
Reserved																15
Animation Down Pointer																16
Color Map Table (if needed)																17 (20/32/272)

Figure 19. OSD Header Definition

Note :
T=0 - Pseudo color
P=0 - Use existing color map
P=1 - New color map follows
T=1 - True color (16 bits/pel)
P=0 - CbYCrY (8 bits each)
P=1 - YCbCrAlpha (6:3:3:4)
R+1 - <nbits>/2, where nbits is number of bits per pixel (2, 4, or 8)
A - alpha keying value
F+1 - animation frame count
H=1 - horizontal doubling
L= ceil(image_size*nbits/2048)
All pointers are 16-bit values which points a 64-bit word. : (<row 7 bits> & <bank 1 bits> & <column 8 bits>)

	Bits																Word
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	No.
Y						0	B	Cb				Cr				1

Figure 20. Color Map Entry

Note :
B=0 - opaque color
B=1 - blend allowed

Cursor

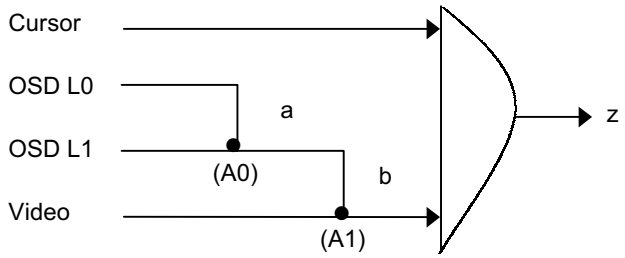
The cursor has size of 32x32 at maximum and can be placed anywhere on the screen. The position information which is written on a register is read every vertical blanking interval. The bitmap start address is also checked during that interval and a new cursor bitmap is loaded into internal memory if the new bitmap pointer differs from old one.
Four cursor colors and hotspot position data follows bitmap. The hotspot point of a cursor will be located on the screen position specified by registers.
The cursor bitmap is defined as the series of 2-bit pixel color index values. Every four 16-bit words defines a horizontal row of 32 pixels from left to right and the 32 succession of 4 words makes up a whole cursor. If you want a smaller cursor than 32x32 one, fill the non-used space with a transparent-color index.

	Bits																Word
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	No.
32 x 32 pattern																1 - 128
Cursor Color 0																129
Cursor Color 1																130
Cursor Color 2																131
Cursor Color 3																132
Hotspot X						Hotspot Y						0	0	0	0	0	0	133
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	134

Figure 21. Cursor Definition

Mixing

There are two OSD layers above video and one layer under video; and on top is the cursor. The top two OSD layers can be mixed at 16 levels and the result can be mixed with video at 16 levels. The bottom OSD layer is visible only when video is not active, for example, outside of a PIP box.



Note :
X denotes mixing operation with blending factor A0 or A1.
a = L0xA0 + L1x(1-A0)
b = axA1 + Videox(1-A1) when A0 /= 1, else b = L0
A0,A1 = k/64 where k = 0...62, 64

Animation

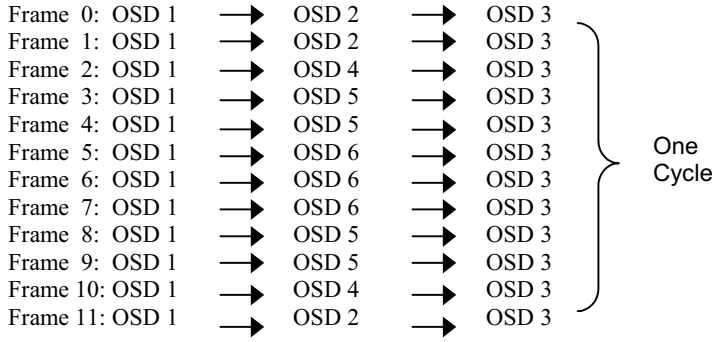
OSD layers 0 and 1 (L0, L1) supports simple animation. Only one animation object is allowed at a time on a layer. To support animation, a header contains two pointers in order to make a double linked list. If animation was enabled and both pointers are not 0 in a header, next animation object (OSD header) is automatically called by tracking animation up/down pointers.

EXAMPLE: CASE 1 - circular animation

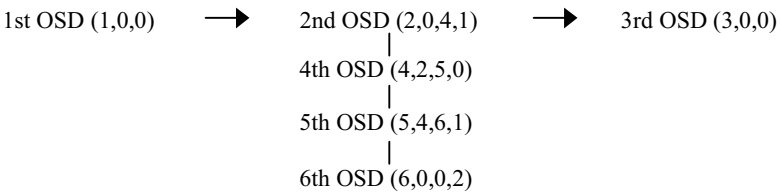
1st OSD (1,0,0) → 2nd OSD (2,0,4,1) → 3rd OSD (3,0,0)
4th OSD (4,2,5,0)
5th OSD (5,4,6,1)
6th OSD (6,5,0,2)

Values inside parentheses = (header_ptr, anim_up_ptr, anim_dn_ptr, [anim_Frame_cnt])

OSD display order in frame number from the start of animation:

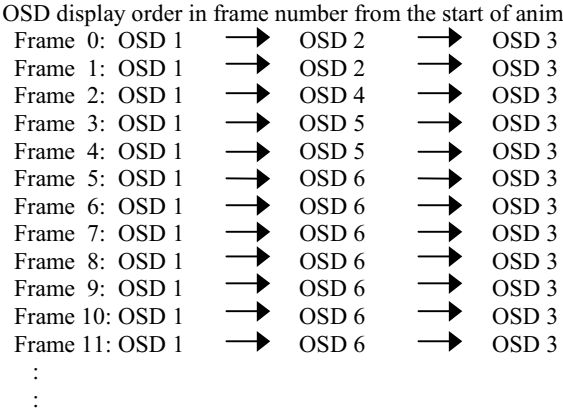


EXAMPLE: CASE 2 - linear animation



Values inside parentheses = (header_ptr, anim_up_ptr, anim_dn_ptr, [anim_Frame_cnt])

OSD display order in frame number from the start of animation:



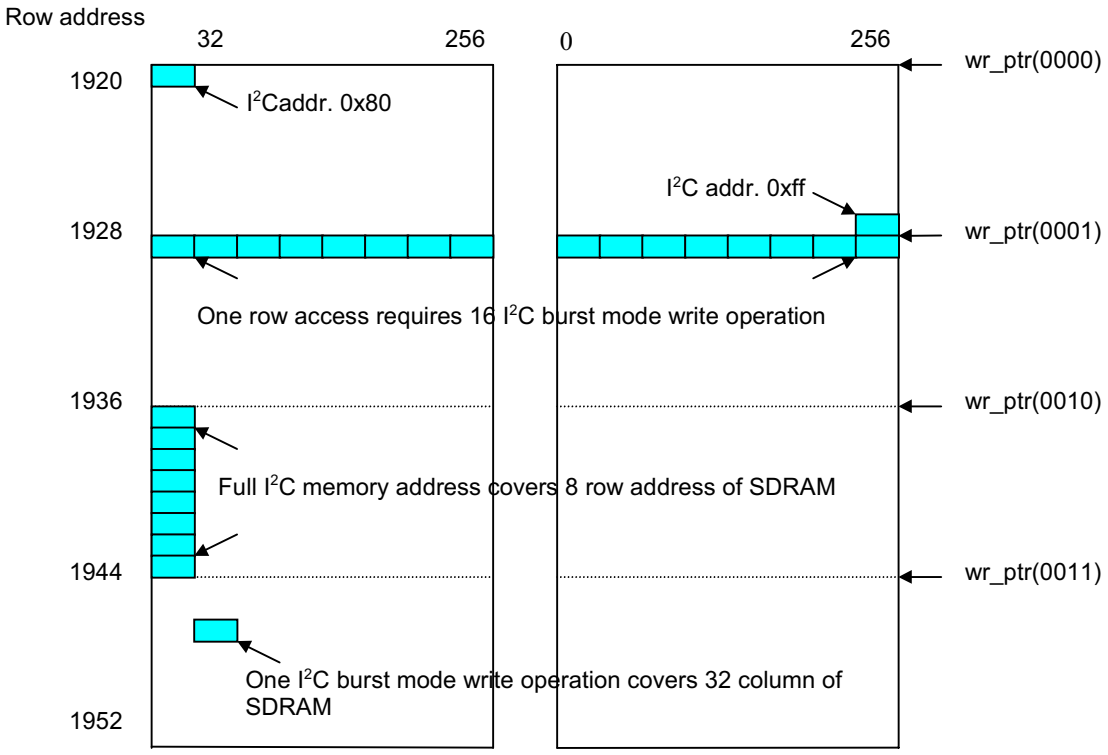


Figure 22. Memory Map of OSD Buffer

5.5 Color Space Conversion

The Color Space Conversion Block is a nine-multiplier array with internal bus structure and summing adders needed to implement a 3x3 matrix multiplier as shown in Figure 23. The data type of input ports, A(7:0), B(7:0), and C(7:0), is 8-bit integer which is also the data type of output ports, X(7:0), Y(7:0), and Z(7:0). The 9 coefficient input registers, '**csc_coef0**' ~ '**csc_coef8**', always receive 10-bit value which represents the range of 1023/2 ~ -1024/2. The nine coefficient values can be stored by I^2C registers and can be loaded by '**coef_load**' register.

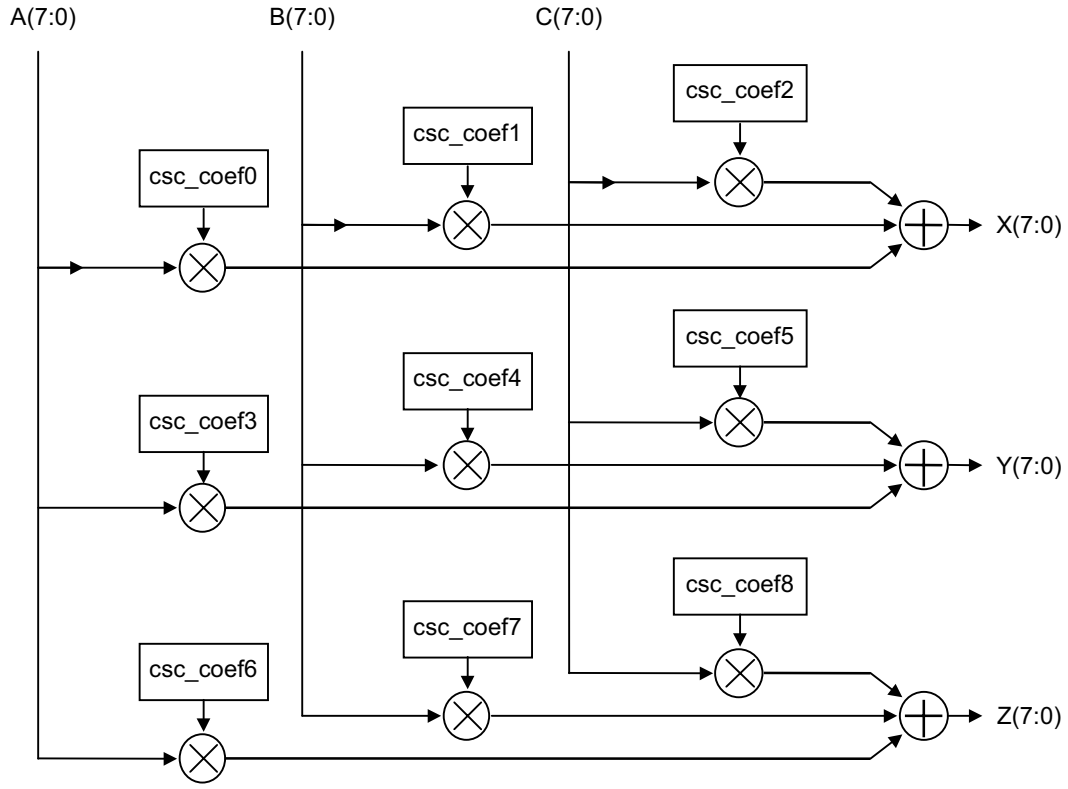


Figure 23. Functional Block Diagram of Color Space Conversion

5.6 Lookup Table Control

The VDP has two sets of swappable "lookup tables" and offers two three-channel customer control functions for RGB components as shown in Figure 24. Each lookup table has each individual Red, Green, and Blue component table. As a result, the VDP has totally 6 individual 256-byte lookup tables. Each lookup table can be programmed individually. If the contents of each lookup table are same, the set of lookup table(red, green, and blue lookup table) can be programmed simultaneously. If one set of lookup table is selected in "Write mode", the other is automatically selected in "Read mode". The lookup table is automatically changed only at the falling edge of "VDOUT_N" sync signal. The lookup table can be accessed by using the '**lut_sel**', '**lutwrgb**' register, 8-bit programmable address(0x80), and 8-bit incremental address(0x00 ~ 0xff). The 8-bit incremental address covers one lookup table.

The lookup table control block compensates for the opto-electronic transfer characteristics of the monitor and also performs Black level Expansion enhancements of the picture contrast or White compression via nonlinear adjusting functions.

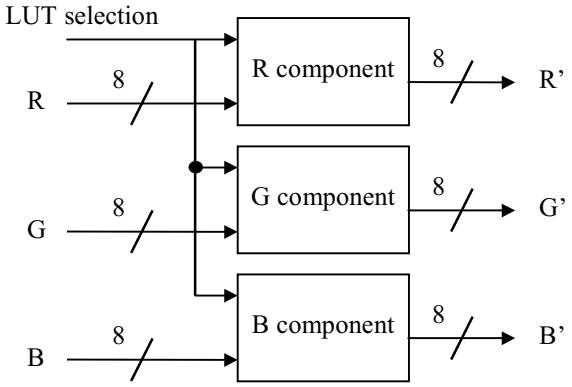


Figure 24. I/O Relations of Customer Control Block

5.7 D/A Conversion

The D/A Conversion Block consists of three high-speed D/A converter cells and Sync Generator. The D/A cell is a high-speed but lower-power 10-bit CMOS D/A converter containing stable voltage reference. The current high-accurate cells decrease non-linearity errors and glitches.

Features of the D/A

- Resolution : 10-bit 3-channel
- High speed operation(Max. conversion speed) : 75MHz
- Linearity error : ± 0.5 LSB (DNL)
- Analog output range : AVDD ~ AVDD-1(75Ω load)
- Built in self-bias circuit
- Power supply : +3.3V single

Sync Generator provides external sync signals, horizontal deflection, vertical deflection, horizontal sync and vertical sync signals for proper HD display and digital interface. All sync signals are digital output. HSYNCOUT_N and VSYNCOUT_N signals are synchronized with red, green, and blue digital and analog output. Especially digital processor can directly use these signals. HDOUT_N and VDOUT_N signals used for Monitor interface are also digital output. The analog output signals(ROUT, GOUT, BOUT) form and required interface circuit are described as following pictures.

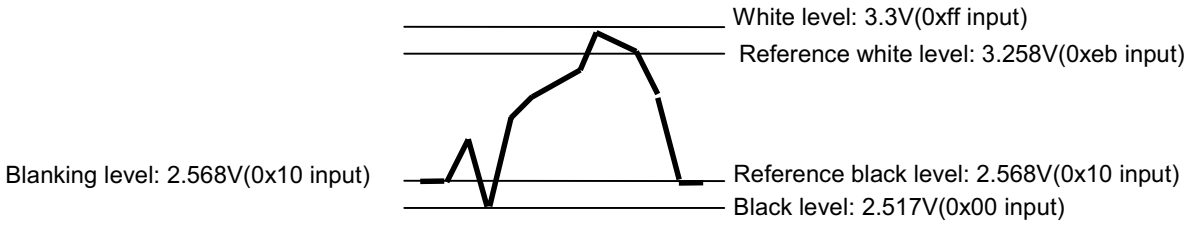


Figure 25. Analog Output Signal Form

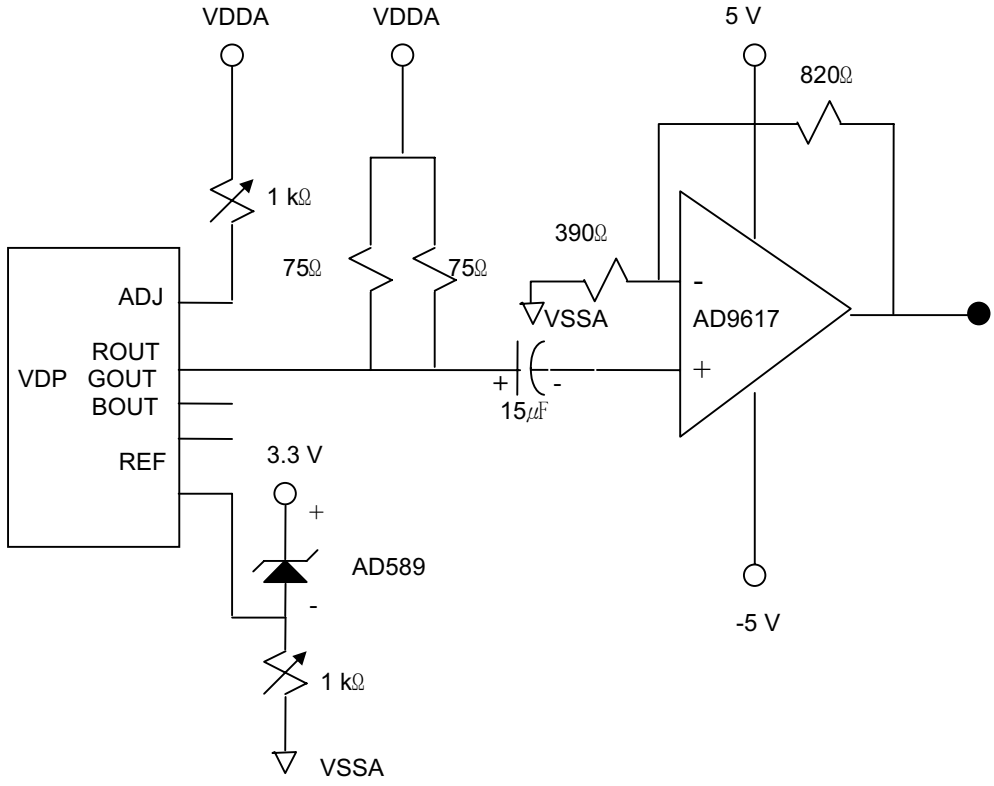


Figure 26. DAC Application Circuit

5.8 Display Sync Timing

The Video Display Processor(VDP) generates display sync signals required for monitor interface and HSYNCOUT_N and VSYNCOUT_N signals which denotes the active image positions of VDP output data. The VDP also generates horizontal and vertical deflection signals(HDOUT_N, VDOUT_N) for monitor back-trace. The 'FIELDSYNC' signal can be used for detecting Top/Bottom information. If 'FIELDSYNC' value is '1', present display is TOP field and vice versa. The followings are display sync timings of the VDP, which follow SMPTE274M specification.

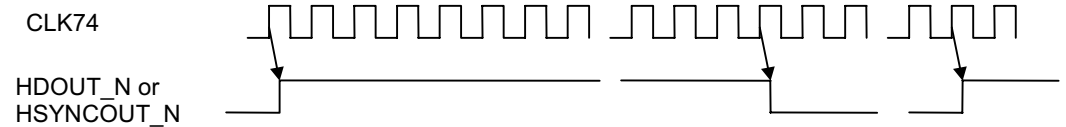


Figure 27. HSYNC Timing

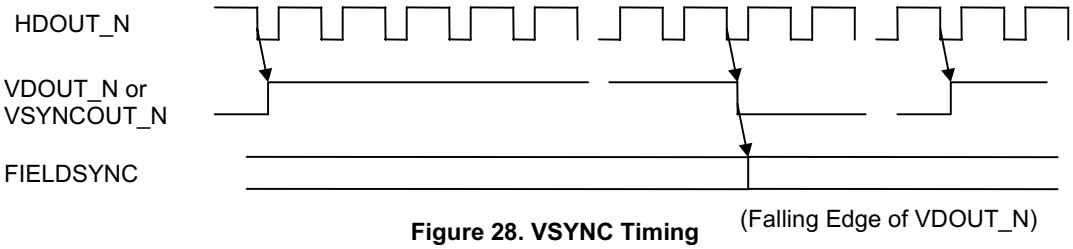


Figure 28. VSYNC Timing

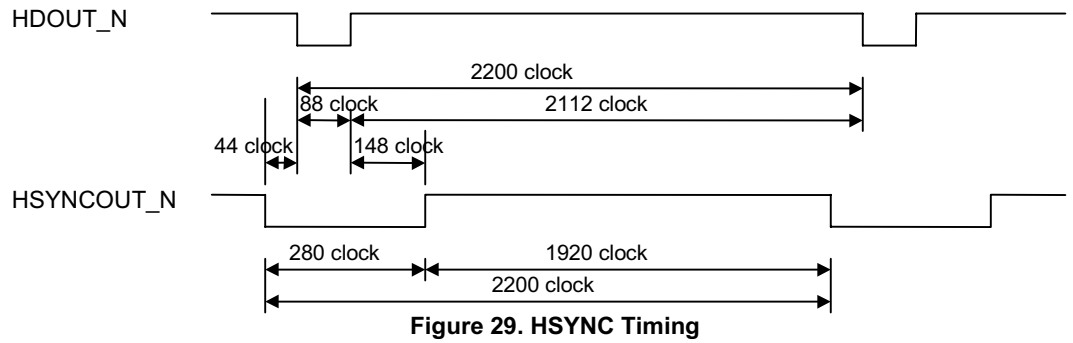


Figure 29. HSYNC Timing

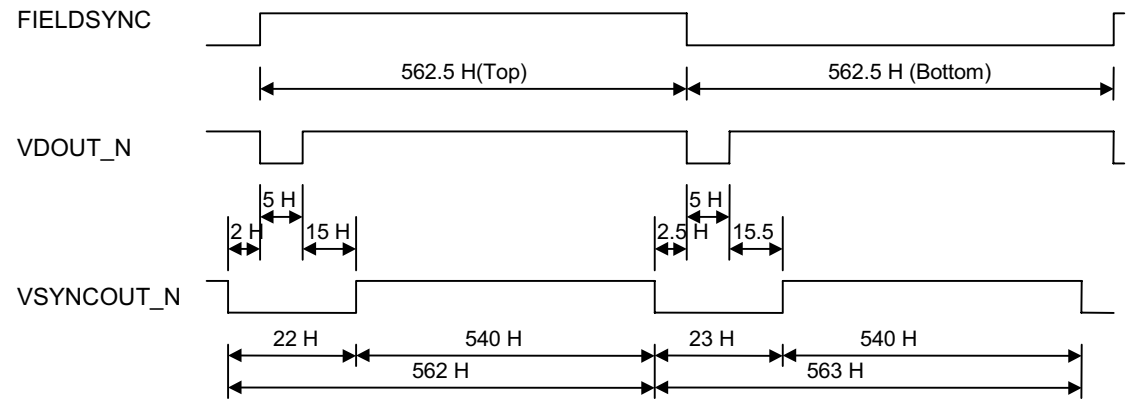


Figure 30. VSYNC Timing

5.9 SDRAM/Clock Interface

The VDP can store two frames of ATV image, two frames of NTSC/VGA image, and four frames of on-screen data. In the SVGA input mode, the VDP can store only SVGA image into the SDRAM. It can not store ATV image simultaneously. PIP function can not be supported in the SVGA input mode. The VDP requires 64-Mbit SDRAM (GM72V161621AT or same type) and as shown in Figure 31, four 16-Mbit SDRAMs can be directly attached to the VDP. The operation clock speed is 74.25MHz or 74.175MHz and it coincides with the VDP display clock. The memory interface clock should be delivered to the four SDRAMs with the same clock phase and should be delayed 2 ~ 3 ns compared with the VDP clock. So the clock of memory is delayed properly with clk74in and clk74out in the VDP.

The SDRAM address, data, and control signal path should be designed carefully and the path length for each SDRAM should be same to acquire better noise margin.

'H60' signal selects 60Hz/59.94Hz clock input. If this signal not used, the VDP automatically skips/repeats input images.

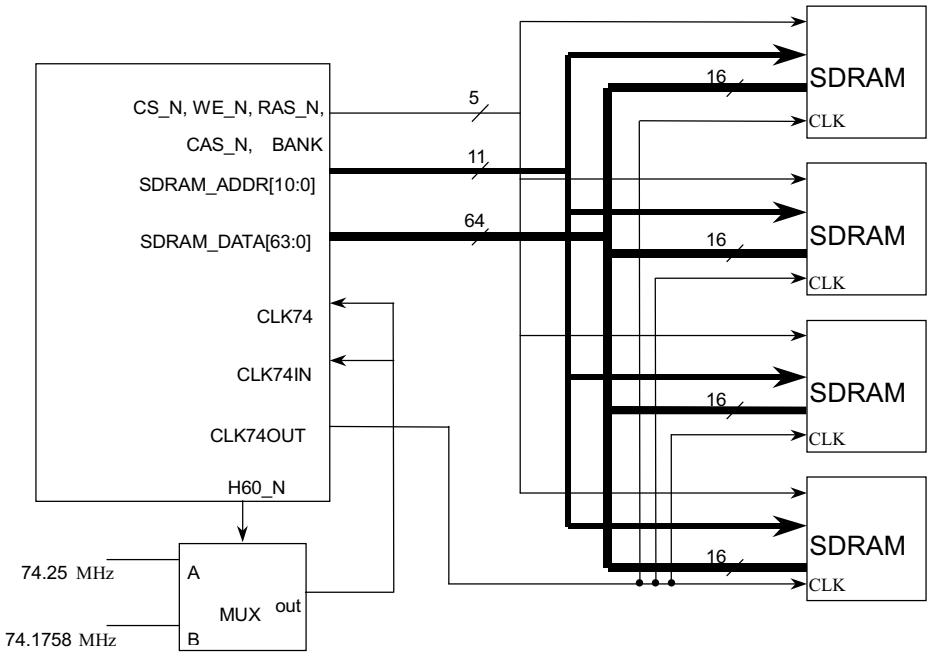


Figure 31. SDRAM Interface Scheme

5.10 NTSC/VGA Interface

The VDP interfaces with 4:2:2 digital NTSC image and 4:2:2 digital VGA image. Digital NTSC input can be 480x768 or 480x720 60Hz interlaced image or 480x768 60Hz double scanned NTSC (progressive) image. The VGA input can be 480x640 60Hz VGA, or 768x1024 60Hz SVGA input. The VDP interfaces with NTSC and VGA by using same input data ports and control ports. The interface scheme is described in Figure 32. and Table 16.

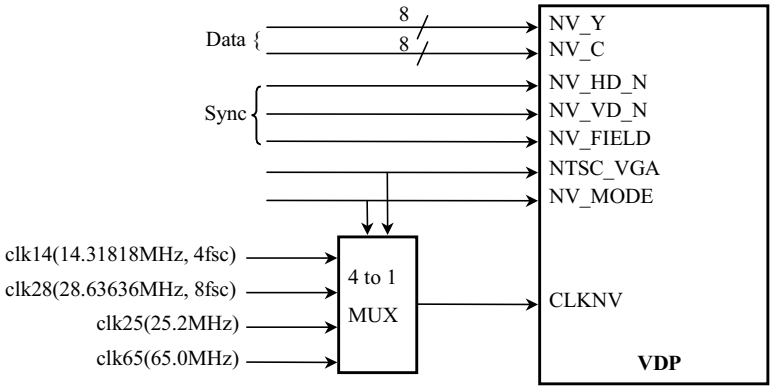


Figure 32. The NTSC/VGA Interface Scheme

Table 16. The Required Clock Input Depending on the NTSC/VGA

INPUT	NTSC_VGA	NV_MODE	CLKNV
NTSC	0	0	CLK14
Double scanned NTSC	0	1	CLK28
VGA	1	0	CLK25
SVGA	1	1	CLK65

NTSC Interface Timing

The NTSC interface timing can be controlled by interface registers. The input order of chrominance components is selected by '**nvinputformat**' register value. If '**cbcr**' value of '**nvinputformat**' register is '0', NTSC interface acquires chrominance data in CbCr order as shown in Figure 33. If that value is '1', NTSC interface acquires chrominance data in CrCb order as shown in Figure 34.

The interface between NTSC/VGA sync signals (NV_HD_N, NV_VD_N) and image data (NV_Y, NV_C) can be controlled by '**nvin_h**', and '**nvin_v**' registers. The '**nvin_h**' register value denotes the number of required clock difference between the rising edge of 'NV_HD_N' signal and the starting point of active image data in horizontal direction. The '**nvin_v**' register value denotes the number of required 'NV_HD_N' signals between the rising edge of 'NV_VD_N' signal and the starting point of active image data in vertical direction. Most NTSC chips generate 'HD' and 'VD' signals for monitor back-trace, 'HSYNC' signals, and 'VSYNC' signals that denote the positions of active image data. The VDP can interface with all sets of signals in the double scanned NTSC input. But it is recommended to interface with 'HSYNC' and 'VSYNC' signals in normal NTSC input. As shown in Figure 33. if the rising edge coincides with starting point of active data input, the '**nvin_h**' value can be zero. As shown in Figure 34. the starting point of active data is two clocks later than the rising edge of 'HSYNC', the '**nvin_h**' register value must be programmed with proper value and the required '**nvin_h**" value is 2 in this case. The 'high' level of 'NV_HD_N' should be longer than or equal to a '**nvin_h**' + 768 clock duration. The VDP grabs 768 active data by using clock counter from the active data position which can be calculated by '**nvin_h**' register value.

The required vertical sync timing is shown in Figure 35. The rising edge of vertical sync signal (NV_VD_N) must precede the rising horizontal sync edge (NV_HD_N) of first active line data. The falling edge of vertical sync signal must follow final falling edge of active line data as shown in Figure 35. The '**nvin_v**' register is used in the same manner and in Figure 35. case, the value is zero. The proper rising position of NV_VD_N for Field 1(Top field) is 23rd line and for Field 2(Bottom field) is 286th line. The proper falling position of NV_VD_N for Field 1 is 262nd line and for Field2 is 525th line.

The FIELD signal is required for NTSC interface. The value of 'FIELD' signal "0" means that present input is TOP field and vice versa. The 'FIELD' signal must be changed at the low interval of 'NV_VD_N'. In interfacing with the double scanned NTSC, VGA, or SVGA, the 'FIELD' signal value is not necessary in the VDP. The VGA output generally consists of three analog signal outputs, HD sync signals, and VD sync signals and those sync signals are used for monitor back trace. Thus, the VDP requires active data position that can be done by programming the '**nvin_h**' and '**nvin_v**' register value. The default input values are described in the register description section.

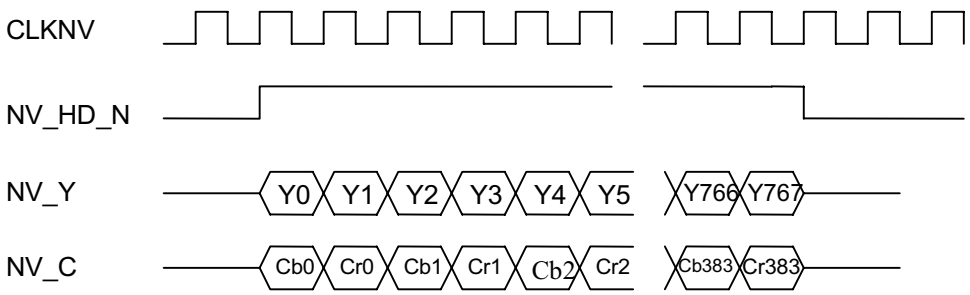


Figure 33. NTSC Data Interface(Default Mode)

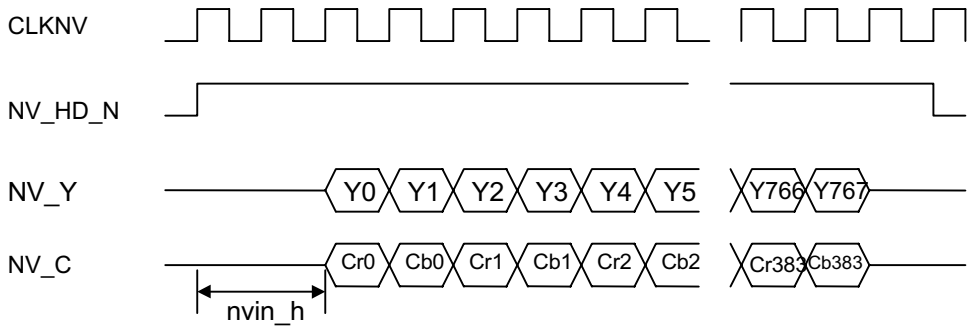


Figure 34. NTSC Data Interface(Default Mode)

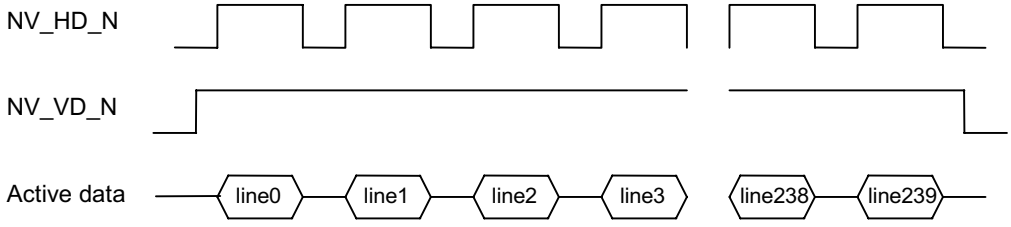


Figure 35. NTSC Data Interface(Default Mode)

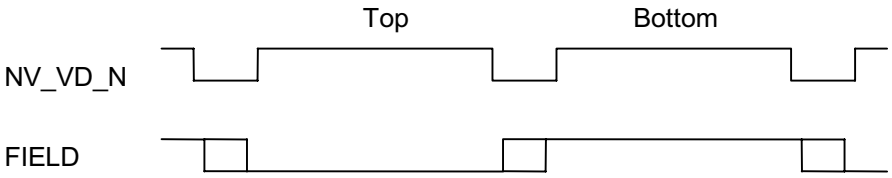


Figure 36. NTSC FIELD Signal Interface

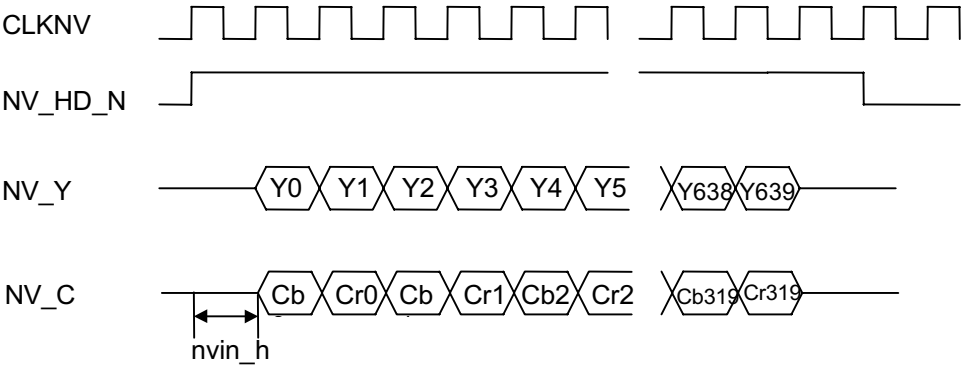


Figure 37. VGA Data Interface

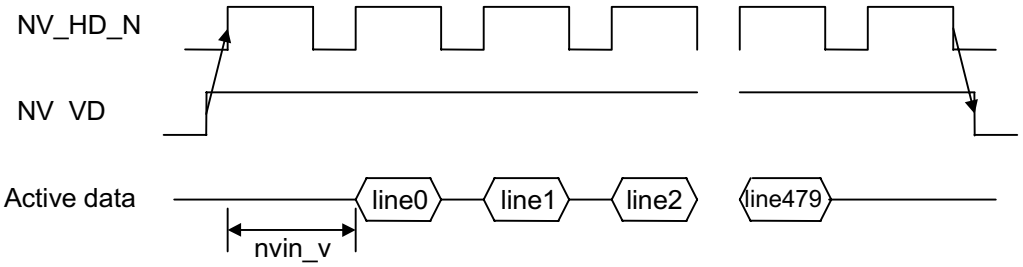


Figure 38. VGA Sync Interface

5.11 Video Decoder Interface

The VDP can interface with MPEG2 MP@HL Video Decoder(GDC21D401B) without any additional logic. The following figure shows the pin connections required between two chips.

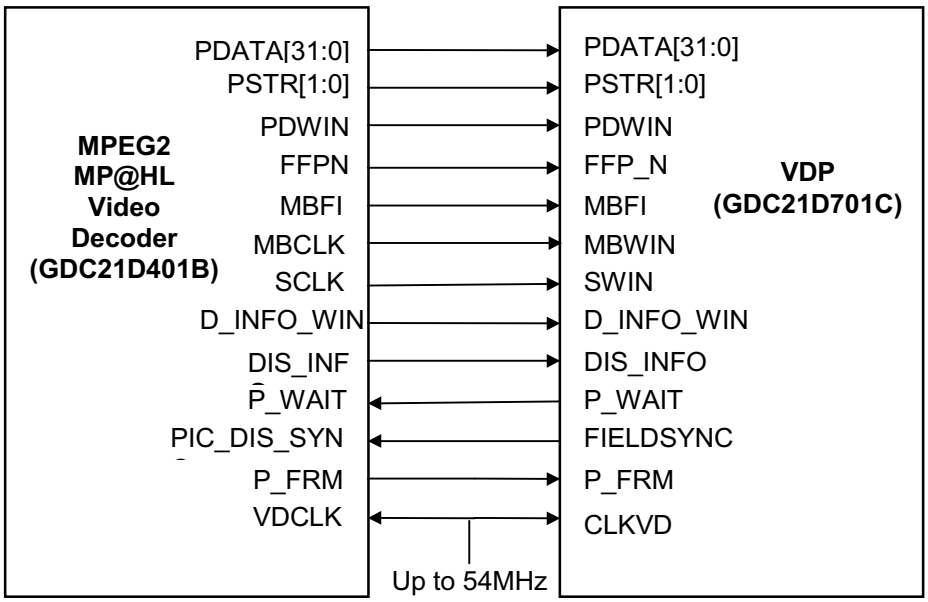


Figure 39. The Interface between the Video Decoder and the VDP

6. Register Descriptions

VDP Registers for I²C Interface

REGISTERS	R/W	ADDR	HEX	DESCRIPTION
csc_coef0[0]	R/W	0	0	A coefficient of color space converter(LSB of 10-bit)
csc_coef0[1]	R/W	1	1	A coefficient of color space converter(MSB(2-bit) of 10-bit)
csc_coef1[0]	R/W	2	2	A coefficient of color space converter(LSB of 10-bit)
csc_coef1[1]	R/W	3	3	A coefficient of color space converter(MSB of 10-bit)
csc_coef2[0]	R/W	4	4	A coefficient of color space converter(LSB of 10-bit)
csc_coef2[1]	R/W	5	5	A coefficient of color space converter(MSB of 10-bit)
csc_coef3[0]	R/W	6	6	A coefficient of color space converter(LSB of 10-bit)
csc_coef3[1]	R/W	7	7	A coefficient of color space converter(MSB of 10-bit)
csc_coef4[0]	R/W	8	8	A coefficient of color space converter(LSB of 10-bit)
csc_coef4[1]	R/W	9	9	A coefficient of color space converter(MSB of 10-bit)
csc_coef5[0]	R/W	10	a	A coefficient of color space converter(LSB of 10-bit)
csc_coef5[1]	R/W	11	b	A coefficient of color space converter(MSB of 10-bit)
csc_coef6[0]	R/W	12	c	A coefficient of color space converter(LSB of 10-bit)
csc_coef6[1]	R/W	13	d	A coefficient of color space converter(MSB of 10-bit)
csc_coef7[0]	R/W	14	e	A coefficient of color space converter(LSB of 10-bit)
csc_coef7[1]	R/W	15	f	A coefficient of color space converter(MSB of 10-bit)
csc_coef8[0]	R/W	16	10	A coefficient of color space converter(LSB of 10-bit)
csc_coef8[1]	R/W	17	11	A coefficient of color space converter(MSB of 10-bit)
fltr_coef0[0]	R/W	18	12	A coefficient of FIR filter(LSB of 10-bit) Center tap coefficient
fltr_coef0[1]	R/W	19	13	A coefficient of FIR filter(MSB(2-bit) of 10-bit) Center tap coefficient
fltr_coef1[0]	R/W	20	14	A coefficient of FIR filter(LSB of 10-bit)
fltr_coef1[1]	R/W	21	15	A coefficient of FIR filter(MSB of 10-bit)
fltr_coef2[0]	R/W	22	16	A coefficient of FIR filter(LSB of 10-bit)
fltr_coef2[1]	R/W	23	17	A coefficient of FIR filter(MSB of 10-bit)
fltr_coef3[0]	R/W	24	18	A coefficient of FIR filter(LSB of 10-bit)
fltr_coef3[1]	R/W	25	19	A coefficient of FIR filter(MSB of 10-bit)
fltr_coef4[0]	R/W	26	1a	A coefficient of FIR filter(9 LSBs of 10-bit)
fltr_coef4[1]	R/W	27	1b	A coefficient of FIR filter(9 MSBs of 10-bit)
coef_load	R/W	28	1c	Coefficient load command bit
csc_offset	R/W	29	1d	YcbCr offset selection
display_mode	R/W	32	20	Select display modes
multi_chnl_pos	R/W	33	21	Select hex value as multi-channel display position and input
multi_brdr_clr	R/W	34	22	Select multi-channel border color
pip_mode	R/W	35	23	Select PIP size and border width
pip_brdr_clr	R/W	36	24	Select PIP border color
pip_win_clr	R/W	37	25	Select PIP window color when there is no signal
pip_pos_x	R/W	38	26	Select PIP x-position(LSB of 11-bit)
pip_pos_x	R/W	39	27	Select PIP x-position(MSB(3-bit) of 11-bit)
pip_pos_y	R/W	40	28	Select PIP y-position(LSB of 10-bit)
pip_pos_y	R/W	41	29	Select PIP y-position(MSB(2-bit) of 10-bit)
zoom_pos	R/W	42	2a	Select zoom position(0~8)
osd_mode	R/W	43	2b	Control OSD operation and write/read address
sd_pos_x	R/W	44	2c	Select x-position of SD/NTSC format image
sd_pos_y	R/W	45	2d	Select y-position of SD/NTSC format image

VDP Registers for I²C Interface(*continued)*

REGISTERS	R/W	ADDR	HEX	DESCRIPTION
nvin_h	R/W	46	2e	Select horizontal active position of NTSC/VGA input
nvin_v	R/W	47	2f	Select vertical active position of NTSC/VGA input
nvinputformat	R/W	48	30	Select cb, cr chrom. data input order(NTSC/VGA)
atvformat	R	49	31	Represent present ATV format
arc_mode	R/W	50	32	Select SD or NTSC display format(16:9 or 4:3)
deint_th	R/W	51	33	De-interlacer threshold value
test_ptrn	R/W	52	34	Select test pattern
osd_base	R/W	53	35	OSD base address for Host interface
dma_block_size	R/W	54	36	Select DMA block size
dma_mode	R/W	55	37	Select DMA mode
host_wait	R/W	56	38	Select ready wait counter value
nonactive_val	R/W	59	3b	Select the gray level value of non-active region in SD display mode
lut_sel	R/W	60	3c	Select write mode lookup table
lutwrgb	R/W	61	3d	Red/Green/Blue component LUT write enable
palette_sel	R/W	62	3e	Select and control OSD color palette
disp_sel	R/W	63	3f	Select GBR/YPbPr display modes and sync level types
cur_adrl	R/W	64	40	Start Address of Cursor Bitmap, LSB
cur_adrh	R/W	65	41	Start Address of Cursor Bitmap, MSB
layer0_adrl	R/W	66	42	Start Address of the First Header of OSD Layer 0, LSB
layer0_adrh	R/W	67	43	Start Address of the First Header of OSD Layer 0, MSB
layer1_adrl	R/W	68	44	Start Address of the First Header of OSD Layer 1, LSB
layer1_adrh	R/W	69	45	Start Address of the First Header of OSD Layer 1, MSB
osd_en	R/W	70	48	Cursor Enable OSD Layer 0 (top) Enable OSD Layer 1 Enable OSD Layer 0 Animation Enable OSD Layer 1 Animation Enable
cur_pos_xl	R/W	71	4a	Cursor Position X, LSB
cur_pos_xh	R/W	72	4b	Cursor Position X, MSB
cur_pos_yl	R/W	73	4d	Cursor Position Y, LSB
cur_pos_yh	R/W	74	4d	Cursor Position Y, MSB
osd_load	R/W	75	4e	OSD Register Update

6.1 Coefficients of Color Space Converter

Nine 10-bit **csc_coef***n* registers are the coefficient registers of Color Space Converter. The following equation describes the corresponding row/column positions of the coefficient registers.

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} csc\_coef0 & csc\_coef1 & csc\_coef2 \\ csc\_coef3 & csc\_coef4 & csc\_coef5 \\ csc\_coef6 & csc\_coef7 & csc\_coef8 \end{bmatrix} \begin{bmatrix} A \\ B \\ C \end{bmatrix}$$

If the coefficient value is 299/256, we can calculate the coefficient register value as follows.

Coefficient value	001 0010 1011(11 bits)
Two complement notations of 299	001 0010 1011(11 bits)
1bit shift-right	000 1001 0101(11 bits)
Get 10 LSBs (register value)	00 1001 0101 (10 bits)
Register assignment	csc_coef*n*[1] csc_coef*n*[0]

If the coefficient value is -66/256, we can calculate the coefficient register value as follows.

Two complement notations of -66	111 1011 1110(11 bits)
1bit shift-right	111 1101 1111(11 bits)
Get 10 LSBs (register value)	11 1101 1111(10 bits)
Register assignment	csc_coef*n*[1] csc_coef*n*[0]

10-bit coefficients are stored in two 8-bit registers. 8 LSBs are stored in low address byte, and 2 MSBs are stored in high address byte.

The following table shows the initial coefficient settings of the VDP.

REGISTER NAME	REGISTER DEFAULT VALUE
csc_coef0	00 1000 0000 (256)
csc_coef1	11 1110 1000 (-48)
csc_coef2	11 1100 0100 (-120)
csc_coef3	00 1000 0000 (256)
csc_coef4	00 1110 1101 (475)
csc_coef5	00 0000 0000 (0)
csc_coef6	00 1000 0000 (256)
csc_coef7	00 0000 0000 (0)
csc_coef8	00 1100 1001 (403)

The register values are loaded to the Color Space Converter by using the **coef_load** register. Each register value is calculated with the following matrix coefficients.

$$\begin{bmatrix} G \\ B \\ R \end{bmatrix} = \frac{1}{256} \begin{bmatrix} 256 & -48 & -120 \\ 256 & 475 & 0 \\ 256 & 0 & 403 \end{bmatrix} \begin{bmatrix} Y \\ Cb-128 \\ Cr-128 \end{bmatrix}$$

6.2 Coefficients of FIR filter

Five 10-bit **flt_coef***n* registers are the coefficient registers of FIR filter. The designed FIR filter has symmetrical filter coefficients and five coefficient register values constitute 9-tap FIR filter as follows.

flt_coef4 flt_coef3 flt_coef2 flt_coef1 flt_coef0 flt_coef1 flt_coef2 flt_coef3 flt_coef4

The coefficient register values can be located in the range 512 ~ -511 and the corresponding filter coefficient values can be located in the range 512/256 ~ -511/256. The following table shows the initial coefficient settings of the VDP.

REGISTER NAME	REGISTER DEFAULT VALUE
fir_coef0	01 0000 0000
fir_coef1	00 0000 0000
fir_coef2	00 0000 0000
fir_coef3	00 0000 0000
fir_coef4	00 0000 0000

6.3 coef_load(default: xxxx xx00) x: unused bit

	1	0
	fir_load	csc_load

csc_load	DESCRIPTION
0	Get Color Space Converter coefficient register values
1	Load coefficients to Color Space Converter

fir_load	DESCRIPTION
0	Get filter coefficient register values
1	Load coefficients to Filter

If the loaded bits are set to ‘1’, the coefficient values are loaded on the falling edge of ‘VD’ signal and then the VDP is automatically set to ‘0’.

6.4 csc_offset(default : xxxx x011)

2	1	0
Y_offset	Cb_offset	Cr_offset

Y_offset	DESCRIPTION
0	Original Y value is used for matrix calculation
1	Y-16 is used for matrix calculation

Cb_offset	DESCRIPTION
0	Original Cb value is used for matrix calculation
1	Cb-128 is used for matrix calculation

Cr_offset	DESCRIPTION
0	Original Cr value is used for matrix calculation
1	Cr-128 is used for matrix calculation

csc_coefficient value must be set to '000' when the VDP output is in YPbPr display mode. The following shows the required matrix coefficients.

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \frac{1}{256} \begin{bmatrix} 256 & 0 & 0 \\ 0 & 256 & 0 \\ 0 & 0 & 256 \end{bmatrix} \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix}$$

6.5 display_mode(0000 0000)

7	6	5	4	3	2	1	0
ntpip_freeze	zoom	multi_ch	pip_on	unused	ntsc_freeze	atv_freeze	disp_sel

disp_sel	DESCRIPTION
0	ATV display
1	NTSC/VGA display

atv_freeze	DESCRIPTION
0	Normal display
1	ATV image Freeze. It works when disp_sel = '0'

ntsc_freeze	DESCRIPTION
0	Normal display
1	NTSC main image Freeze. It works when disp_sel = '1'

pip_on	DESCRIPTION
0	PIP off
1	PIP on

multi_ch	DESCRIPTION
0	Normal display
1	Multi-channel display

zoom	DESCRIPTION
0	Normal display(x1)
1	Zoomed display(x4) when ATV MD input form off

ntpip_freeze	DESCRIPTION
0	Normal NTSC PIP
1	Freeze NTSC PIP

6.6 multi_chnl_pos(xxx0 0000)

	4	3~0
	multi_chnl_input	multi_chnl_pos

If the '**multi_chnl_input**' value is '0', ATV input image is selected for multi-channel display. If the '**multi_chnl_input**' value is '1', NTSC input image is selected. The '**multi_chnl_pos**' value is located in the range 0 ~ 15 and each value represents the display position of active display area as follows.

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

6.7 multi_brdr_clr(0010 1101) - blue

7~4	3~2	1~0
y	cb	cr

The '**multi_brdr_clr**' value is located in the range 0 ~ 255 and each value represents 256 pseudo color. The border of multi-channel display is colored by using '**multi_brdr_clr**' register values.

Y = (0 ~ 15) x 16
Cb = (0 ~ 3) x 64 + 32, Cr = (0 ~ 3) x 64 + 32

Table 17. The Color Map

	White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
y	1011	1010	1000	0111	0101	0100	0010	0001
cb	01	00	10	01	10	01	11	01
cr	01	10	00	00	10	11	01	01
hexa. value	b5	a2	88	74	5a	47	2c	15

6.8 pip_mode(0000 0110)

			4	3-2	1	0
reduce	v_sel	h_sel	pip_empty	brdr_width	pip_size	pip_sel

pip_sel	DESCRIPTION
0	ATV main display, NTSC/VGA PIP
1	NTSC/VGA main display, ATV PIP

pip_size	DESCRIPTION
0	Small size PIP
1	Large size PIP

brdr_width	DESCRIPTION
00	PIP and multi-channel border width is 2 pixels
01	PIP and multi-channel border width is 4 pixels
10	PIP and multi-channel border width is 6 pixels
11	PIP and multi-channel border width is 8 pixels

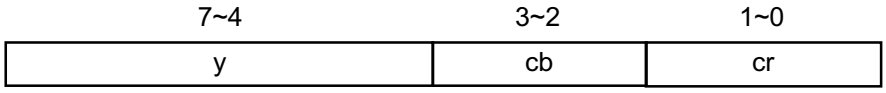
pip_empty	DESCRIPTION
0	Normal PIP display
1	If this bit is set, it means that there is no PIP data. The predetermined color of '**pip_win_clr**' is displayed in the PIP window.

h_sel	DESCRIPTION
0	Horizontally 5% crop when reduce is '1'.
1	Horizontally 10% 100 crop when reduce is '1'.

v_sel	DESCRIPTION
0	Vertically 5% crop when reduce is '1'.
1	Vertically 10% crop when reduce is '1'.

reduce	DESCRIPTION
0	Normal PIP display
1	Crop the boundary part of PIP image.

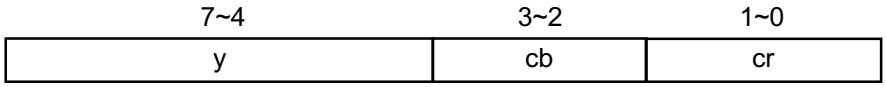
6.9 pip_brdr_clr(0100 0111) – red



The '**pip_brdr_clr**' value is located in the range 0 ~ 255 and each value represents 256 pseudo color.

The color map is the same as that of the '**multi_brdr_clr**'. (See Table 17)

6.10 pip_win_clr(0111 0100) - green



The '**pip_win_clr**' value is used when '**pip_empty**' flag is set to '1'.

The color map is the same as that of the '**multi_brdr_clr**'. (See Table 17)

6.11 pip_pos_x(001 1110 0000)

This 2-byte register defines the x-start position of PIP image in 1080x1920 display area. The register value range is 0 ~ 1919. The register value must be selected thus all PIP windows are located in the active display area. This value must be changed synchronizing with the '**multi_chnl_pos**' register in the multi-PIP display mode. The following table shows the required register values for proper operations of Multi-PIP display functions.

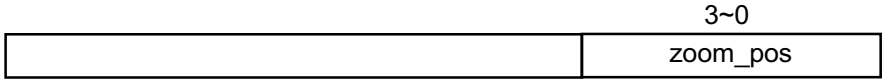
multi_chnl_pos	0, 4, 8, 12	1, 5, 9, 13	2, 6, 10, 14	3, 7, 11, 15
Required register value	0	480	960	1440

6.12 pip_pos_y(00 1000 1000)

This 2-byte register defines the y-start position of PIP image in 1080x1920 display area. The value of '**pip_pos_y * 2**' is used for calculating vertical location. The register value range is 0 ~ 539. This register value must be selected thus all PIP window is located in the active display area. This value must be changed synchronizing with the '**multi_chnl_pos**' register in the Multi-PIP display mode. The following table shows the required register values for proper operations of Multi-PIP functions.

multi_chnl_pos	0, 1, 2, 3	4, 5, 6, 7	8, 9, 10, 11	12, 13, 14, 15
Required register value	0	136	272	408

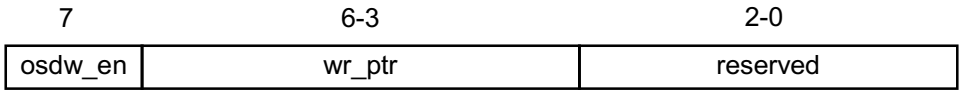
6.13 zoom_pos(xxxx 0000)



The '**zoom_pos**' value range is 0 ~ 15 and each value represents the zoom position of active display area.

zoom_pos	**Zooming Position**	**zoom_pos**	**Zooming Position**
0	Upper left part	1	Upper center part
2	Upper right part	3	Undefined
4	Medium left part	5	Medium center part
6	Medium right part	7	Undefined
8	Lower left part	9	Lower center part
10	Lower right part	11 ~ 15	Undefined

6.14 osd_mode(0000 0xxx)



osdw_en	**DESCRIPTION**
0	OSD write disable
1	OSD write enable

I^2C has 16-bit address range that can access only 8-row address of SDRAM. Therefore in order to access all (128-row address) OSD buffers '**wr_ptr**' values are added, and they constitute MSB of SDRAM address. For OSD data write operation, '**lutw_en**' bit of '**lut_sel**' register must be set to '0', and '**osdw_en**' bit of '**osd_mode**' register must be set to '1'.

6.15 sd_pos_x(0010 1000)

This register defines the x-start position of SD format image in 1080x1920 display area. The proper register value range is 0 ~ 79. If this register value is '0', the SD active image is displayed in the left end of display, and if this register value is '79', the SD active image is displayed in the right end of display. '**sd_pos_x * 8**' is used for calculating horizontal location.

6.16 sd_pos_y(xx01 1110)

This register defines the y-start position of SD format image in 1080x1920 display area. The proper register value range is 0 ~ 59. Minimum resolution is 1 pixel. If this register value is '0', SD active image is displayed in the upper part of display, and if this register value is '59', SD active image is displayed in the lower part of display.

6.17 nvin_h(x000 0000)

This register selects the horizontal active position of NTSC/VGA input. The proper register value range is 0 ~ 111. In NTSC input mode, HSYNC signal is synchronized with image data, and recommended register value is '0'. In VGA and SVGA input mode, the VDP interfaces with HD signal that is not synchronized with image data. In this case, the register value is used for the interface active image data. The recommended register value for VGA is '48' and for SVGA is '72'. Slight adjustment may be needed for exact interface.

6.18 nvin_v(xx00 0000)

This register selects the vertical active position of NTSC/VGA input. The proper register value range is 0 ~ 43. In NTSC input mode, VSYNC signal is synchronized with image data, and recommended register value is '0'. In VGA and SVGA input mode, the VDP interfaces with VD signal that is not synchronized with image data. In this case, the register value is used for interface active image data. The recommended register value for VGA is '32' and for SVGA is '28'. Slight adjustment may be needed for exact interface.

6.19 nvinputformat(xxx0 0--0) : - Means read only bit

	4	3	2~1	0
	lock_off	nt_type	nv_mode	cbcr

CBCR	DESCRIPTION
0	In 422 input format, chrom. data is inputted in order of cb, cr
1	In 422 input format, chrom. data is inputted in order of cr, cb

nt_type	DESCRIPTION
0	480x768 input format
1	480x720 input format

lock_off	DESCRIPTION
0	Display sync is locked to the ntsc input
1	Display sync is unlocked to the ntsc input

The '**nv_mode**' bits are the read only bits. nv_mode[1] represents NTSC_VGA input pin value and nv_mode[0] represents NV_MODE input pin value.

6.20 atvformat(x--- ----) : This register operates in read only mode.

	6	5	4~3	2~0
	60Hz	interlaced	fm_rate	format

FORMAT	DESCRIPTION
000	HD 1920 x 1080
001	HD 1280 x 720
010	HD 704 x 480
011	SD 704 x 480
100	SD 640 x 480

fm_rate	DESCRIPTION
00	60Hz
01	30Hz
10	24Hz

interlaced	DESCRIPTION
0	Interlaced
1	Progressive

60Hz	DESCRIPTION
0	60Hz
1	59.94Hz

The VDP receives ATV format data from the Video Decoder. This register value indicates the present ATV format information.

6.21 arc_mode(x100 0000)

	6 ~ 4	3	2	1	0
	v_offset	full 16 : 9	large	v_wide	h_wide

h_wide	DESCRIPTION
0	4:3 display of SD or NTSC input
1	Horizontal wide display of 4:3 SD or NTSC input

v_wide	DESCRIPTION
0	4:3 display of SD or NTSC input
1	Vertical wide display of 4:3 SD or NTSC input

large	DESCRIPTION
0	4:3 display of SD or NTSC input
1	Full display of 4:3 SD or NTSC input with vertical offset

full 16:9	DESCRIPTION
0	Small display of 16:9 SD input
1	Full display of 16:9 SD input

The '**v_offset**' value represents the vertical offset position when 'large' bit is set to '1'.

When '**v_offset**' value is '0', the upper part of display is displayed, and when '**v_offset**' value is '7', the lower part of display is displayed.

If input format is not progressive frame format, '**v_offset**' value can be 0, 2, 4, and 6. The all '**v_offset**' values can be used in progressive frame input format.

6.22 deint_th(0001 1000)

This register value selects the threshold value of 3-D de-interlacer. It is not necessary to change this register value in normal display mode. When the value is '0x00', only intra-field linear interpolation method is used for de-interlacing.

6.23 test-ptrn(xxxx x000)

This register selects 7 test patterns. The '0x00' value displays normal ATV or NTSC image, and '0x01' ~ '0x07' values select the following test patterns. The VDP automatically generates proper test patterns in GBR/YPbPr display modes.

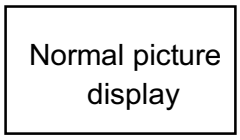


Figure 40(a).test_ptrm=000

Figure 40(b).test_ptrm=001:Full white

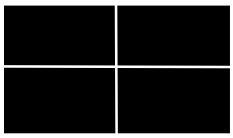


Figure 40(c).test_ptrm=0:Cross

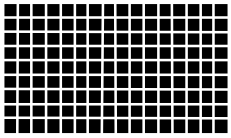


Figure 40(d) test_ptrn=011:Cross

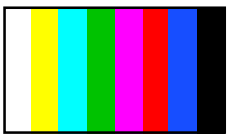


Figure 40(e).test_ptrm=100:Color

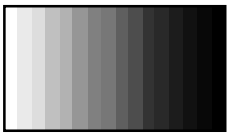


Figure 40(f).test_ptrm=101:Gray scale(16 level)

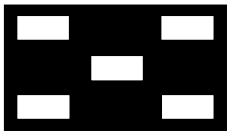


Figure 40(g).test_ptrm=110:Write

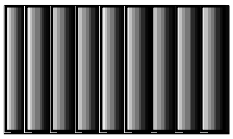


Figure 40(h).test_ptrm=111:Ramp

Figure 40. Seven Test Patterns

6.24 osd_base(x000 0000)

This register value selects the OSD base address of the VDP. In host interface mode, OSD memory address can be calculated by the following rule with h_addr[8]='1'.

wr_ptr[3:0]	osd_base[6:0]	h_addr[7:1]

6.25 dma_block_size(x000 0000)

This register value determines the number of DMA block size in DMA operation mode. The DMA block has 16bitx128bit data. If the register value is '0', only one DMA block can be loaded. If the register value is 'n', n+1 DMA blocks are loaded.

6.26 dma_mode(xxxx 0000)

	3 ~ 2	1	0
	dma_idle	dma_mode	dma_start

dma_start	DESCRIPTION
0	dma_disable
1	dma_enable

dma_mode	DESCRIPTION
0	burst_mode
1	cycle steel mode

In cycle steel mode, periodically, the VDP activates DMA_REQ_N signals, receives four 16-bit data, and deactivates DMA_REQ_N signals within 16 ~ 128 clock, until receiving 128 16-bit data. The '**dma_idle**' register selects DMA_REQ_N deactivation period between DMA request cycle.

dma_idle	DESCRIPTION
00	16 clock period of DMA negation
01	32 clock period of DMA negation
10	64 clock period of DMA negation
11	128 clock period of DMA negation

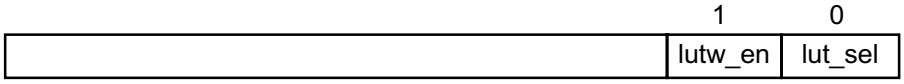
6.27 host_wait(1111 1111)

This register value determines the host_wait (T_{READY}) time. Small value of this register can reduce the register and memory access time.

6.28 nonactive_val(0001 0000)

This register value determines the gray level value of non-active region in SD and NTSC display mode. The register value also determines the gray level value of background in Multi-PIP display mode.

6.29 lut_sel(xxxx xx00)

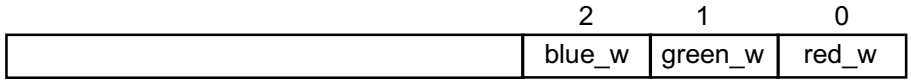


lut_sel	DESCRIPTION
0	LUT0: write mode, LUT1: read mode
1	LUT1: write mode, LUT0: read mode

lutw_en	DESCRIPTION
0	LUT write disable
1	LUT write enable

For lookup table access, '**pltw_en**' bit of '**palette_sel**' register and '**osdw_en**' bit of '**osd_mode**' register must be set to '0', and '**lutw_en**' bit of '**lut_sel**' register must be set to '1'. For OSD data write operation, '**pltw_en**' bit of '**palette_sel**' register and '**lutw_en**' bit of '**lut_sel**' register must be set to '0', and '**osdw_enb**' bit of '**osd_mode**' register must be set to '1'.

6.30 lutwrgb(xxxx x111)



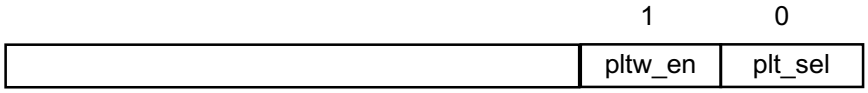
red_w	DESCRIPTION
0	Red component LUT write enable
1	Red component LUT write disable

green_w	DESCRIPTION
0	Green component LUT write enable
1	Green component LUT write disable

blue_w	DESCRIPTION
0	Blue component LUT write enable
1	Blue component LUT write disable

The VDP has two sets of lookup table buffers and each set has red, green, and blue component lookup table. If one lookup table is selected in write mode, the other is automatically selected in read mode, and they are switched on the falling edge of 'VDOUT_N' sync signal. In lookup table write mode, if two or three lookup table data are loaded at a time, the corresponding **red_w**, **green_w**, or **blue_w** register bit values can be set to '0' simultaneously. After power-on reset, the VDP initializes one lookup table to bypass mode automatically.

6.31 palette_sel(xxxx xx00)

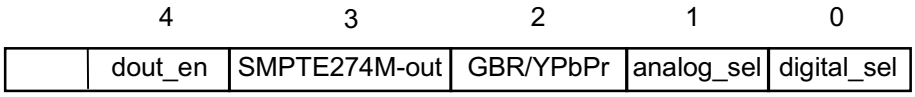


plt_sel	DESCRIPTION
0	Select 0 ~127 color palettes
1	Select 128 ~ 255 color palettes

pltw_en	DESCRIPTION
0	Palette write disable
1	Palette write enable

For color palette access, '**plt_en**' bit of '**palette_sel**' register must be set to '1', and '**lutw_en**' bit of '**lut_sel**' register and '**osdw_en**' bit of '**osd_mode**' register must be set to '0'.

6.32 disp_sel(xxx1 0100)



digital_sel	DESCRIPTION
0	Constant digital output value in the sync interval
1	Three-level value in the sync interval

analog_sel	DESCRIPTION
0	Constant analog output value in the sync interval
1	Three-level value in the sync interval

GBR/YPbPr	DESCRIPTION
0	YPbPr analog/digital output
1	GBR analog/digital output

SMPTE274M_out	DESCRIPTION
0	Normal digital output
1	SMPTE 274M digital output

dout_en	DESCRIPTION
0	Digital output disable
1	Digital output enable

6.33 osd_en(xx00 x000)

	5	4	3	2	1	0
reserved	l1_an_en	l0_an_en	reserved	l1_ en	l0_en	cur_en

cur_en	DESCRIPTION
0	Cursor layer disable
1	Cursor layer enable

l0_en	DESCRIPTION
0	OSD layer 0 disable
1	OSD layer 0 enable

l1_en	DESCRIPTION
0	OSD layer 1 disable
1	OSD layer 1 enable

l0_an_en	DESCRIPTION
0	OSD layer 0 animation disable
1	OSD layer 0 animation enable

l0_an_en	DESCRIPTION
0	OSD layer 1 animation disable
1	OSD layer 1 animation enable

6.34 osd_load(xxxx xxx0)

	0
reserved	osd_load

osd_load	DESCRIPTION
0	Get OSD control register values
1	Load OSD register values to the OSD block

7. Electrical Characteristics

7.1 Absolute Maximum Rating

SYMBOL	PARAMETERS	VALUES	UNIT
V_{DD}	Power supply voltage	-0.33 to 5.5	V
V_I	Digital input voltage	-0.33 to V_{DD} + 0.5	V
Vo	Digital output voltage	-0.33 to V_{DD} + 0.5	V
T_{stg}	Storage temperature	-55 to 125	°C
P_d	Power dissipation	5.0	W

Note : Absolute Maximum Rating means that the safety of the device cannot be guaranteed beyond these values, and this doesn't imply that the device should be operated within these limits.

7.2 Recommended Operating Range

SYMBOL	PARAMETERS	VALUES	UNIT
V_{DD}	Power supply voltage	3.3 ± 10%	V
T_{opr}	Operating temperature	0 to 70	°C

7.3 DC Characteristics (VDD = 3.3 V±10%, TA = 0 ~ 70°C)

SYMBOL	PARAMETERS	MIN	MAX	UNIT	TEST CONDITION
V_{IH}	Input high voltage	0.7xV_{DD}	VDD+0.33	V	
V_{IL}	Input low voltage	-0.33	0.2xVDD	V	
V_{OH}	Output high voltage	2.4	-	V	
V_{OL}	Output low voltage	-	0.4	V	
I_{CC}	Operating current	-	1000	mA	

7.4 AC Characteristics (VDD = 3.3 V±10%, TA = 0 ~ 70°C)

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	REMARK
T_S	Data/Enable setup time	0	-	-	nS	below
T_H	Data/Enable hold time	3	-	-	nS	below
T_D	Output delay time	-	-	14	nS	below
T_L	Reset low time	20	-	-	Cycle	
T_I	Data valid time after reset HIGH	3	-	-	Cycle	
F_{OPR}	Operating frequency	-	74.25	-	MHz	clk74
	Operating frequency	-	65	-	MHz	clknv
	Operating frequency	-	54	-	MHz	clkvd

Note:1. Setup/Hold time on rising edge of clk
2. Output data delay time on rising edge of clk
3. *Test Condition : Load Capacitance = 50pF

Data/Enable Setup/Hold Time and Output Delay Time

CLOCK	INPUT	T_S	T_H	REMARK	CLOCK	OUTPUT	T_D	REMARK
CLK74	SDRAM_DATA	0	3	64-bit data	CLK74	WE_N	12	SDRAM interface 11-bit address
CLKVD	NV_MODE	0	3		CLK74	CS_N	12	
CLKVD	D_INFO_WIN	0	3	**Core Test**	CLK74	RAS_N	12	
CLKVD	FFP_N	0	3		CLK74	CAS_N	12	
CLKVD	MBFI	0	3		CLK74	SDRAM_ADDR	12	
CLKVD	SWIN	0	3		CLK74	BANK	12	64-bit data
CLKVD	MBWIN	0	3		CLK74	SDRAM_DATA	12	
CLKVD	PDWIN	0	3		CLK74	FIELDSYNC	14	
CLKVD	PSTR	0	3		CLK74	VSYNCOUT_N	14	
CLKVD	DIS_INFO	0	3		CLK74	H60_N	14	
CLKVD	P_FRM	0	3		CLK74	HDOUT_N	14	
CLKVD	PDATA	0	3	32-bit data	CLK74	VDOUT_N	14	**Core Test**
CLKVD	SDA	0	3		CLK74	HSYNCOUT_N	14	
CLKVD	SCL	0	3		CLK74	RDOUT	14	10-bit data
CLKNV	NV_VD_N	0	3		CLK74	GDOUT	14	10-bit data
CLKNV	NV_HD_N	0	3		CLK74	BDOUT	14	10- bit data
CLKNV	NV_C	0	3	8-bit data	CLKVD	P_WAIT	14	
CLKNV	NV_Y	0	3	8-bit data	CLKVD	SDA	14	
CLKNV	NV_FIELD	0	3					

8. Package Mechanical Data

8.1 Package Pin Out

PIN	TYPE	NAME	PIN	TYPE	NAME
1	GND	**VSS**	44	GND	**VSS**
2	I	**CLKNV**	45	I/O	**SDRAM_DATA[62]**
3	PWR	**VDD**	46	I/O	**SDRAM_DATA[63]**
4	I/O	**SDRAM_DATA[32]**	47	GND	**VSS**
5	GND	**VSS**	48	I	**NV_Y[0]**
6	I/O	**SDRAM_DATA[33]**	49	I	**NV_Y[1]**
7	I/O	**SDRAM_DATA[34]**	50	PWR	**VDD**
8	PWR	**VDD**	51	I	**NV_Y[2]**
9	I/O	**SDRAM_DATA[35]**	52	I	**NV_Y[3]**
10	I/O	**SDRAM_DATA[36]**	53	GND	**VSS**
11	GND	**VSS**	54	I	**NV_Y[4]**
12	I/O	**SDRAM_DATA[37]**	55	I	**NV_Y[5]**
13	I/O	**SDRAM_DATA[38]**	56	PWR	**VDD**
14	I/O	**SDRAM_DATA[39]**	57	I	**NV_Y[6]**
15	I/O	**SDRAM_DATA[40]**	58	I	**NV_Y[7]**
16	PWR	**VDD**	59	GND	**VSS**
17	I/O	**SDRAM_DATA[41]**	60	I	**NV_C[0]**
18	I/O	**SDRAM_DATA[42]**	61	I	**NV_C[1]**
19	GND	**VSS**	62	PWR	**VDD**
20	I/O	**SDRAM_DATA[43]**	63	I	**NV_C[2]**
21	I/O	**SDRAM_DATA[44]**	64	I	**NV_C[3]**
22	I/O	**SDRAM_DATA[45]**	65	GND	**VSS**
23	I/O	**SDRAM_DATA[46]**	66	I	**NV_C[4]**
24	PWR	**VDD**	67	I	**NV_C[5]**
25	I/O	**SDRAM_DATA[47]**	68	PWR	**VDD**
26	I/O	**SDRAM_DATA[48]**	69	I	**NV_C[6]**
27	I/O	**SDRAM_DATA[49]**	70	I	**NV_C[7]**
28	I/O	**SDRAM_DATA[50]**	71	GND	**VSS**
29	GND	**VSS**	72	I	**NTSC_VGA**
30	I/O	**SDRAM_DATA[51]**	73	I	**NV_MODE**
31	I/O	**SDRAM_DATA[52]**	74	I	**NV_HD_N**
32	PWR	**VDD**	75	I	**NV_VD_N**
33	I/O	**SDRAM_DATA[53]**	76	I	**HOST_SEL**
34	I/O	**SDRAM_DATA[54]**	77	GND	**VSSA**
35	I/O	**SDRAM_DATA[55]**	78	I	**REF**
36	I/O	**SDRAM_DATA[56]**	79	PWR	**VDDA**
37	GND	**VSS**	80	I	**ADJ**
38	I/O	**SDRAM_DATA[57]**	81	GND	**VSSA**
39	I/O	**SDRAM_DATA[58]**	82	O	**ROUT/PROUT**
40	PWR	**VDD**	83	PWR	**VDDA**
41	I/O	**SDRAM_DATA[59]**	84	O	**GOUT/YOUT**
42	I/O	**SDRAM_DATA[60]**	85	GND	**VSSA**
43	I/O	**SDRAM_DATA[61]**	86	O	**BOUT/PBOUT**

Package Pin Out*(Continued)*

PIN	TYPE	NAME	PIN	TYPE	NAME
87	PWR	**VDDA**	133	I/O	**CB/BDOUT[7]/H_ADDR[6]**
88	O/Z	**READY**	134	I/O	**CB/BDOUT[6]/H_ADDR[5]**
89	O	**CR/RDOUT[1]/DMA_ACK_N**	135	I/O	**CB/BDOUT[5]/H_ADDR[4]**
90	GND	**VSS**	136	PWR	**VDD**
91	I	**NV_FIELD**	137	I/O	**CB/BDOUT[4]/H_ADDR[3]**
92	O	**HDOUT_N**	138	I/O	**CB/BDOUT[3]/H_ADDR[2]**
93	O	**VDOUT_N**	139	GND	**VSS**
94	PWR	**VDD**	140	I/O	**CB/BDOUT[2]/H_ADDR[1]**
95	I/O	**CR/RDOUT[0]/DMA_REQ_N**	141	PWR	**VDD**
96	GND	**VSS**	142	I/O	**YD/GDOUT[1]/H_CS_N**
97	O	**HSYNCOUT_N**	143	GND	**VSS**
98	O	**VSYNCOUT_N**	144	O	**SCAN**
99	O	**FIELDSYNC**	145	O	**SCAN**
100	O	**H60_N**	146	O	**SCAN**
101	PWR	**VDD**	147	O	**SCAN**
102	I/O	**SDA**	148	O	**SCAN**
103	GND	**VSS**	149	O	**SCAN**
104	I	**SCL**	150	I/O	**YD/GDOUT[0]/H_RW_N**
105	PWR	**VDD**	151	I/O	**CB/BDOUT[1]/D_STB_N**
106	I/O/Z	**CR/RDOUT[9]/H_DATA[15]**	152	GND	**VSS**
107	I/O/Z	**CR/RDOUT[8]/H_DATA[14]**	153	I/O	**BD/CBOUT[0]/READY_TYPE**
108	GND	**VSS**	154	PWR	**VDD**
109	I/O/Z	**CR/RDOUT[7]/H_DATA[13]**	155	GND	**VSS**
110	I/O/Z	**CR/RDOUT[6]/H_DATA[12]**	156	GND	**VSS**
111	I/O/Z	**CR/RDOUT[5]/H_DATA[11]**	157	GND	**VSS**
112	PWR	**VDD**	158	GND	**VSS**
113	I/O/Z	**CR/RDOUT[4]/H_DATA[10]**	159	O	**CLK74OUT**
114	I/O/Z	**CR/RDOUT[3]/H_DATA[9]**	160	GND	**VSS**
115	GND	**VSS**	161	I	**CLK74IN**
116	I/O/Z	**CR/RDOUT[2]/H_DATA[8]**	162	GND	**VSS**
117	I/O/Z	**YD/GDOUT[9]/H_DATA[7]**	163	GND	**VSS**
118	PWR	**VDD**	164	GND	**VSS**
119	I/O/Z	**YD/GDOUT[8]/H_DATA[6]**	165	GND	**VSS**
120	I/O/Z	**YD/GDOUT[7]/H_DATA[5]**	166	GND	**VSS**
121	GND	**VSS**	167	I	**P_FRM**
122	I/O/Z	**YD/GDOUT[6]/H_DATA[4]**	168	O	**NC**
123	I/O/Z	**YD/GDOUT[5]/H_DATA[3]**	169	O	**NC**
124	GND	**VSS**	170	O	**P_WAIT**
125	I/O/Z	**YD/GDOUT[4]/H_DATA[2]**	171	PWR	**VDD**
126	I/O/Z	**YD/GDOUT[3]/H_DATA[1]**	172	I	**PDATA[31]**
127	PWR	**VDD**	173	I	**PDATA[30]**
128	I/O/Z	**YD/GDOUT[2]/H_DATA[0]**	174	GND	**VSS**
129	I/O	**CB/BDOUT[9]/H_ADDR[8]**	175	I	**PDATA[29]**
130	GND	**VSS**	176	I	**PDATA[28]**
131	I/O	**CB/BDOUT[8]/H_ADDR[7]**	177	PWR	**VDD**
132	PWR	**VDD**	178	I	**PDATA[27]**

Package Pin Out*(Continued)*

PIN	TYPE	NAME	PIN	TYPE	NAME
179	I	**PDATA[26]**	225	GND	**VSS**
180	GND	**VSS**	226	I	**PDWIN**
181	I	**PDATA[25]**	227	I	**D_INFO_WIN**
182	I	**PDATA[24]**	228	I	**DIS_INFO**
183	I	**PDATA[23]**	229	PWR	**VDD**
184	PWR	**VDD**	230	I	**FFP_N**
185	I	**PDATA[22]**	231	I	**MBFI**
186	I	**PDATA[21]**	232	GND	**VSS**
187	I	**PDATA[20]**	233	I	**MBWIN**
188	I	**PDATA[19]**	234	I	**SWIN**
189	GND	**VSS**	235	I	**RESET_N**
190	I	**PDATA[18]**	236	I	**RESETS_N**
191	I	**PDATA[17]**	237	PWR	**VDD**
192	I	**PDATA[16]**	238	I/O	**SDRAM_DATA[0]**
193	PWR	**VDD**	239	GND	**VSS**
194	I	**PDATA[15]**	240	I/O	**SDRAM_DATA[1]**
195	I	**PDATA[14]**	241	I/O	**SDRAM_DATA[2]**
196	GND	**VSS**	242	PWR	**VDD**
197	I	**PDATA[13]**	243	I/O	**SDRAM_DATA[3]**
198	I	**PDATA[12]**	244	I/O	**SDRAM_DATA[4]**
199	PWR	**VDD**	245	I/O	**SDRAM_DATA[5]**
200	I	**PDATA[11]**	246	I/O	**SDRAM_DATA[6]**
201	I	**PDATA[10]**	247	GND	**VSS**
202	GND	**VSS**	248	I/O	**SDRAM_DATA[7]**
203	I	**PDATA[9]**	249	I/O	**SDRAM_DATA[8]**
204	I	**PDATA[8]**	250	PWR	**VDD**
205	PWR	**VDD**	251	I/O	**SDRAM_DATA[9]**
206	I	**PDATA[7]**	252	I/O	**SDRAM_DATA[10]**
207	I	**PDATA[6]**	253	I/O	**SDRAM_DATA[11]**
208	GND	**VSS**	254	I/O	**SDRAM_DATA[12]**
209	I	**PDATA[5]**	255	GND	**VSS**
210	I	**PDATA[4]**	256	I/O	**SDRAM_DATA[13]**
211	PWR	**VDD**	257	I/O	**SDRAM_DATA[14]**
212	I	**PDATA[3]**	258	PWR	**VDD**
213	I	**PDATA[2]**	259	I/O	**SDRAM_DATA[15]**
214	GND	**VSS**	260	I/O	**SDRAM_DATA[16]**
215	I	**PDATA[1]**	261	I/O	**SDRAM_DATA[17]**
216	I	**PDATA[0]**	262	GND	**VSS**
217	PWR	**VDD**	263	I/O	**SDRAM_DATA[18]**
218	I	**PSTR[1]**	264	I/O	**SDRAM_DATA[19]**
219	I	**PSTR[0]**	265	I/O	**SDRAM_DATA[20]**
220	GND	**VSS**	266	PWR	**VDD**
221	I	**CLKVD**	267	PWR	**VDD**
222	PWR	**VDD**	268	I/O	**SDRAM_DATA[21]**
223	PWR	**VDD**	269	I/O	**SDRAM_DATA[22]**
224	I	**CLK74**	270	I/O	**SDRAM_DATA[23]**

Package Pin Out*(Continued)*

PIN	TYPE	NAME	PIN	TYPE	NAME
271	GND	**VSS**	288	O	**SDRAM_ADDR[3]**
272	GND	**VSS**	289	O	**SDRAM_ADDR[4]**
273	I/O	**SDRAM_DATA[24]**	290	GND	**VSS**
274	I/O	**SDRAM_DATA[25]**	291	O	**SDRAM_ADDR[5]**
275	I/O	**SDRAM_DATA[26]**	292	O	**SDRAM_ADDR[6]**
276	PWR	**VDD**	293	O	**SDRAM_ADDR[7]**
277	I/O	**SDRAM_DATA[27]**	294	O	**SDRAM_ADDR[8]**
278	I/O	**SDRAM_DATA[28]**	295	PWR	**VDD**
279	GND	**VSS**	296	O	**SDRAM_ADDR[9]**
280	I/O	**SDRAM_DATA[29]**	297	O	**SDRAM_ADDR[10]**
281	I/O	**SDRAM_DATA[30]**	298	O	**BANK**
282	I/O	**SDRAM_DATA[31]**	299	PWR	**VDD**
283	GND	**VSS**	300	O	**WE_N**
284	O	**SDRAM_ADDR[0]**	301	O	**CAS_N**
285	PWR	**VDD**	302	O	**RAS_N**
286	O	**SDRAM_ADDR[1]**	303	O	**CS_N**
287	O	**SDRAM_ADDR[2]**	304	GND	**VSS**

8.2 Package Dimensions

PACKAGE CONTROL OUTLINE, 304 Pin HQFP, 40x40 mm BODY,

1.30/0.43 mm FORM, 3.80 mm THICK

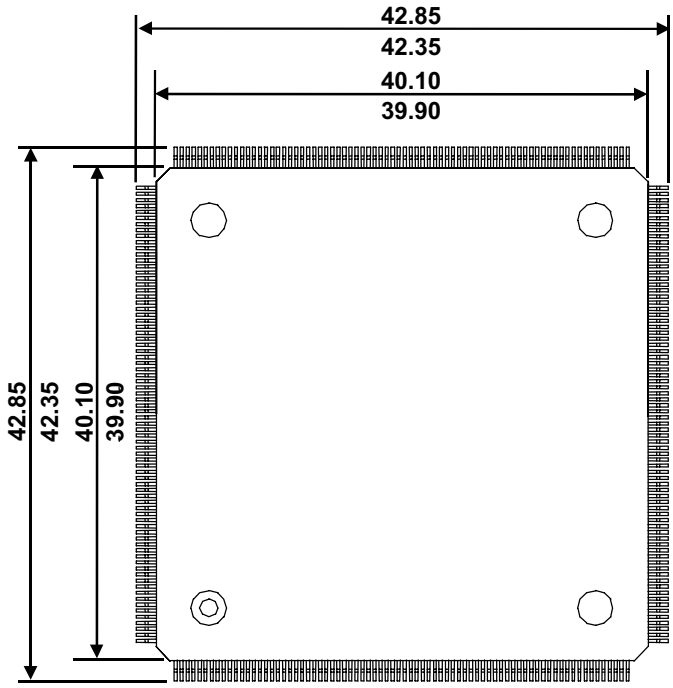


Figure 41. Physical Dimensions 1

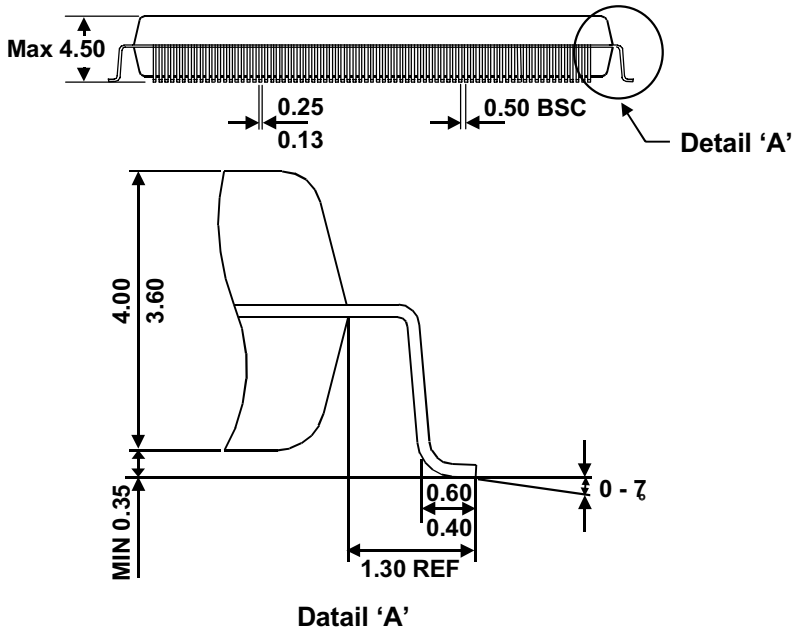


Figure 42. Physical Dimensions 2