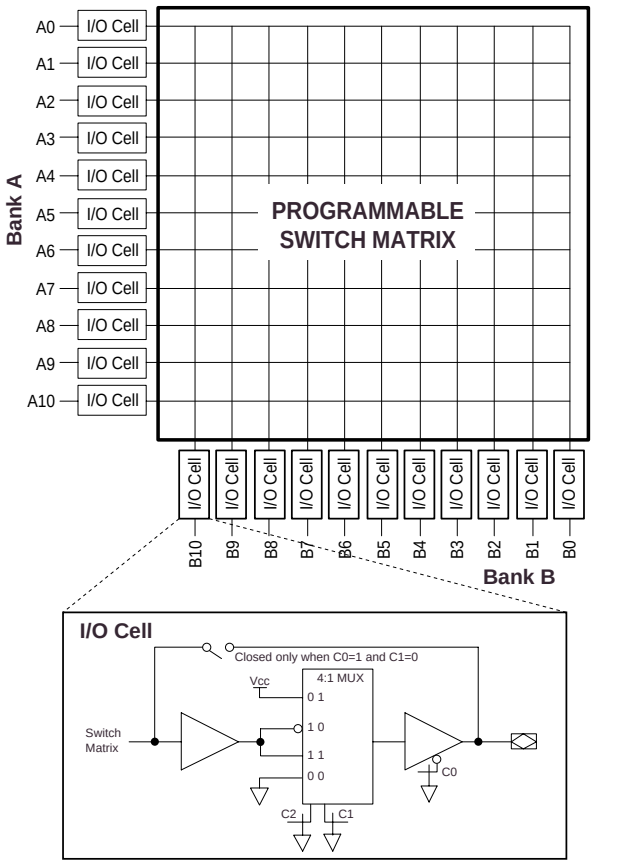
ispGDS22/18/14

in-system programmable Generic Digital Switch™

Features

- **HIGH-SPEED SWITCH MATRIX**
  - **— 7.5 ns Maximum Propagation Delay**
  - **— Typical Icc = 25 mA**
  - **— UltraMOS® Advanced CMOS Technology**
- **FLEXIBLE I/O MACROCELL**
  - **— Any I/O Pin Can be Input, Output, or Fixed TTL High or Low**
  - **— Programmable Output Polarity**
  - **— Multiple Outputs Can be Driven by One Input**
- **IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)**
  - **— Programming Time of Less Than One Second**
  - **— 4-Wire Programming Interface**
  - **— Minimum 10,000 Program/Erase Cycles**
- **E^2 CELL TECHNOLOGY**
  - **— Non-Volatile Reprogrammable Cells**
  - **— 100% Tested/100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **APPLICATIONS INCLUDE:**
  - **— Software-Driven Hardware Configuration**
  - **— Multiple DIP Switch Replacement**
  - **— Software Configuration of Add-In Boards**
  - **— Configurable Addressing of I/O Boards**
  - **— Multiple Clock Source Selection**
  - **— Cross-Matrix Switch**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

Functional Block Diagram (ispGDS22)



Description

The Lattice Semiconductor ispGDS™ family is an ideal solution for reconfiguring system signal routing or replacing DIP switches used for feature selection. With today's demands for customer ease of use, there is a need for hardware which is easily reconfigured electronically without dismantling the system. The ispGDS devices address this challenge by replacing conventional switches with a software configurable solution. Since each I/O pin can be set to an independent logic level, the ispGDS devices can replace most DIP switch functions with about half the pin count, and without the need for additional pull-up resistors. In addition to DIP switch replacement, the ispGDS devices are useful as signal routing cross-matrix switches. This is the only non-volatile device on the market which can provide this flexibility.

With a maximum tpd of 7.5ns, and a typical active Icc of only 25 mA, these devices provide maximum performance at very low power levels. The ispGDS devices may be programmed in-system, using 5 volt only signals, through a simple 4-wire programming interface. The ispGDS devices are manufactured using Lattice Semiconductor's advanced non-volatile E^2CMOS process which combines CMOS with Electrically Erasable (E^2) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

Each I/O macrocell can be configured as an input, an inverting or non-inverting output, or a fixed TTL high or low output. Any I/O pin can be driven by any other I/O pin in the opposite bank. A single input can drive one or more outputs in the opposite bank, allowing a signal (such as a clock) to be distributed to multiple destinations on the board, under software control. The I/Os accept and drive TTL voltage levels.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor is able to deliver 100% field programmability and functionality of all Lattice Semiconductor products. In addition, 10,000 erase/write cycles and data retention in excess of 20 years are specified.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
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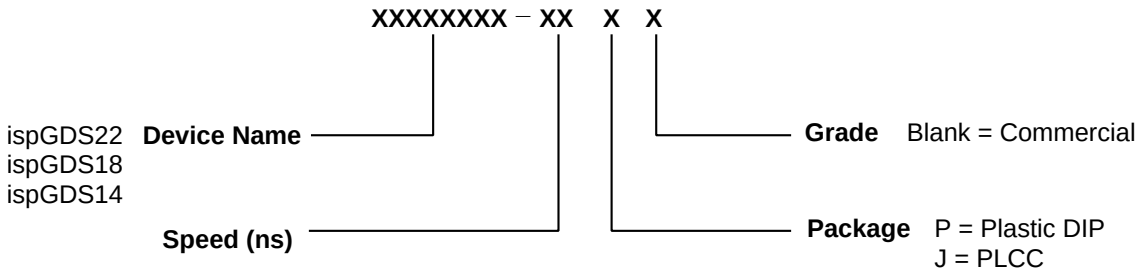
July 1997

ispGDS Ordering Information

Commercial Grade Specifications

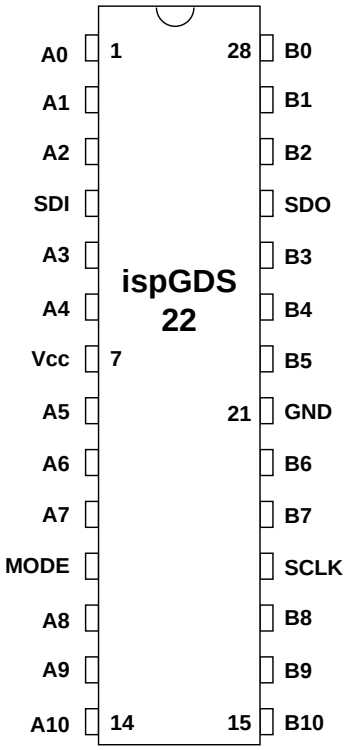
Matrix Size	I/O Pins	Tpd (ns)	Isb (mA)	Icc (mA)	Ordering #	Package
11 x 11	22	7.5	25	40	ispGDS22-7P	28-Pin Plastic DIP
					ispGDS22-7J	28-Lead PLCC
9 x 9	18	7.5	25	40	ispGDS18-7P	24-Pin Plastic DIP
7 x 7	14	7.5	25	40	ispGDS14-7P	20-Pin Plastic DIP
					ispGDS14-7J	20-Lead PLCC

Part Number Description

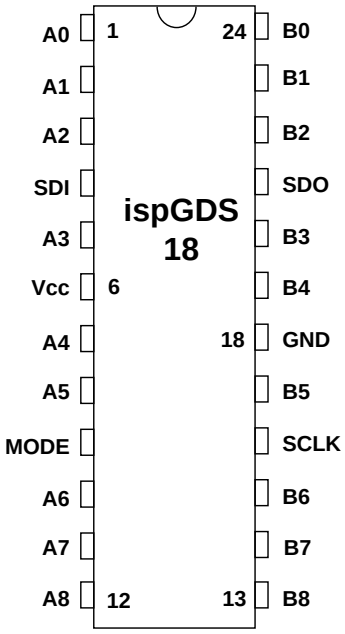


Pin Configuration

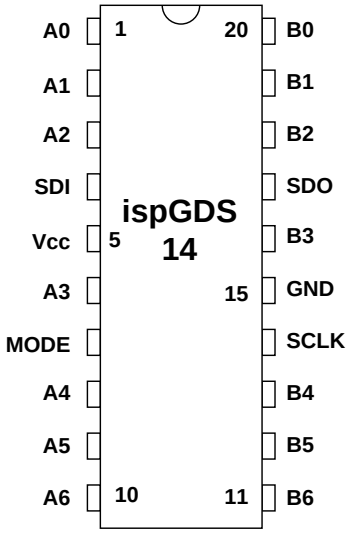
28-Pin DIP



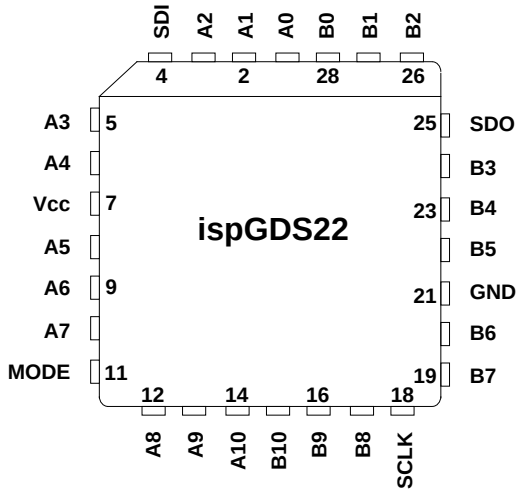
24-Pin DIP



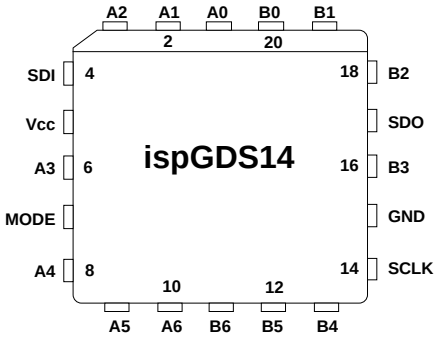
20-Pin DIP



28-Pin PLCC



20-Pin PLCC



ispGDS Family Overview

There are three members of the ispGDS family, the ispGDS22, ispGDS18, and ispGSD14. The numerical portion of the part name indicates the number of I/O cells available. All of the devices are available in a DIP package, with the ispGDS22 and ispGDS14 also available in a PLCC package. Each of the devices operate identically, with the only difference being the number of I/O cells available.

The ispGDS devices are all programmed through a four-pin interface, using TTL level signals. The four dedicated programming pins are named MODE, SDI, SDO, and SCLK. No high-voltage is needed, as the voltages needed for programming are generated internally. Programming of the entire device, including erasure, can be done in less than one second. During the programming operation, all I/O pins will be tri-stated. Further details of the programming process can be found in the In-System Programming section later in this datasheet.

The I/O cells in each device are divided equally into two banks (Bank A and Bank B). Each I/O cell can be configured as an input, an inverting output, a non-inverting output, or set to a fixed TTL high or low. A switch matrix connects the I/O banks, allowing an I/O cell in one bank to be connected to any of the I/O cells in the other bank. A single I/O cell configured as an input can drive one or more I/O cells in the other bank. The full I/O macrocell, which is identical for each of the I/O pins, is shown below. The allowable configurations are shown on the following page.

In-System Programmability

The ispGDS family of devices feature In-System Programmable technology. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via four TTL level logic interface signals. These four signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. For details on the operation of the internal state machine and programming of ispGDS devices please refer to the ISP Architecture and Programming section in this Data Book.

Device Programming

The ispGDS family of devices uses a standard JEDEC file, as used for programmable logic devices, to describe device programming information. Popular logic compilers, such as ABEL and CUPL, can produce the JEDEC files for these devices.

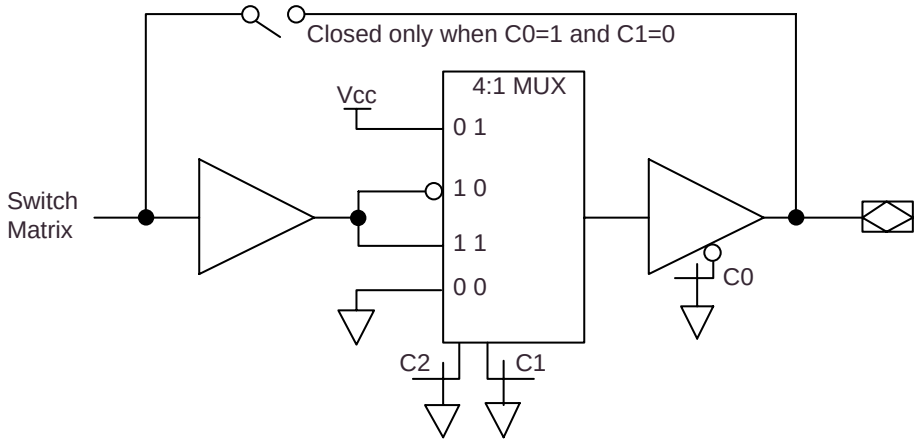
The JEDEC files can be used to program the ispGDS devices in a number of ways, which are shown in the section titled ISP Architecture and Programming.

Electronic Signature

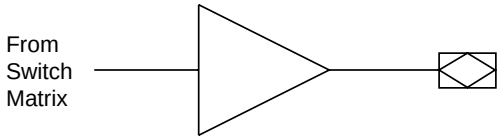
An electronic signature word is provided with every ispGDS device. It contains 32 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the fuse checksum in the JEDEC fusemap.

I/O Macrocell

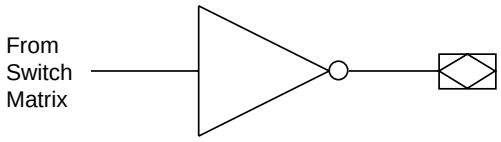


I/O Macrocell Configurations



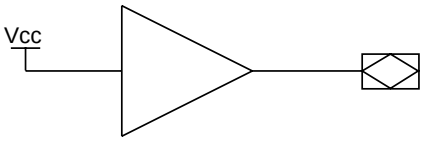
Configuration for Active High Output

- C0 = 0.
- C1 = 1.
- C2 = 1.



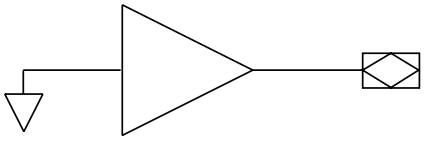
Configuration for Active Low Output

- C0 = 0.
- C1 = 0.
- C2 = 1.



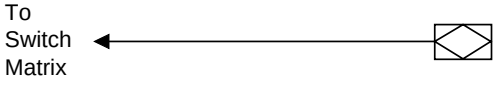
Configuration for Fixed TTL High Output

- C0 = 0.
- C1 = 1.
- C2 = 0.



Configuration for Fixed TTL Low Output

- C0 = 0.
- C1 = 0.
- C2 = 0.



Configuration for Dedicated Input

- C0 = 1.
- C1 = 0.
- C2 = 1.

Note 1: The development software configures all of the architecture control bits and checks for proper pin usage automatically.
Note 2: The default configuration for unused pins is for all configuration bits set to one, which produces a tri-stated output.

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Cond.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. $V_{in} = V_{IL}$ or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. $V_{in} = V_{IL}$ or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–130	mA

COMMERCIAL

I_{SB}	Standby Power Supply Current	Inputs = 0V Outputs open	L-7	—	15	25	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -7	—	25	40	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
$C_{I/O}$	I/O Capacitance (as input or output)	8	pF	V_{CC} = 5.0V, V_I = 2.0V

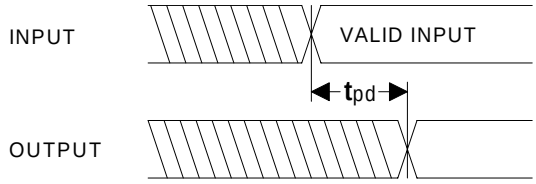
*Characterized but not 100% tested.

AC Switching Characteristics

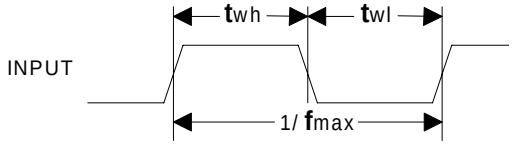
Over Recommended Operating Conditions

PARAMETER	TEST COND.	DESCRIPTION		COM MIN.	COM MAX.	UNITS
t_{pd}	A	Input to Output Delay	One Input Driving One Output	1	7.5	ns
f_{max}	A	Maximum Input Frequency	One Output Switching	—	50	MHz
t_{wh}	A	Input Pulse Duration, High		10	—	ns
t_{wl}	A	Input Pulse Duration, Low		10	—	ns

Switching Waveforms



Input to Output Delay



Input Pulse Width/ Fmax

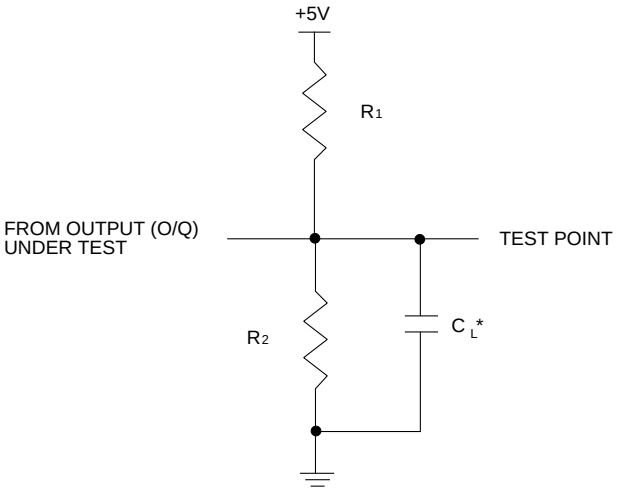
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

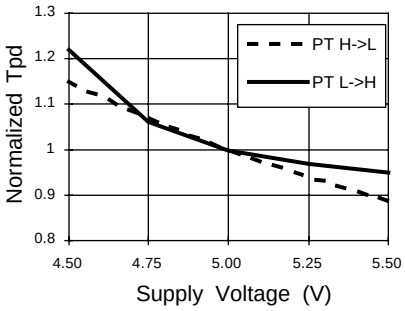
Test Condition	R_1	R_2	C_L
A	470Ω	390Ω	50pF



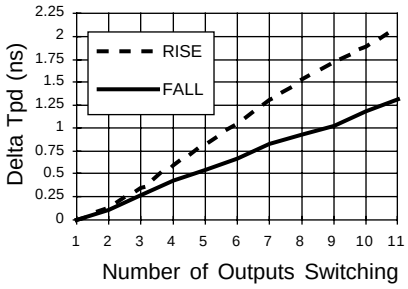
*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Typical AC and DC Characteristic Diagrams

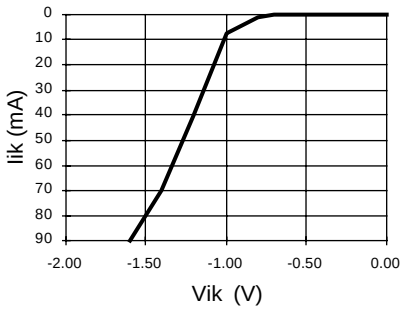
Normalized Tpd vs Vcc



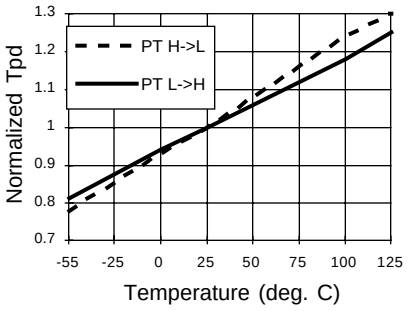
Delta Tpd vs # of Outputs Switching



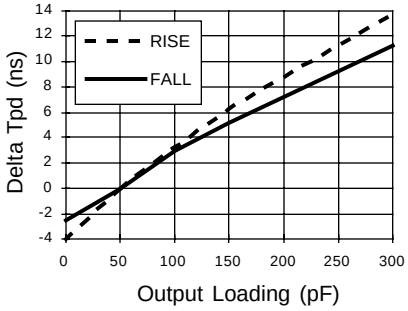
Input Clamp (Vik)



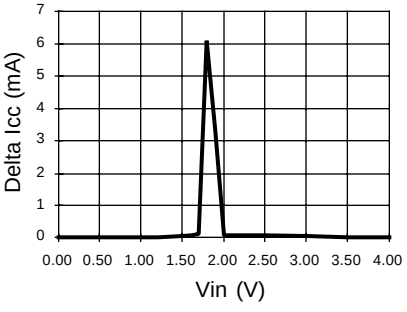
Normalized Tpd vs Temp



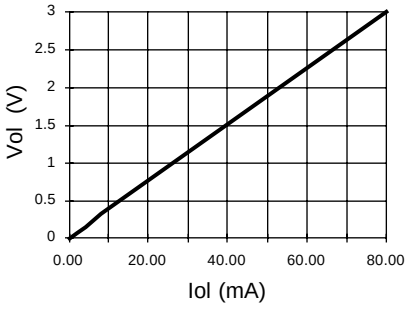
Delta Tpd vs Output Loading



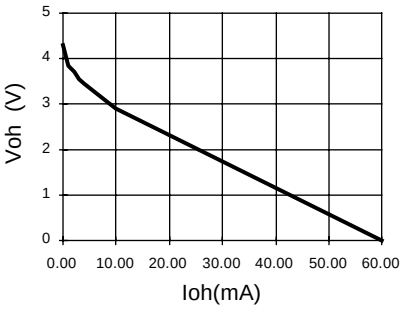
Delta Icc vs Vin (1 input)



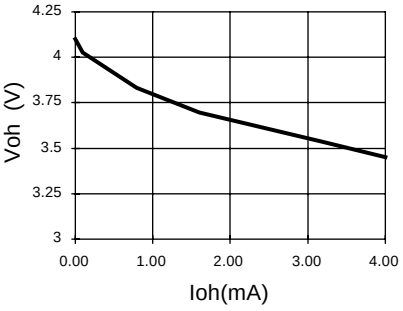
Vol vs Iol



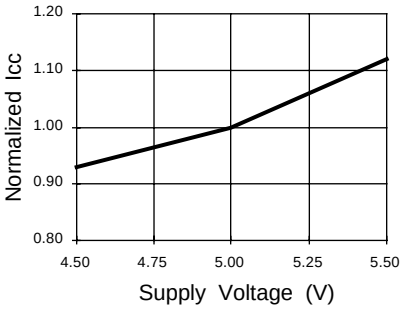
Voh vs Ioh



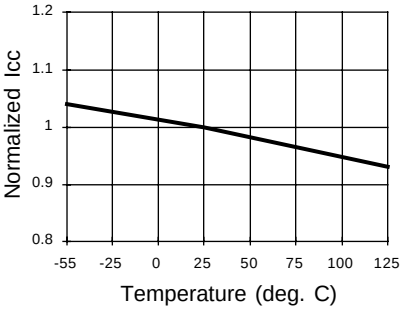
Voh vs Ioh



Normalized Icc vs Vcc



Normalized Icc vs Temp



Normalized Icc vs Freq.