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NEC
NEC Electronics Inc.

μPD72069
Floppy-Disk Controller

T-52-33-61

Description

The μPD72069 Floppy-Disk Controller (FDC) is one of NEC's integrated solutions for today's floppy-disk controller designs. An outgrowth of the μPD765A—long established as the industry standard for floppy-disk contol—the μPD72069 maintains complete microcode compatibility and contains the latest enhancements required for multitasking applications. Additionally, the μPD72069 integrates the standard host-interface registers used in IBM PC, PC/XT, PC/AT, and PS/2® designs.

The μPD72069 incorporates a high-performance analog PLL that requires no adjustments and supports all standard data rates as well as 600 kb/s and 1 Mb/s for the latest advances in tape and disk technology.

The μPD72069 has on-chip clock generation, selectable write precompensation, and all the circuitry necessary for interfacing directly to four floppy-disk drives.

Features

- 100% μPD765A/765B software and hardware compatible
- IBM and ECMA (Sony) formats
- Analog PLL (no adjustment required)
- Data transfer rate: 1 Mb/s; 600, 500, 300, 250, 150 kb/s
- Two system clock generators
- Write precompensation (programmable shift values)
- Programmable stepping speed
- Direct control of four FDDs
  - — Spindle motor control
  - — Unit select control
  - — High-current driver outputs (open drain)
- Three selectable modes support:
  - — PC, PC/XT, PC/AT registers
  - — Internal operating mode selection
  - — External operating mode selection

Ordering Information

Part Number	Package
μPD72069GF-3BA	100-pin plastic miniflat
μPD72069L	84-pin PLCC (plastic leaded chip carrier)

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Pin Identification

Symbol	I/O	Signal Function
A0	In	Address 0. Selects a register in μPD72069.
ACTL	In	Active Level. Sets active level of drive interface signal. ACTL — Active Level 0 — High 1 — Low
CGP1, CGP2	Out	Charge Pump. Phase difference of sub PLL devices.
$\overline{CS}$	In	Chip Select. Validates $\overline{RD}$ and $\overline{WR}$ signals.
D_0-D_7	I/O	Data Bus. Bidirectional, three-state data bus.
DEN0, DEN1 (*)	Out	Density. Specifies the density of a drive that can support more than one density. The output is a value corresponding to the selected data transmision rate. DEN0: When DR1 = 0 and DR0 = 1, the DEN0 output is 1. Otherwise it is 0. DEN1: When DR1 = 1 and DR0 = 1, the DEN1 output is 0. Otherwise it is 1. The values specified above are applicable when ACTL = 1. The values are reversed when ACTL = 0.
DIR (*)	Out	Direction. Specifies the seek direction. ACTL — DIR — Direction 0 — 0 — Outward 0 — 1 — Inward 1 — 0 — Inward 1 — 1 — Outward
DMAAK	In	DMA Acknowledge. Enables DMA cycle.
DMARQ	Out	DMA Request. Requests data transfer in DMA mode.
DR0-DR2	In	Data Rate. Sets data transfer rate in external mode.
DS0-DS3 (*)	Out	Drive Select. Selects up to four FDDs.
EM0-EM4 (*)	Out	Enable Motor. Controls FDD spindle motor on/off; also can be used as a general-purpose output port.
ENIDX (*)	In	Enable Index. Validates INDEX and RDATA signals from FDD.
ENPCS (*)	In	Enable Precompensation. This pin is usually connected to the LCT pin
$\overline{ENRW}$	In	Enable Read Write. Validate $\overline{RD}$ and $\overline{WR}$ signals when MSEL = 1. When MSEL = 0, this signal is meaningless.
FLT (*)	In	Fault. Indicates FDD is faulty.
FLTR (*)	Out	Fault Reset. Releases FDD from fault state.

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Pin Identification (cont)

Symbol	I/O	Signal Function
FMT	In	Format. Selects format in external mode. FMT: 0 = IBM; 1 = ECMA/ISO
HDLD (*)	Out	Head Load. Sets drive head in the load state.
INDEX (*)	In	Indicates drive head is positioned at physical start point of track on the medium.
INT	Out	Interrupt Request. Requests main system to process transferred data and execution results.
LCT (*)	Out	Low Current. Indicates drive head has selected a cylinder on or after the 43rd.
LPF1, LPF2	Out	Lowpass Filter. Phase difference of main PLL devices.
MSEL	In	Mode Select. Validates IBM-PC register and on-chip peripheral circuit.
PCS0, PCS1	In	Precompensation. Sets precompensation value in external or register mode.
$\overline{RD}$	In	Read. This control signal causes the main system to read data from the μPD72069 to the data bus.
RDATA (*)	In	Read data (consists of clock and data bits) from FDD.
READY (*)	In	Indicates FDD is ready.
RESET	In	Sets μPD72069 to idle state. FDD interface outputs except for WDATA (undefined) are: ACTL: 0 = All low; 1 = All high For the main system, INT and DMARQ are set to low and D_0-D_7 are set for input.
RSEL	In	Register Select. When MSEL = 1, used with $\overline{CS}$ and A0 to select register for IBM-PC (digital out register or control register). Invalid when MSEL = 0
SIDE (*)	Out	Side Select. Selects double-sided drive head. ACTL: 0, 0, 1, 1 / SIDE: 0, 1, 0, 1 / Drive Head: Head 0, Head 1, Head 1, Head 0
STEP (*)	Out	Generates seek pulses.
TC	In	Terminal Count. Terminates data transfer.
TRK0 (*)	In	Indicates drive head is positioned at cylinder 0.
WDATA (*)	Out	Write data (clock and data bits) to FDD.
WE (*)	Out	Requests FDD to write data.
WPRT (*)	In	Indicates medium is write-protected.
$\overline{WR}$	In	Write. Control signal that allows the main system to write data bus data into μPD72069.

Pin Identification (cont)

Symbol	I/O	Signal Function
XA1, XA2	In	Crystal A. For internal oscillator frequency control, a crystal resonator is connected to XA1 and XA2. For external clock input at XA1, XA2 is open. Frequency = 16 MHz
XB1, XB2	In	Crystal B. For internal oscillator frequency control, a crystal resonator is connected to XB1 and XB2. For external clock input at XB1, XB2 is open. Frequency = 19.2 MHz
2SIDE (*)	In	Indicates a medium with two usable sides has been loaded into the FDD.
IC	—	Internal Connection. Connect to GND1
NC	—	No Connection.
GND1	—	Ground for digital devices.
GND2	—	Ground for analog devices.
GND3	—	Ground for buffers.
V_{DD1}	In	+5-volt power supply for digital devices.
V_{DD2}	In	+5-volt power supply for analog devices.

(*) Active high when ACTL = 0; active low when ACTL = 1.

Output Pin Reset Status

Pin	Reset Status
D_0-D_7	Input
DMARQ, INT	Low
CGP1, CGP2, LPF1, LPF2, WDATA	Undefined
DIR, DS0-DS3, EM0-EM3, FLTR, HDLD, LCT, SIDE, STEP, WE	Low when ACTL = 0; high when ACTL = 1.
DEN0, DEN1	Output depends on the preset data transfer rates. Value set when ACTL = 0 is inverted when ACTL = 1, and vice versa.

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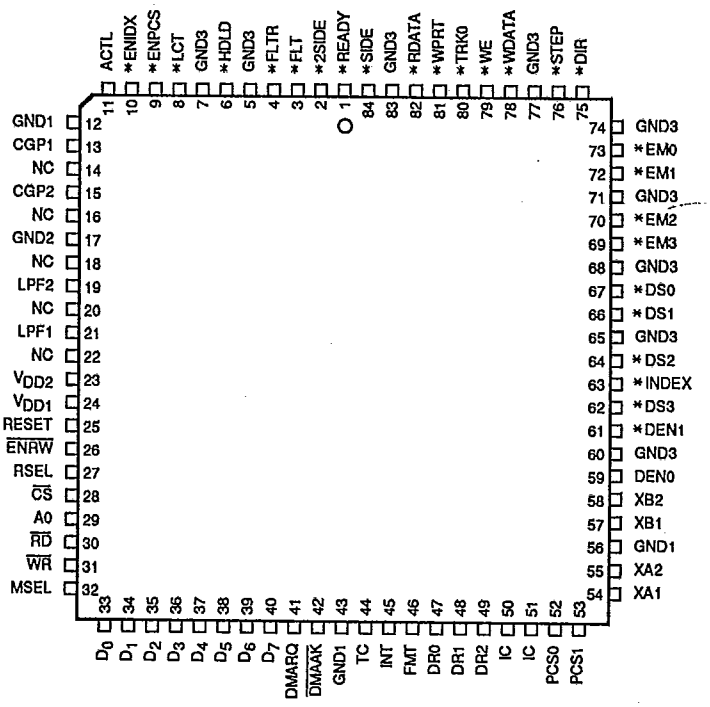
Pin Configurations

84-Pin PLCC



* Active level is variable

IC Connect to GND1

Connect GND1, GND2, and GND3 to main ground with the shortest possible wiring

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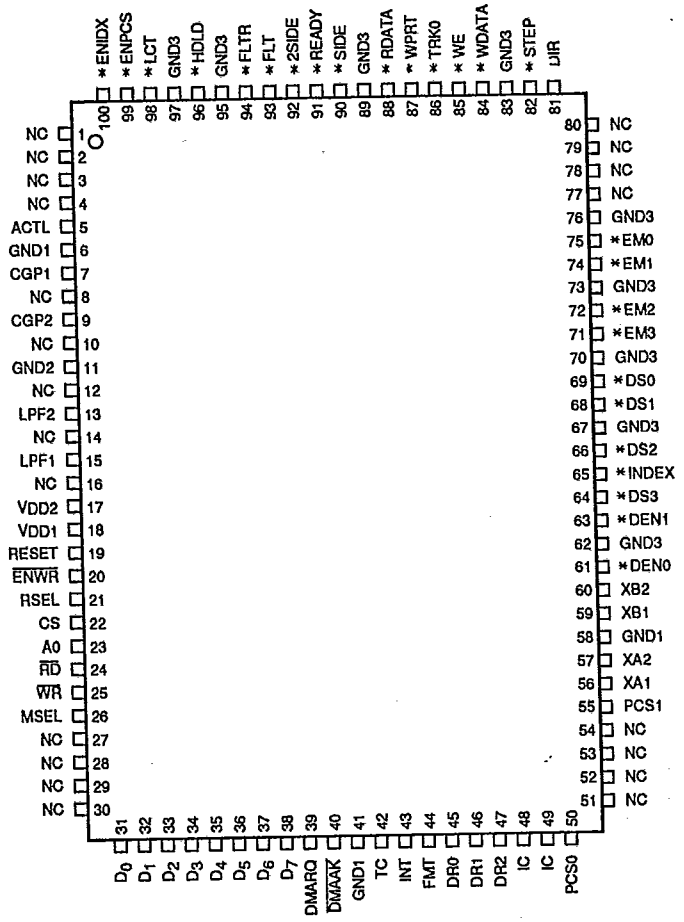
100-Pin Plastic Miniflat



* Active level is variable

IC Connect to GND1

Connect GND1, GND2, and GND3 to main ground with the shortest possible wiring

63vQ-5921B

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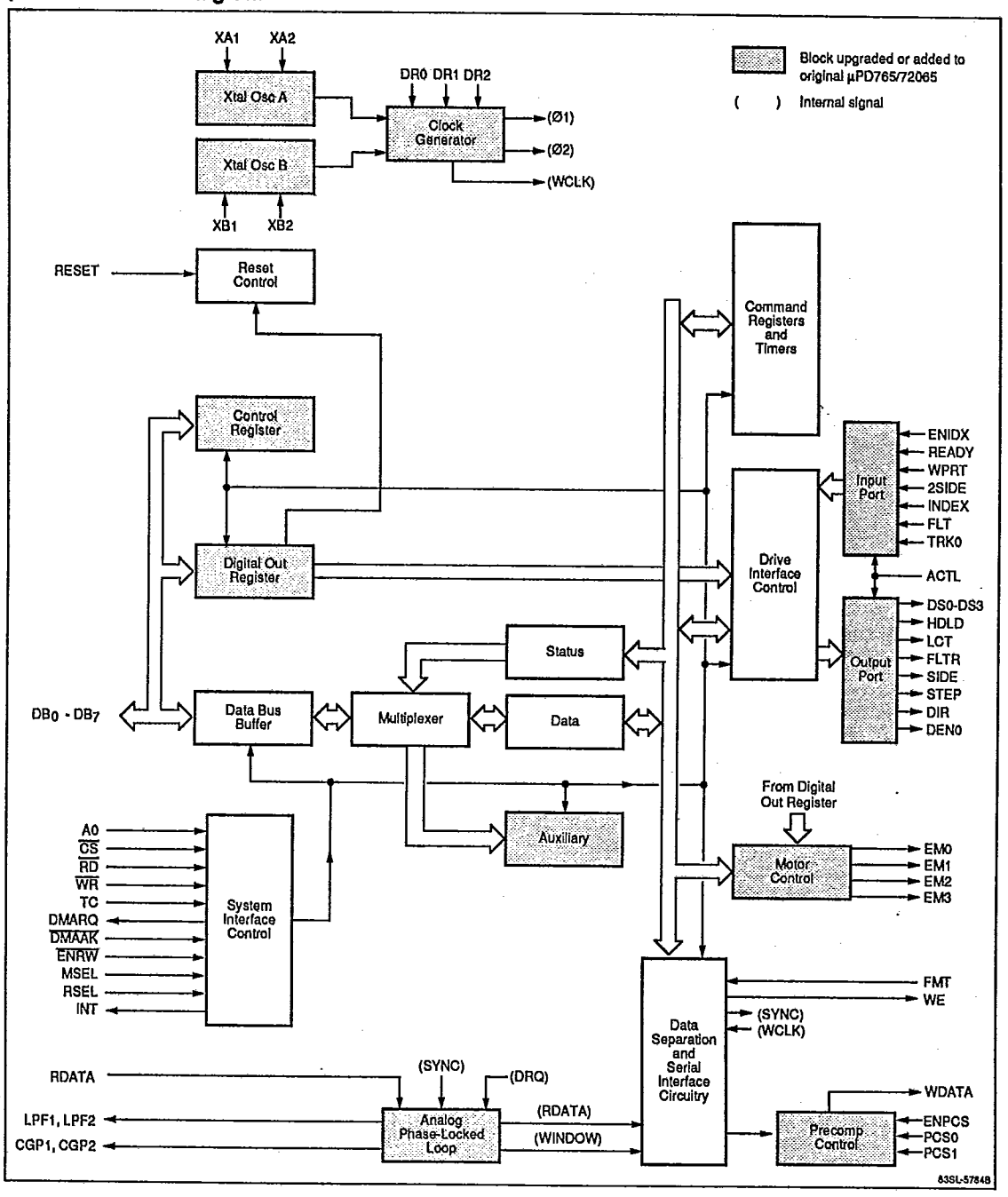
μPD72069 Block Diagram



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Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Voltage on any pin (except V_{DD})	−0.5 to +7 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to 150°C

Oscillator Specifications

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Low-level input voltage	V_{IL}	−0.5		0.2 V_{DD}	V	Pins XA1, XB1
High-level input voltage	V_{IH}	0.8 V_{DD}		V_{DD} + 0.5	V	
Clock cycle	ϕ_{CYA}	62.2	62.5	63.8	ns	Pins XA1, XA2
	ϕ_{CYB}	51.8	52.08	52.3	ns	Pins XB1, XB2
Clock width, high/low	ϕ_ℓ	0.35		0.65	ϕ_{CYA}, ϕ_{CYB}	
Clock rise time	ϕ_R			0.15	ϕ_{CYA}, ϕ_{CYB}	
Clock fall time	ϕ_F			0.15	ϕ_{CYA}, ϕ_{CYB}	

Analog PLL Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
VCO free-run frequency	f_T	9.9	10.0	10.1	MHz
f_T power supply voltage coefficient	f_{TUDD}	−0.1	0	+0.1	%/V
f_T temperature coefficient	f_{TTA}	−10	0	+10	ppm/°C
Capture range	f_{CTB}	±7.5			%
Lock range	f_{CTA}	±10			%
Capture range power supply voltage coefficient	f_{CTUD}	−5	0	+5	%/V
Capture range temperature coefficient	f_{CTTA}	−5	0	+5	ppm/°C
VCO jitter	t_{JIT}	0		2	ns
Peak shift margin	t_{PFTM}	80			%
Pull-in time	t_{PLIN}			20	bit

AC Characteristics 1; 1 Mb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;

MFM data transfer rate = 1 Mb/s; ϕ_{CYA} = 62.5 ns (16 MHz at XA1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	6.5			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	100			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	2			ϕ_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	62.5			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	125			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			6	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	32			ϕ_{CYA}	When external clock is input to XA1 pin.
Clock setup time at standby release	6	t_{CW}	16			ϕ_{CYA}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	16			ϕ_{CYA}	
INT response time from DMARQ ↓	7	t_{MI}	60		77	ϕ_{CYA}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			1	ϕ_{CYA}	

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AC Characteristics 1; 1 Mb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{RDATA}$ active-low time	8	t_{RDD}	40			ns	
$\overline{WDATA}$ active-low time	8	t_{WDD}		125		ns	
DS0-DS3 setup time to $\overline{DIR}$	9	t_{DSD}	9.5			μs	Note 2
DIR setup time to $\overline{STEP}$	9	t_{DST}	0.5			μs	
DS0-DS3 hold time after $\overline{STEP}$	9	t_{STU}	2.5			μs	
$\overline{STEP}$ active-low time	9	t_{STP}	3	3.5	4	μs	
DS0-DS3 hold time after $\overline{DIR}$ (Note 1)	9	t_{DDS}	22.5			μs	
DIR hold time after $\overline{STEP}$	9	t_{STD}	12			μs	
$\overline{STEP}$ cycle time	9	t_{SC}	16.5			μs	
$\overline{FLTR}$ active-low time	10	t_{FR}	4		5	μs	
$\overline{INDEX}$ low time	10	t_{IDX}	4			ϕ_{CYA}	

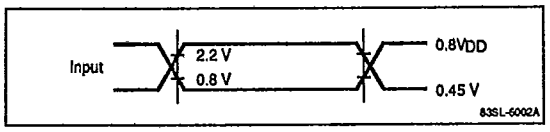
Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 9.5 μs is actually 9.450 μs.

(3) See figure 1 for timing measurement voltage thresholds.

Figure 1. Voltage Threshold for Timing Measurements



AC Characteristics 2; 500 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 500 kb/s; ϕ_{CYA} = 62.5 ns (16 MHz at XA1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	13			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	200			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	4			ϕ_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	125			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	250			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			12	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	64			ϕ_{CYA}	When external clock is input to XA1 pin.
Clock setup time at standby release	6	t_{CW}	32			ϕ_{CYA}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	32			ϕ_{CYA}	
INT response time from DMARQ ↓	7	t_{MI}	120		154	ϕ_{CYA}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			2	ϕ_{CYA}	

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AC Characteristics 2; 500 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ active-low time	8	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ active-low time	8	t_{WDD}		250		ns	
DS0-DS3 setup time to $\overline{\text{DIR}}$	9	t_{DSD}	19			μs	Note 2
DIR setup time to $\overline{\text{STEP}}$	9	t_{DST}	1			μs	
DS0-DS3 hold time after $\overline{\text{STEP}}$	9	t_{STU}	5			μs	
$\overline{\text{STEP}}$ active-low time	9	t_{STP}	6	7	8	μs	
DS0-DS3 hold time after $\overline{\text{DIR}}$ (Note 1)	9	t_{DDS}	45			μs	
DIR hold time after $\overline{\text{STEP}}$	9	t_{STD}	24			μs	
$\overline{\text{STEP}}$ cycle time	9	t_{SC}	33			μs	
$\overline{\text{FLTR}}$ active-low time	10	t_{FR}	8		10	μs	
$\overline{\text{INDEX}}$ low time	10	t_{IDX}	8			ϕ_{CYA}	

Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 19 μs is actually 18.950 μs.

(3) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 3; 250 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 250 kb/s; ϕ_{CYA} = 62.5 ns (16 MHz at XA1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	26			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	400			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	8			ϕ_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	250			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	500			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			6	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	128			ϕ_{CYA}	When external clock is input to XA1 pin.
Clock setup time at standby release	6	t_{CW}	64			ϕ_{CYA}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	64			ϕ_{CYA}	
INT response time from DMARQ ↓	7	t_{MI}	240		308	ϕ_{CYA}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			4	ϕ_{CYA}	

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AC Characteristics 3; 250 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ active-low time	8	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ active-low time	8	t_{WDD}		500		ns	
DS0-DS3 setup time to $\overline{\text{DIR}}$	9	t_{DSD}	38			μs	Note 2
DIR setup time to $\overline{\text{STEP}}$	9	t_{DST}	2			μs	
DS0-DS3 hold time after $\overline{\text{STEP}}$	9	t_{STU}	10			μs	
$\overline{\text{STEP}}$ active-low time	9	t_{STP}	12	14	16	μs	
DS0-DS3 hold time after $\overline{\text{DIR}}$ (Note 1)	9	t_{DDS}	90			μs	
DIR hold time after $\overline{\text{STEP}}$	9	t_{STD}	48			μs	
$\overline{\text{STEP}}$ cycle time	9	t_{SC}	66			μs	
$\overline{\text{FLTR}}$ active-low time	10	t_{FR}	16		20	μs	
$\overline{\text{INDEX}}$ low time	10	t_{IDX}	16			ϕ_{CYA}	

Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 38 μs is actually 37.950 μs.

(3) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 4; 600 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;

MFM data transfer rate = 600 kb/s; ϕ_{CYA} = 62.5 ns, ϕ_{CYB} = 52.08 ns (19.2 MHz at XB1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	10.8			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	166.7			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	4			ϕ_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	104.2			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	208.3			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			10	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	64			ϕ_{CYB}	When external clock is input to XB1 pin.
Clock setup time at standby release	6	t_{CW}	32			ϕ_{CYB}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	32			ϕ_{CYB}	
INT response time from DMARQ ↓	7	t_{MI}	120		154	ϕ_{CYB}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			2	ϕ_{CYB}	

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AC Characteristics 4; 600 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ active-low time	8	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ active-low time	8	t_{WDD}		208.3		ns	
DS0-DS3 setup time to $\overline{\text{DIR}}$	9	t_{DSD}	9.5			μs	Note 2
DIR setup time to $\overline{\text{STEP}}$	9	t_{DST}	0.5			μs	
DS0-DS3 hold time after $\overline{\text{STEP}}$	9	t_{STU}	2.5			μs	
$\overline{\text{STEP}}$ active-low time	9	t_{STP}	3	3.5	4	μs	
DS0-DS3 hold time after $\overline{\text{DIR}}$ (Note 1)	9	t_{DDS}	12			μs	
DIR hold time after $\overline{\text{STEP}}$	9	t_{STD}	22.5			μs	
$\overline{\text{STEP}}$ cycle time	9	t_{SC}	16.5			μs	
$\overline{\text{FLTR}}$ active-low time	10	t_{FR}	4		5	μs	
$\overline{\text{INDEX}}$ low time	10	t_{IDX}	8			ϕ_{CYB}	

Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 9.5 μs is actually 9,450 μs.

(3) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 5; 300 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;

MFM data transfer rate = 300 kb/s; ϕ_{CYA} = 62.5 ns, ϕ_{CYB} = 52.08 ns (19.2 MHz at XB1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	21.7			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	333.3			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	8			ϕ_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	208.3			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	416.7			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			20	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	128			ϕ_{CYB}	When external clock is input to XB1 pin.
Clock setup time at standby release	6	t_{CW}	64			ϕ_{CYB}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	64			ϕ_{CYB}	
INT response time from DMARQ ↓	7	t_{MI}	240		308	ϕ_{CYB}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			4	ϕ_{CYB}	

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AC Characteristics 5; 300 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ active-low time	8	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ active-low time	8	t_{WDD}		416.7		ns	
DS0-DS3 setup time to $\overline{\text{DIR}}$	9	t_{DSD}	19			μs	Note 2
DIR setup time to $\overline{\text{STEP}}$	9	t_{DST}	1			μs	
DS0-DS3 hold time after $\overline{\text{STEP}}$	9	t_{STU}	5			μs	
$\overline{\text{STEP}}$ active-low time	9	t_{STP}	6	7	8	μs	
DS0-DS3 hold time after $\overline{\text{DIR}}$ (Note 1)	9	t_{DDS}	24			μs	
DIR hold time after $\overline{\text{STEP}}$	9	t_{STD}	45			μs	
$\overline{\text{STEP}}$ cycle time	9	t_{SC}	33			μs	
$\overline{\text{FLTR}}$ active-low time	10	t_{FR}	8		10	μs	
$\overline{\text{INDEX}}$ low time	10	t_{IDX}	16			ϕ_{CYB}	

Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 19 μs is actually 18.950 μs.

(3) See figure 1 for timing measurement voltage thresholds.

Figure 2. Read Operation

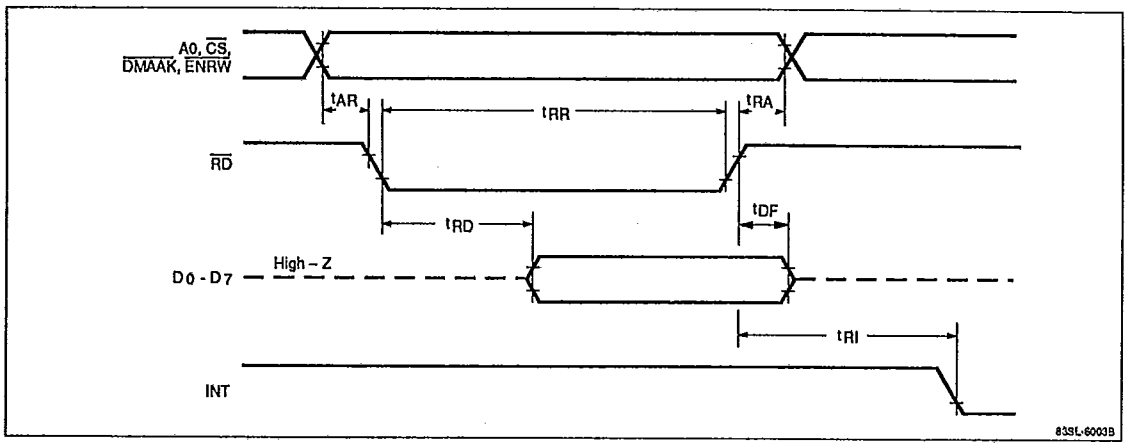

Figure 3. Write Operation

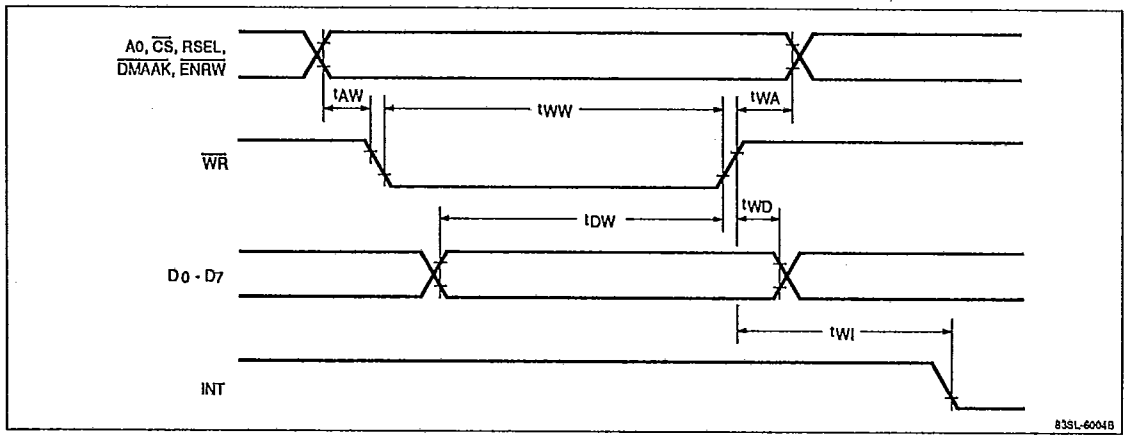

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Figure 4. DMA Operation

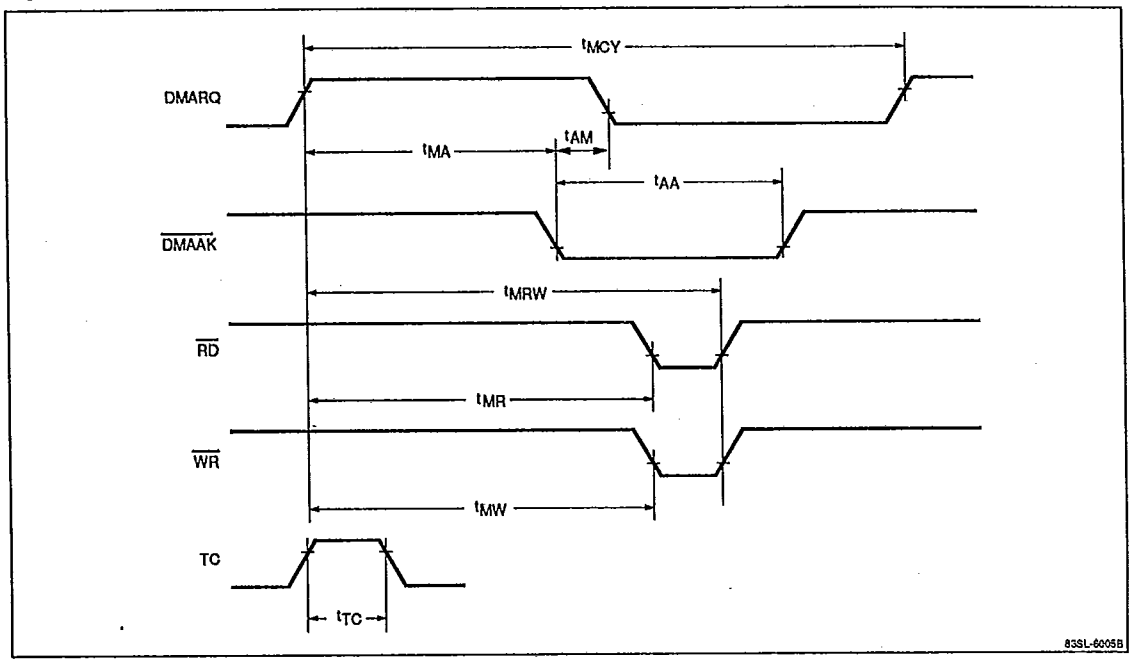


Figure 5. Reset Operattion

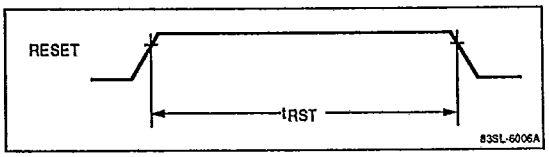
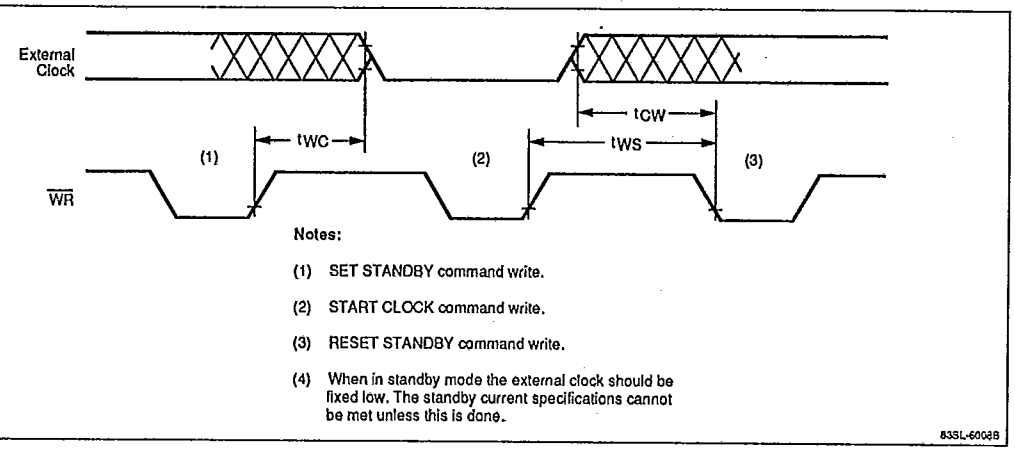


Figure. 6 Standby Operation



Notes:

(1) SET STANDBY command write.

(2) START CLOCK command write.

(3) RESET STANDBY command write.

(4) When in standby mode the external clock should be fixed low. The standby current specifications cannot be met unless this is done.

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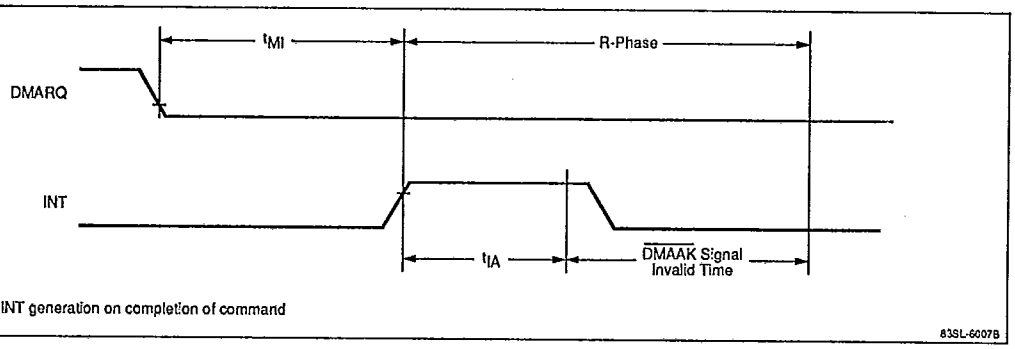
Figure 7. Overrun Operation



INT generation on completion of command

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Figure 8. RDATA and WDATA Waveforms

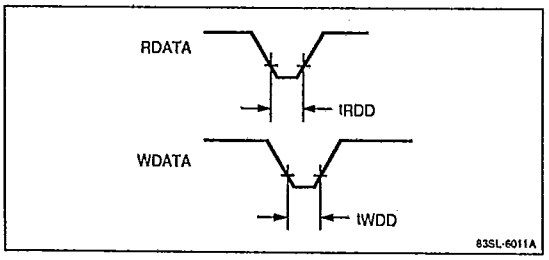

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Figure 9. Seek Operation

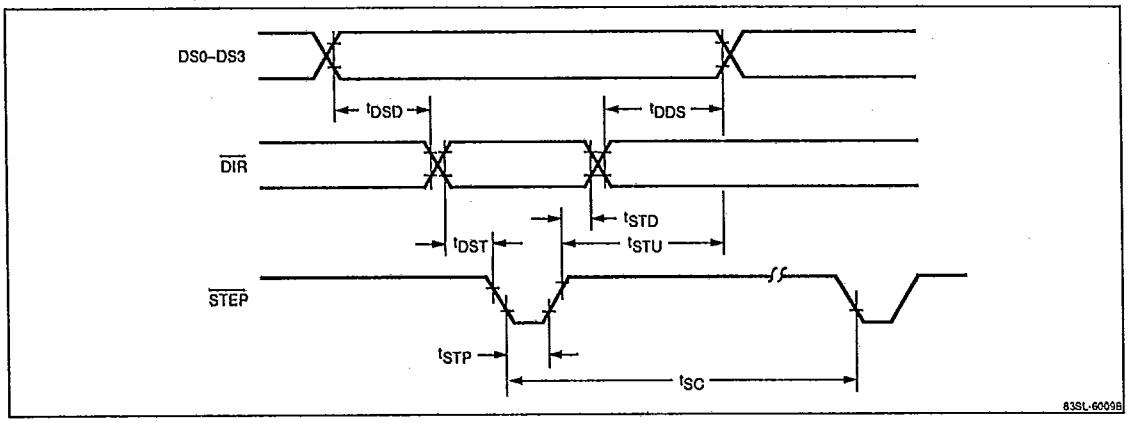
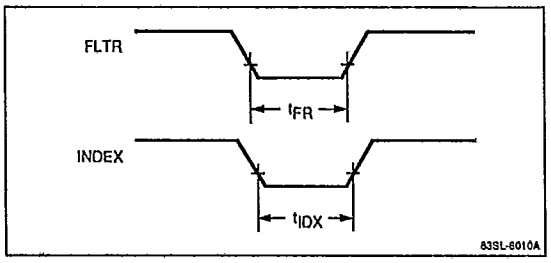


Figure 10. FLTR and INDEX Waveforms



μPD72067/68/69

Table 1 compares features of μPD72067, μPD72068, and μPDPD72069

Operation Modes

Table 2 describes the external, internal, and register modes of the μPD72069

Commands

Table 3 describes the 15 commands and 10 subcommands of the μPD72069.

Table 1. Feature Comparison, μPD72067/68/69

		μPD72067	μPD72068	μPD72069
FDD side external circuits built-in	Data sampling VFO	Digital PLL	Digital PLL	Analog PLL
	Write compensation	✓	✓	✓
	Motor control	✓	✓	✓
	Decoder	—	✓	✓
	Driver	—	✓	✓
Correspondence to high-speed data transmission		500 kb/s	500 kb/s	1.0 Mb/s
* CPU side external circuits built-in		—	✓	✓

* Circuits corresponding to IBM-PC (Address, DMARQ, and INT)

Table 2. Operation Modes

Mode	Function	Remarks
External	Sets the following parameters at the corresponding pins. • Data transmission speed • Write compensation value • Format (IBM/ECMA) • Motor control	Part of the programs of μPD765, 7265, 72065, and 72066 should be modified
Internal	Sets the following parameters using the corresponding commands (software). • Data transmission speed • Write compensation value • Format (IBM/ECMA) • Motor control	Part of the programs of μPD765, 7265, 72065, and 72066 should be modified.

Table 2. Operation Modes (cont)

Mode	Function	Remarks
Register	Corresponds to IBM-PC.	A dedicated CPU side interface is built-in An FDD select (DS0-DS3) stop function is built-in.

Table 3. Commands and Subcommands

Command Name	Function
Read Commands	
READ DATA	Specifies a sector and transfers its data to the host.
READ DELETED DATA	
READ ID	Reads a sector ID.
READ DIAGNOSTIC	Checks the track format.
SCAN EQUAL	Compares each sector data with host data and detects a sector that satisfies the set condition.
SCAN LOW OR EQUAL	
SCAN HIGH OR EQUAL	
Write Commands	
WRITE DATA	Specifies a sector and transfers its data to the host.
WRITE DELETED DATA	
WRITE ID	Writes the format of a track.
Seek Commands	
RECALIBRATE	Moves the read/write head to the outermost track (track 0).
SEEK	Moves the read/write head to the specified cylinder.
Sense Commands	
SENSE INTERRUPT STATUS	Reads the interrupt factor (seek end/state change) in the μPD72069.
SENSE DEVICE STATUS	Reads the FDD status.
Initialize Command	
SPECIFY	Defines a μPD72069 operation mode.
Subcommands	
SET STANDBY	Drives the μPD72069 in the standby status.
RESET STANDBY	Releases the μPD72069 from the standby status.
SOFTWARE RESET	Initializes the μPD72069.

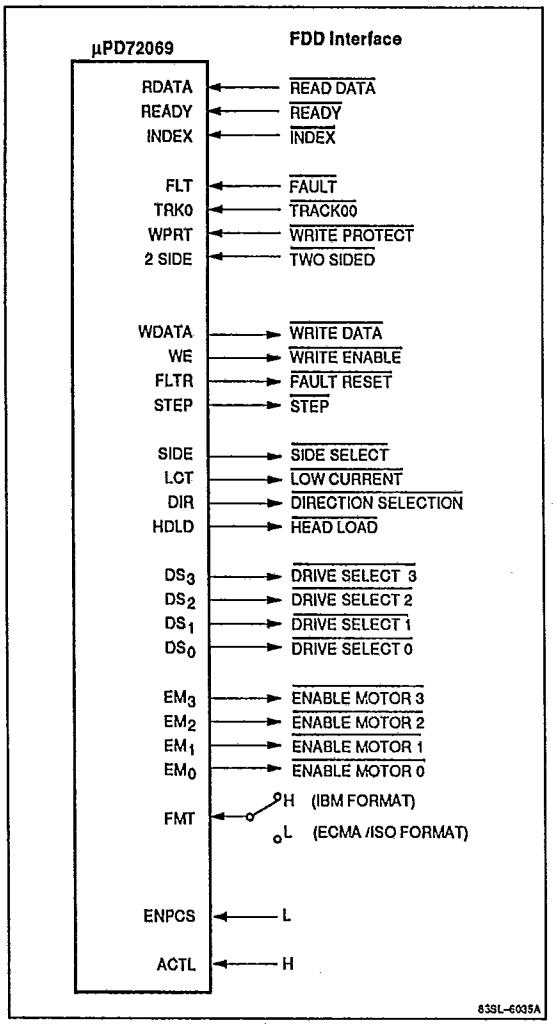
Table 3. Commands and Subcommands (cont)

Command Name	Function
ENABLE EXTERNAL MODE	Sets the μPD72069 in External Mode.
CONTROL INTERNAL MODE	Sets the μPD72069 in Internal Mode and sets both data transmission rate and precompensation value.
ENABLE MOTORS	Control On/Off of the spindle motor.
SELECT FORMAT	Selects either IBM or ECMA/ISO format.
START CLOCK	Starts the clock generator operation.
DATA TRANSFER RATE	Sets a data transmission rate.
PRECOMPENSATION	Sets a precompensation value.

Interface With FDD

Figure 11 is a reference circuit diagram of the direct connections between the μPD72069 and a floppy-disk drive.

Figure 11. μPD72069 to FDD Interface



System Bus

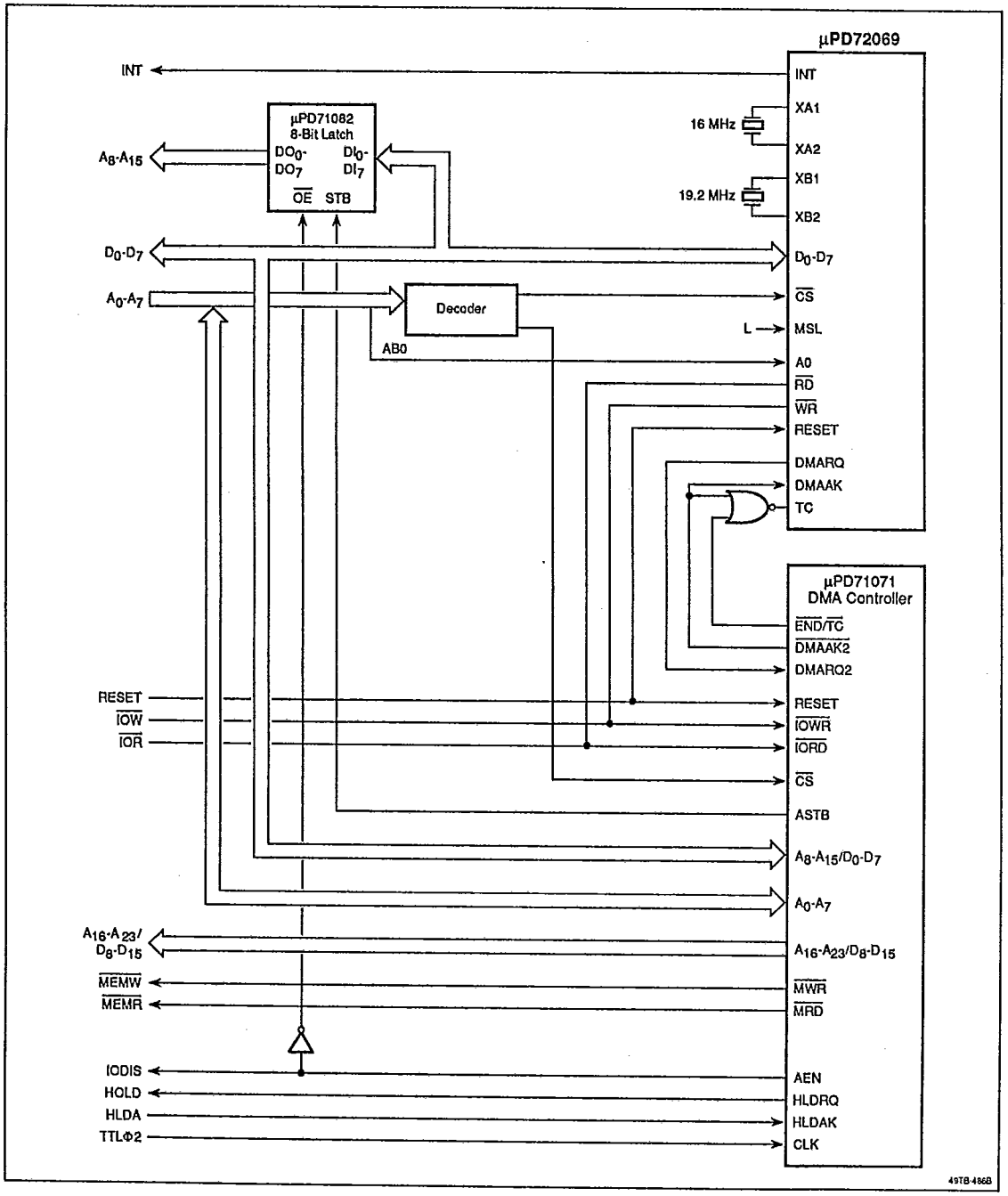
Table 4 lists the system clock XA or XB crystal appropriate for the selected floppy-disk drive

Figure 12 is a reference circuit diagram of the interface between the μPD72069 and a system bus for data transmission in Internal or External mode. To prevent misselection of I/O ports during DMA cycles, the Address Enable (AEN) output of μPD71071 inhibits other I/O ports.

Table 4. System Clock Frequencies

DR2-DR0	Mod Type	Data Rate (kb/s)	XA 16 MHZ	XB 19.2 MHz
000	FM	125	✓	—
	MFM	250	✓	—
001	FM	250	✓	—
	MFM	500	✓	—
010	FM	300	—	✓
	MFM	600	—	✓
011	FM	300	—	✓
	MFM	600	—	✓
100	FM	250	✓	—
	MFM	500	✓	—
101	FM	500	✓	—
	MFM	1 Mb/s	✓	—
110	FM	600	—	✓
111	FM	300	—	✓
	MFM	600	—	✓

Figure 12. μPD72069 to Host System Interface



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