NEC

DATA SHEET

MOS INTEGRATED CIRCUIT

μPD78CP14

8-BIT SINGLE-CHIP MICROCOMPUTER

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The μPD78CP14 is a product provided by replacing μPD78C14 internal mask ROM with PROM.

μPD78CP14DW/KB/R (for evaluation of μPD78C11A, 78C12A, 78C14) which is reprogrammable and μPD78CP14CW/G/GF/L of one time ROM version which is programmable only once (for small production) are provided.

Features:

- o Compatible with μPD78C11A, 78C12A, 78C14 (87AD series)
- o Internal PROM: 16384 words x 8 bits
  The internal PROM capacity can be changed conforming to the μPD78C11A, 78C12A, 78C14 by using software.

- o PROM programming characteristics: μPD27C256A compatible. ★

- o Single power supply: 5 V ±10 % (one-time PROM product) ★
  5 V ±5 % (EPROM product)

- o Compatible with QTOP™ microcomputer ★

Remarks The QTOP Microcomputer is the general term for "One-time single-chip microcomputer with on-chip PROM totally supported from program writing to seating, screening, and verification" offered by NEC.

Ordering Information

Part number	Package	Program memory
μPD78CP14CW	64-pin plastic shrink DIP (750 mil)	One-time PROM
μPD78CP14G-36	64-pin plastic QUIP	One-time PROM
μPD78CP14GF-3BE	64-pin plastic flat-pack (14 x 20 mm)	One-time PROM
μPD78CP14L	68-pin plastic QFJ (950 mil)	One-time PROM
μPD78CP14DW	64-pin ceramic shrink DIP with a window (750 mil)	EPROM
μPD78CP14KB	64-pin ceramic WQFN	EPROM
μPD78CP14R	64-pin ceramic QUIP with a window	EPROM

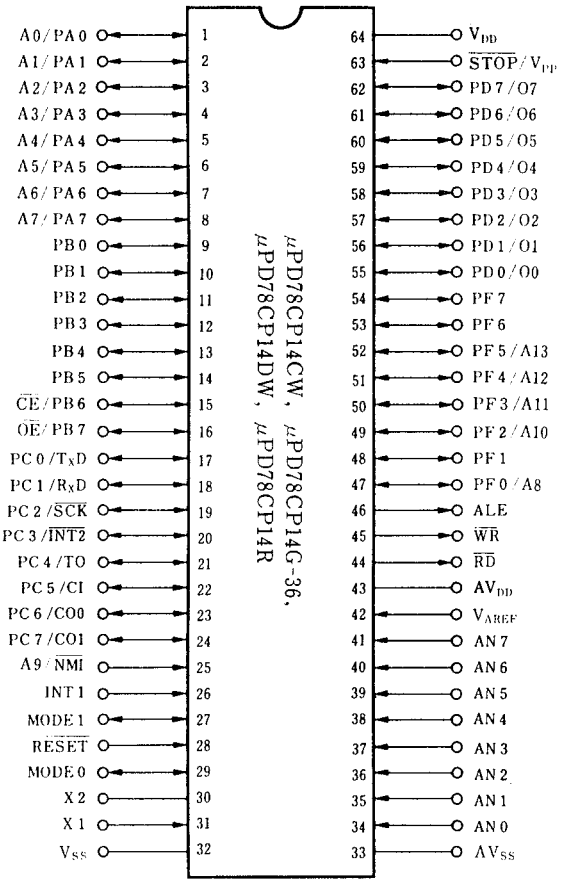
Quality grade

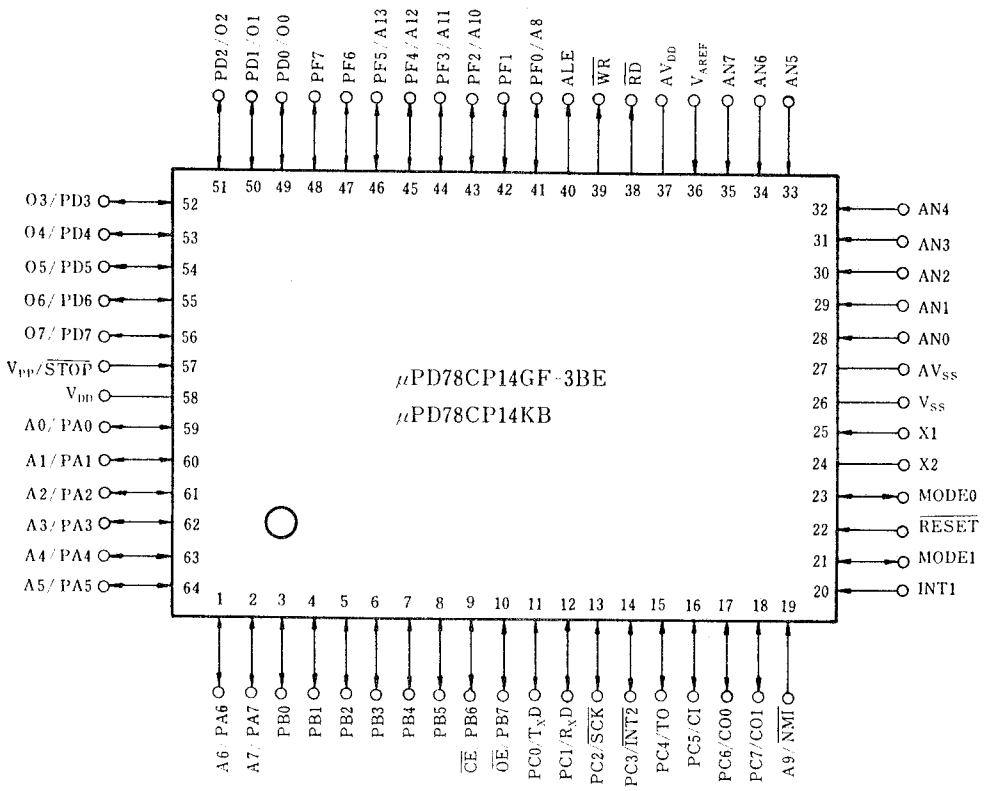
Standard

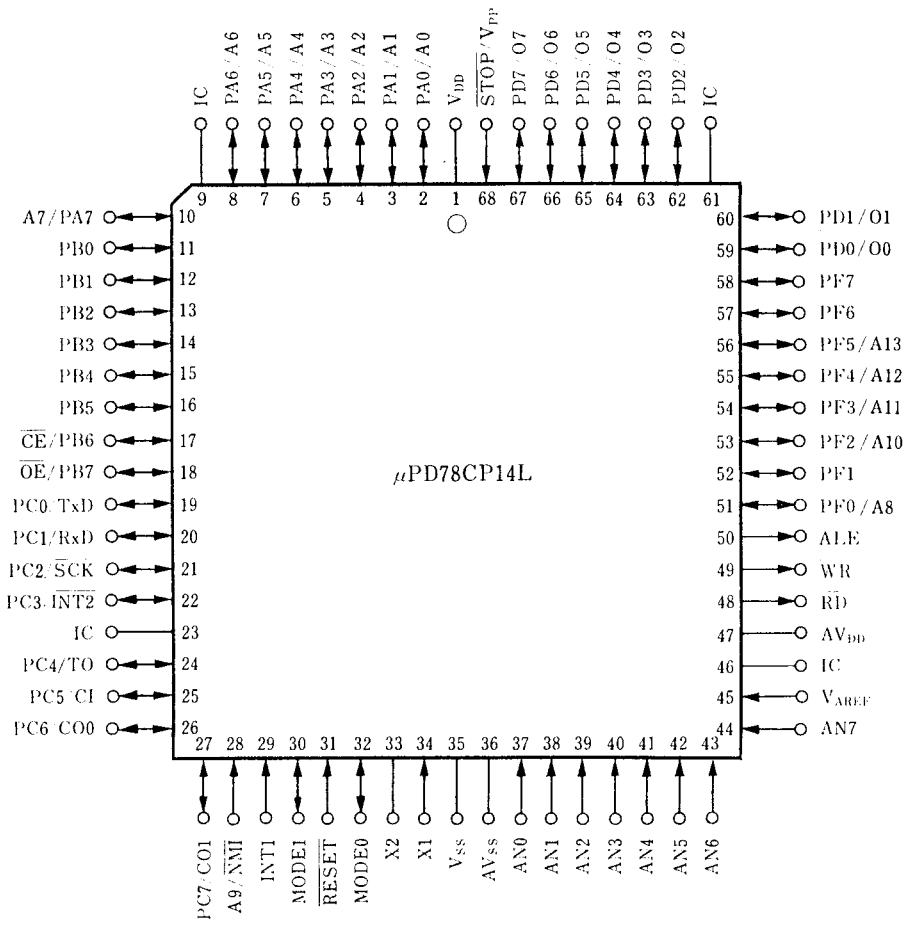
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

This document represents the portion common to the one-time PROM and EPROM products as PROM.

Pin Configuration (Top View)

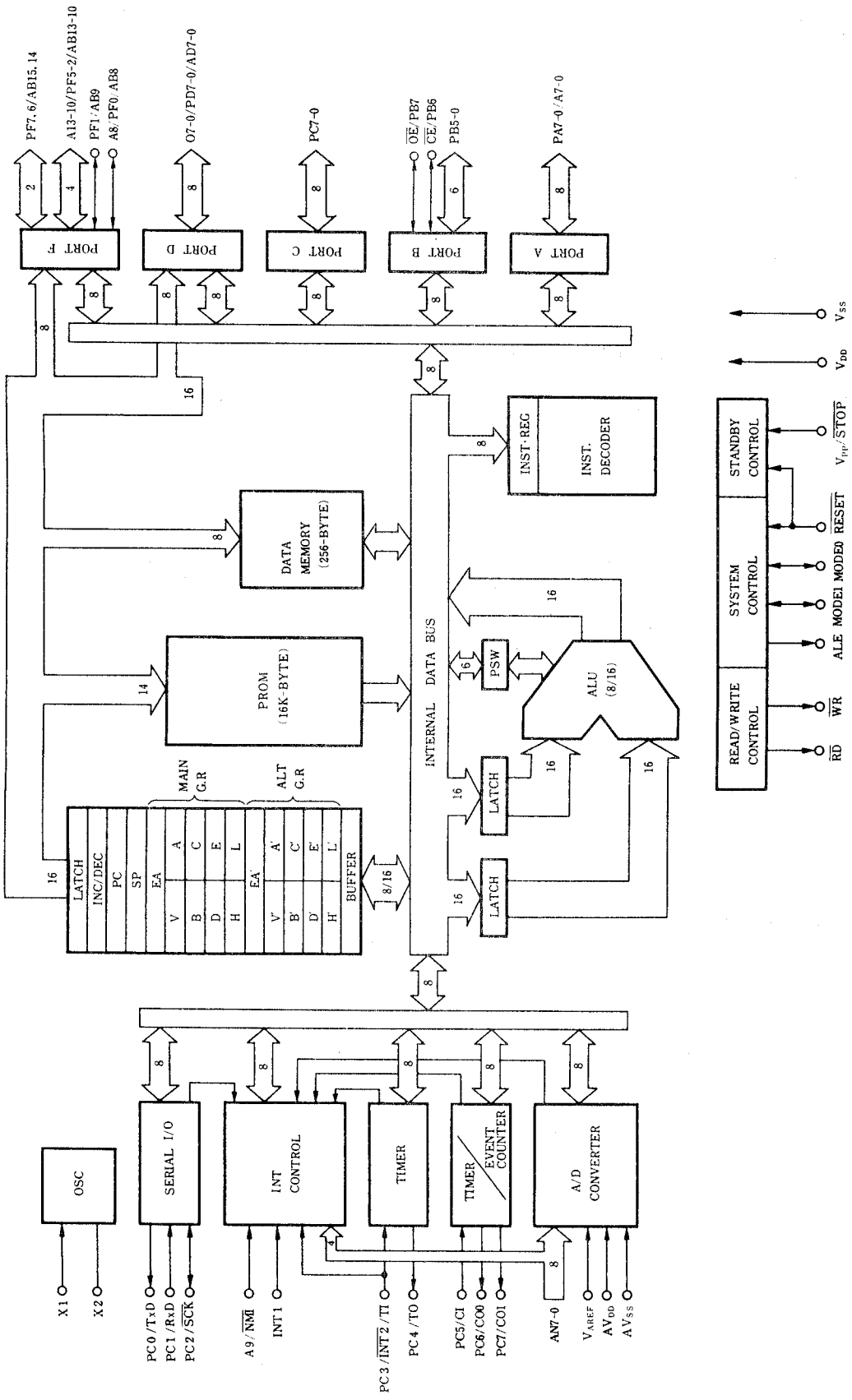



μPD78CP14GF-3BE
μPD78CP14KB
51 PD2/O2
50 PD1/O1
49 PD0/O0
48 PF7
47 PF6
46 PF5/A13
45 PF4/A12
44 PF3/A11
43 PF2/A10
42 PF1
41 PF0/A8
40 ALE
39 WR
38 RD
37 AVDD
36 VAREF
35 AN7
34 AN6
33 AN5
52 O3/PD3
53 O4/PD4
54 O5/PD5
55 O6/PD6
56 O7/PD7
57 VPP/STOP
58 VDD
59 A0/PA0
60 A1/PA1
61 A2/PA2
62 A3/PA3
63 A4/PA4
64 A5/PA5
32 AN4
31 AN3
30 AN2
29 AN1
28 AN0
27 AVSS
26 VSS
25 X1
24 X2
23 MODE0
22 RESET
21 MODE1
20 INT1
1 A6/PA6
2 A7/PA7
3 PB0
4 PB1
5 PB2
6 PB3
7 PB4
8 PB5
9 CE/PB6
10 OE/PB7
11 PC0/TXD
12 PC1/RXD
13 PC2/SCK
14 PC3/INT2
15 PC4/TO
16 PC5/CI
17 PC6/CO0
18 PC7/CO1
19 A9/NMI



IC ……Internally Connected

Block Diagram



Contents

1. PIN FUNCTIONS

1.1 Port Functions

Pin name	I/O	Function
PA7-0 (Port A)	I/O	8-bit input/output port. Input or output can be specified for each bit.
PB7-0 (Port B)		
PC7-0 (Port C)		
PD7-0 (Port D)		8-bit input/output port. Input or output can be specified for each byte.
PF7-0 (Port F)		8-bit input/output port. Input or output can be specified for each bit.

Remarks In these port pins, there are dual function pins described in **1.2 (at normal operation)** and **1.3 (at PROM writing/verify/reading)**

1.2 Functions Other Than Ports (During Normal Operation)

Pin name	I/O	Other uses	Function
TxD (Transmit data)	O	PC0	Serial data output pin.
RxD (Receive data)	I	PC1	Serial data input pin.
$\overline{SCK}$ (serial clock)	I/O	PC2	Serial clock input/output pin. When the internal clock is used, this line functions as an output and when an external clock source is used, this line functions as an input.
$\overline{INT2}$ (Interrupt request)	I	PC3	Maskable interrupt input (rising-edge triggered.)
TI (Timer input)	I		Timer external clock input pin.
Zero-cross	I		Zero cross detection pin of AC input.
TO (Timer output)	O	PC4	Square wave with pulse width of one internal clock cycle for timer count reference used as a half-cycle output.
CI (Counter input)	I	PC5	External pulse input pin to timer/event counter.
CO0, 1 (Counter output 0, 1	O	PC6,7	Programmable square wave output according to timer/event counter.
AD7-0 (Address/data bus 7-0)	I/O	PD7-0	These lines are used as a multiplexed address/data bus with external memory.
AB15-8 (Address bus 15-8	O	PF7-0	These lines are used as an address bus with external memory.
$\overline{WR}$ (Write strobe)	O		Store signal output for external memory write operation. This signal is HIGH except during external memory data write cycles. When the $\overline{RESET}$ signal is LOW or the hardware STOP mode is engaged, this line is placed in a high-impedance state.

Pin name	I/O	Other uses	Function
$\overline{RD}$ (Read strobe)	O		Strobe signal output for external memory read operation. This signal is HIGH except during external memory read cycles. When the $\overline{RESET}$ signal is LOW or the hardware STOP mode is engaged, this line is placed in a high-impedance state.
ALE (Address latch enable)	O		This line is used for the strobe signal to externally latch the lower-order address on the PD7-PD0 lines for external memory access. When the $\overline{RESET}$ signal is LOW or the hardware STOP mode is engaged, this line is placed in a high-impedance state.
MODE0 MODE1 (Mode)	I/O I/O		Set the MODE0 pin to 0 (low level) and the MODE1 pin to 1 (high level) (Note 1.)
$\overline{NMI}$ (Non-maskable interrupt)	I		Nonmaskable interrupt input (falling-edge triggered).
INT1 (Interrupt request)	I		Maskable interrupt input (rising-edge triggered.)This line can also be used for AC input zero cross detection.
AN7-0 (Analog input)	I		8-line analog input to A/D converter. Lines AN7-AN4 provide edge falling-edge detection input.
V_{AREF} (Reference voltage)	I		For use as both A/D converter reference voltage and A/D converter operation control.
AV_{DD} (Analog V_{DD})			Power supply line for A/D converter.
AV_{SS} (Analog V_{SS})			GND potential for A/D converter.
X1, X2 (Crystal)			Crystal-oscillator input for system clock timing. When an external clock source is used, the timing pulses are input on X1. The X1 inversion signal is input to X2.

Note Pull up. Pull-up resistance R is $4 \leq R \leq 0.4\ t_{CYC}$ [kΩ] (t_{CYC}: ns units)

Pin name	I/O	Other uses	Function
$\overline{\text{RESET}}$ (Reset)	I		System reset (active-low) input. Input line for hardware STOP mode control signal. When a low level is input, oscillation stops.
$\overline{\text{STOP}}$ (Stop)	I		Input line for hardware STOP mode control signal. When a low level is input, oscillation stops.
V_{DD}			+5 V power supply line.
V_{SS}			GND potential line.

1.3 Functions Other Than Ports (During PROM Write, Verify, Read)

Pin name	I/O	Other uses	Function
A7-0	I	PA7-0	Low-order eight-bit input pins of address.
$\overline{\text{CE}}$	I	PB6	Chip enable signal input pin.
$\overline{\text{OE}}$	I	PB7	Output enable signal input pin.
O7-0	I/O	PD7-0	Data input/output pins.
A13-10 A8	I	PF5-2 PF0	High-order 6-bit input pins address.
A9	I	$\overline{\text{NMI}}$	
MODE0 MODE1	I		Set the MODE0 pin to 1 (high) and the MODE1 pin to 0 (low).
$\overline{\text{RESET}}$	I		Set the RESET pin to 0 (low).
V_{PP}		$\overline{\text{STOP}}$	High voltage apply pin. When EPROM is read, high level (1) is input.

★ **Caution Input low level for PF6 during PROM write, verify, read.**

1.4 Recommended Conditions for Unused Pin

Pin	Recommended connection
PA7-0 B7-0 C7-0 PD7-0 PF7-0	Connect to V_{DD} or V_{SS} via resistor.
$\overline{RD}$ $\overline{WR}$ ALE	Open
$\overline{STOP}$	Connect to V_{DD}
INT1, $\overline{NMI}$	Connect to V_{DD} or V_{SS}
AV_{DD}	Connect to V_{DD}
V_{AREF} AV_{SS}	Connect to V_{SS}
AN7-0	Connect to AV_{SS} or AV_{DD}

2. MEMORY CONFIGURATION

μPD78CP14 memory can be operated in any of the following three modes as specified:

- o μPD78C11A mode (see Figure 2-1)
- o μPD78C12A mode (see Figure 2-2)
- o μPD78C14 mode (see Figure 2-3)

In addition, the internal PROM address range can be specified to map external memory (except PROM) efficiently (See 3.2).

The vector area, call table area, and internal RAM are common to all the modes.

Internal RAM data can be retained with low consumption current by setting the hardware or software STOP mode or the HALT mode.

Figure 2-1. Memory Map (μPD78C11A Mode)

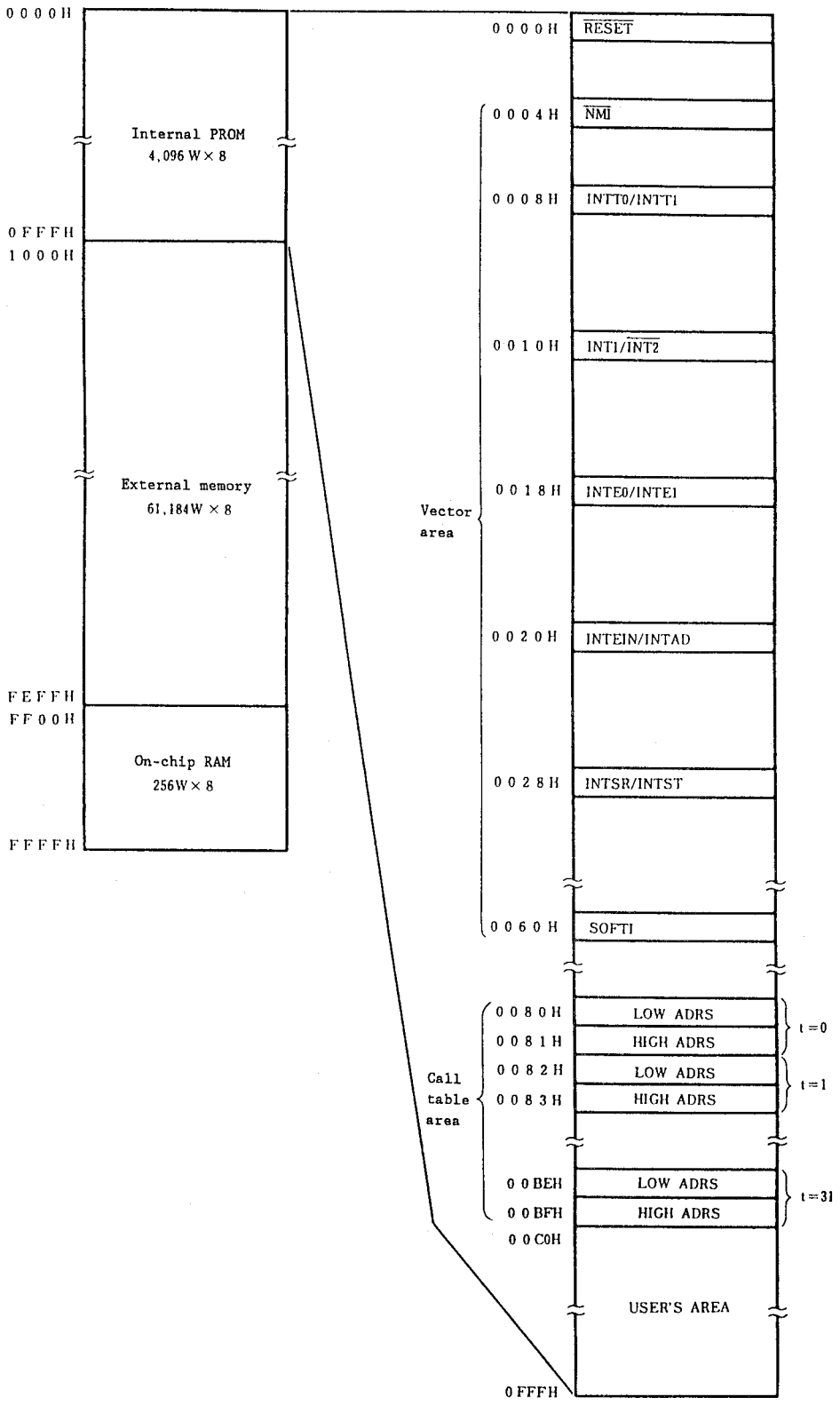


Figure 2-2. Memory Map (μPD78C12A Mode)

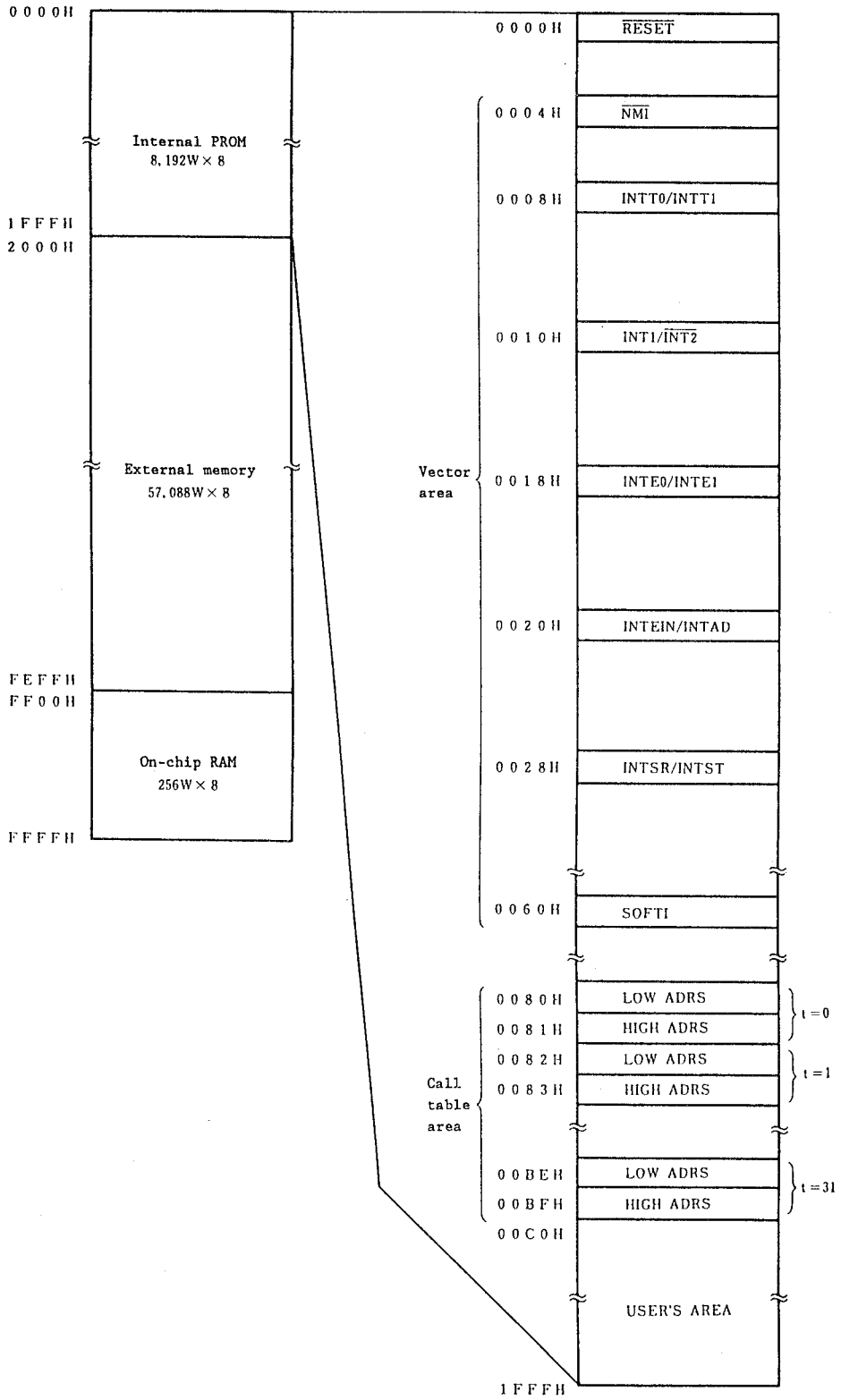
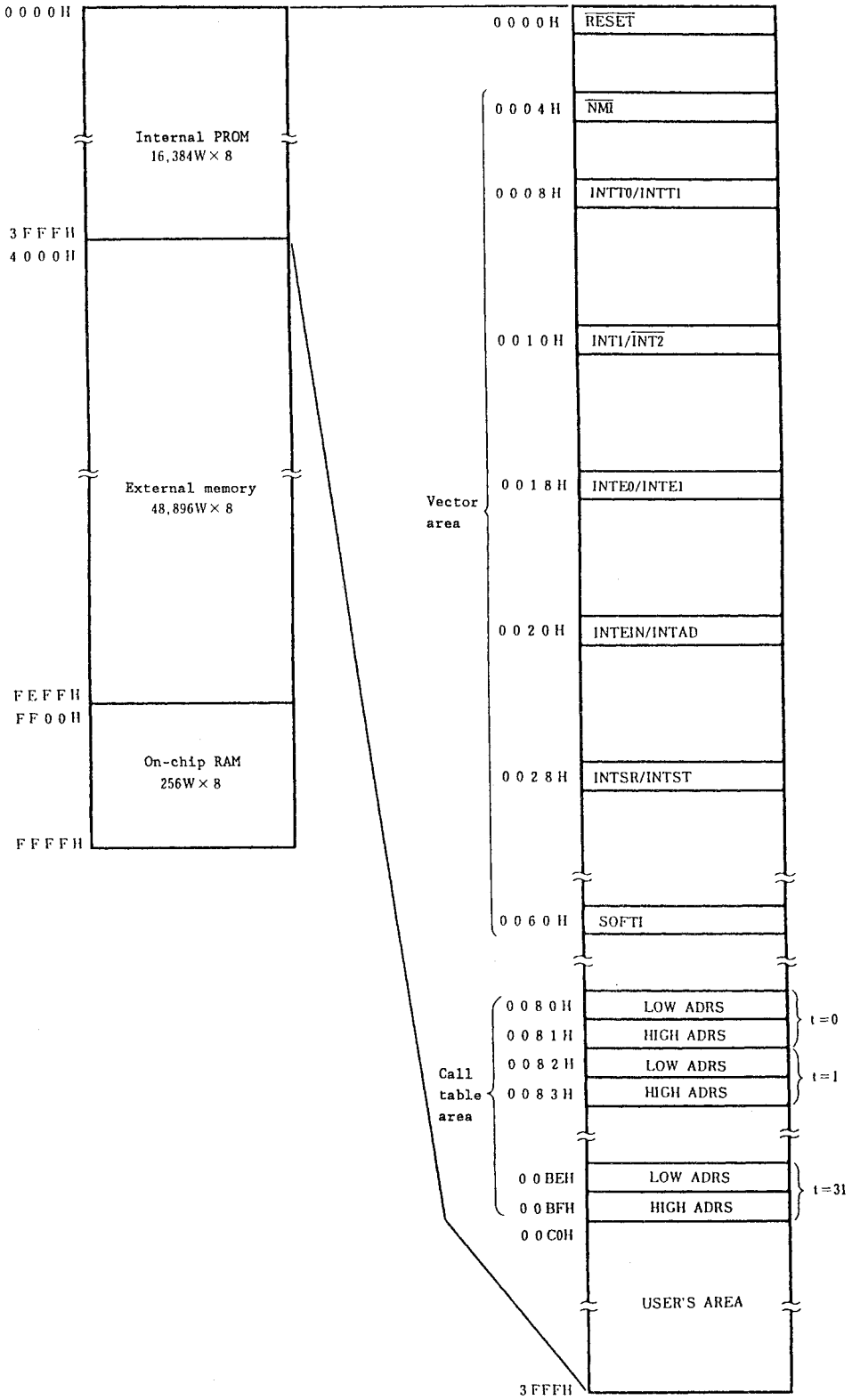


Figure 2-3. Memory Map (μPD78C14 Mode)



3. MEMORY EXTENSION

The μPD78CP14 enables external memory extension by using the MEMORY MAPPING register (MM) or the MODE0 and MODE1 pins. The internal PROM access range can be specified by using MEMORY MAPPING register bits 7 and 6.

3.1 MODE Pins

The μPD78CP14 enables the user to change the programming mode and normal operation mode by setting the MODE0 and MODE1 pins.

Table 3-1 lists mode setting by using the MODE pins.

Table 3-1 Mode Setting by Using MODE Pins

MODE1	MODE0	Operation mode
L	L	Setting prohibted
L	H	Programming mode (Note)
H	L	Normal operation mode
H	H	Setting prohibited

Note See 4.

To make the MODE0 and MODE1 pins high, use pull-up registor of $4 \leq R \leq 0.4\ t_{CYC}$[k ohms] ($t_{CYC}$: ns units).

3.2 MEMORY MAPPING Register (MM)

The MEMORY MAPPING register is an 8-bit register used for the following control:

- PD7-PD0, PF7-PF0 port/extension mode specification.
- Control as to whether or not internal RAM access is enabled.
- Internal PROM access range specification

Figure 3-1 shows the MEMORY MAPPING register format.

(1) MM0-MM2 bits

The MM0-MM2 bits are used to PD7-PD0 port/extension mode, input/output, PF7-PF0 address output specification.

As shown in Figure 3-1, the capacity of external memory that can be connected to the μPD78CP14 can be selected among the following four types:

- 256 bytes
- 4K bytes
- 16K bytes
- 48K, 56K, or 60K bytes (according to how MM6 and MM7 bits are set)

The PF7-PF0 port pins not used for address output can be used as general purpose port pins.

When $\overline{\text{RESET}}$ is input or the hardware STOP mode is entered, the bits are cleared and the PD7-PD0 pins are used as an input port (output high impedance).

(2) MM3 bit (RAE)

The MM3 bit is used to specify whether internal RAM access is enabled (RAE=1) or not (RAE=0).

When standby operation is performed or external RAM connected is used without using internal RAM, set the MM3 bit to "0".

Even if $\overline{\text{RESET}}$ is input during normal operation, the bit contents are held. However, the RAE bit becomes undefined at power on reset, thus the bit must be initialized by using an instruction.

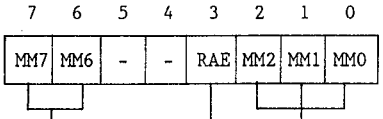
(3) MM6 and MM7 bits

The MM6 and MM7 bits are used to specify the internal PROM access range.

When $\overline{\text{STOP}}$ or $\overline{\text{RESET}}$ is input, the MM6 and MM7 bits are cleared and the 16K-byte mode (μPD78C14 mode) is selected.

The bits are effective only for the μPD78CP14 and 78CG14. When data is written into the bits on the μPD78C11A, 78C12A/14, or 78C14 the CPU ignores it. Therefore, the programs developed on the μPD78CP14 can be moved to mask ROM as they are.

Figure 3-1. MEMORY MAPPING Register Format



0	0	0	Port mode	Single chip	PD7-0 = input port PF7-0 = port mode
0	0	1			PD7-0 = output port PF7-0 = port mode
0	1	0	Extension mode	256 bytes	PD7-0 = extension mode PF7-0 = port mode
1	0	0		4K bytes	PD7-0, PF3-0 = extension mode PF7-4 = port mode
1	1	0		16K bytes	PD7-0, PF5-0 = extension mode PF7-6 = port mode
1	1	1		48K/56K/60K (Note) bytes	PD7-0, PF7-0 = extension mode

Note According to how the MM7 and MM6 bits are set.

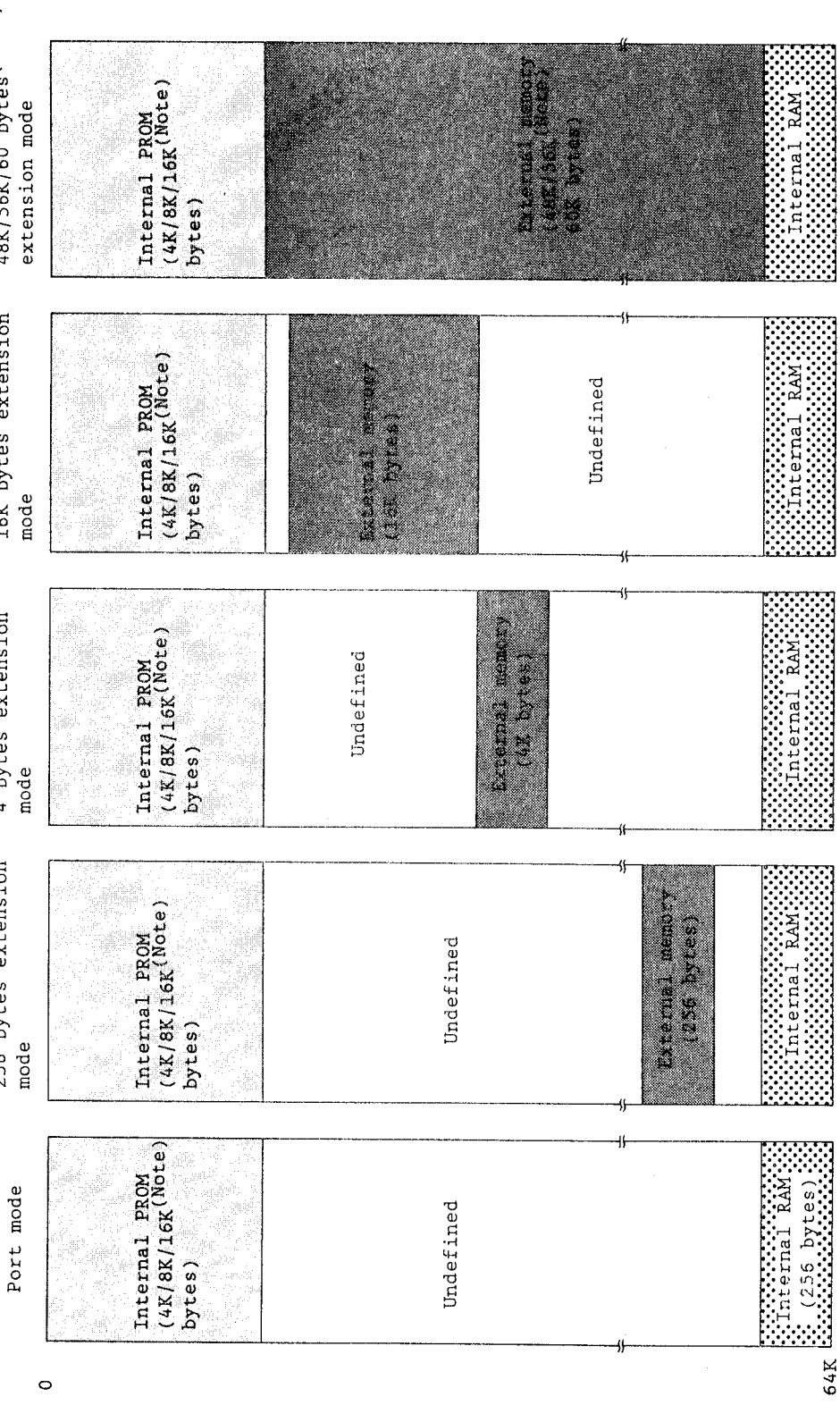
Internal RAM access

0	Disable
1	Enable

Internal PROM access

0	0	Access to the 0000H-3FFFH address area of internal PROM (μPD78C14 mode)
0	1	Access to the 0000H-1FFFH address area of internal PROM (μPD78C12A mode)
0	1	Access to the 0000H-0FFFH address area of internal PROM (μPD78C11A mode)
1	1	Setting prohibited

Figure 3-2. External Extension Mode Set by Using MEMORY MAPPING Register



Note The capacity can be selected among the three types by setting the MM6 and MM7 bits.

4. PROM PROGRAMMING

The μPD78CP14 contains 16384 x 8 bit PROM for internal program memory. Table 4-1 lists the pins used to write and verify the PROM.

The μPD78CP14 programming timing is compatible with the μPD27C256A programming timing.

Also refer to the μPD27C256A documents.

Table 4-1. Pin Functions in PROM Programming

Pin name	Function
$\overline{RESET}$	Low level input (during write/verify, read)
MODE0	High level input (during write/verify, read)
MODE1	Low level input (during write/verify, read)
PF6	Low level input (during write/verify, read)
V_{PP} Note	High voltage input (during write/verify), high level input (during read)
$\overline{CE}$ Note	Chip enable input
$\overline{OE}$ Note	Output enable input
A13-0 Note	Address input
O7-0 Note	Data input (during write, data output (during verify/read)
V_{DD} Note	Supply voltage input

Note These pins are compatible with the μPD27C256A pins.

Cautions 1. Cover the μPD78CP14 containing an erasion window with shading cover film except in EPROM erasion.

2. The μPD78CP14 of one time PROM product which does not contain an erasion window cannot be erased with ultraviolet rays.

3. The μPD78CP14 does not contain memory at 4000H-7FFFH.
   If read operation is performed, FFH is always read.

   To program in the μPD27C256A,

   (1) set PROM programmer 4000H-7FFFH buffer to all FFH; or

   (2) program the ROM 0000H-3FFFH area only.

4.1 PROM Programming Operation Mode

The PROM programming operation mode is set as listed in Table 4-2. At the time, treat every pin not used for programming as listed in Table 4-3.

Table 4-2. EPROM Programming Mode

Operation mode	(Note) $\overline{CE}$	(Note) $\overline{OE}$	(Note) V_{PP}	(Note) V_{DD}	$\overline{RESET}$	MODE0	MODE1	PF6
Program	L	H	+12.5 V	+6 V	L	H	L	L
Program verify	H	L						
Program inhibit	H	H						
Read	L	L	+5 V	+5 V				
Output disable	L	H						
Standby	H	L/H						

Note These pins are compatible with the μPD27C256A pins.

Caution When V_{PP} is set to +12.5 V and V_{DD} is set to +6 V, both $\overline{CE}$ and $\overline{OE}$ must not be set L simultaneously.

Table 4-3. Recommended Conditions for Unused Pins (in PROM programming mode)

Pin	Recommended connection method
INT1	Connect to V_{SS}
X1	
AN0-7	
VA_{REF}	
AV_{DD}	
AV_{SS}	
Pins except above	Connect each pin via a resistor to V_{SS}
X2	Open

4.2 PROM Write Procedure

Data is written into PROM according to the following procedure: (High speed write is enabled.)

(1) Pull down unused pins to V_{SS} via a resistor and supply +6 V to V_{DD} and +12.5 V to V_{PP}.

(2) Supply initial address.

(3) Supply write data.

(4) Supply 1 ms program pulse (active low) to the $\overline{CE}$ pin.

(5) Verify mode. If data is written, proceed to (7). If data is not written, repeat (3) to (5). If data cannot be written after the steps are repeated 25 times, proceed to (6).

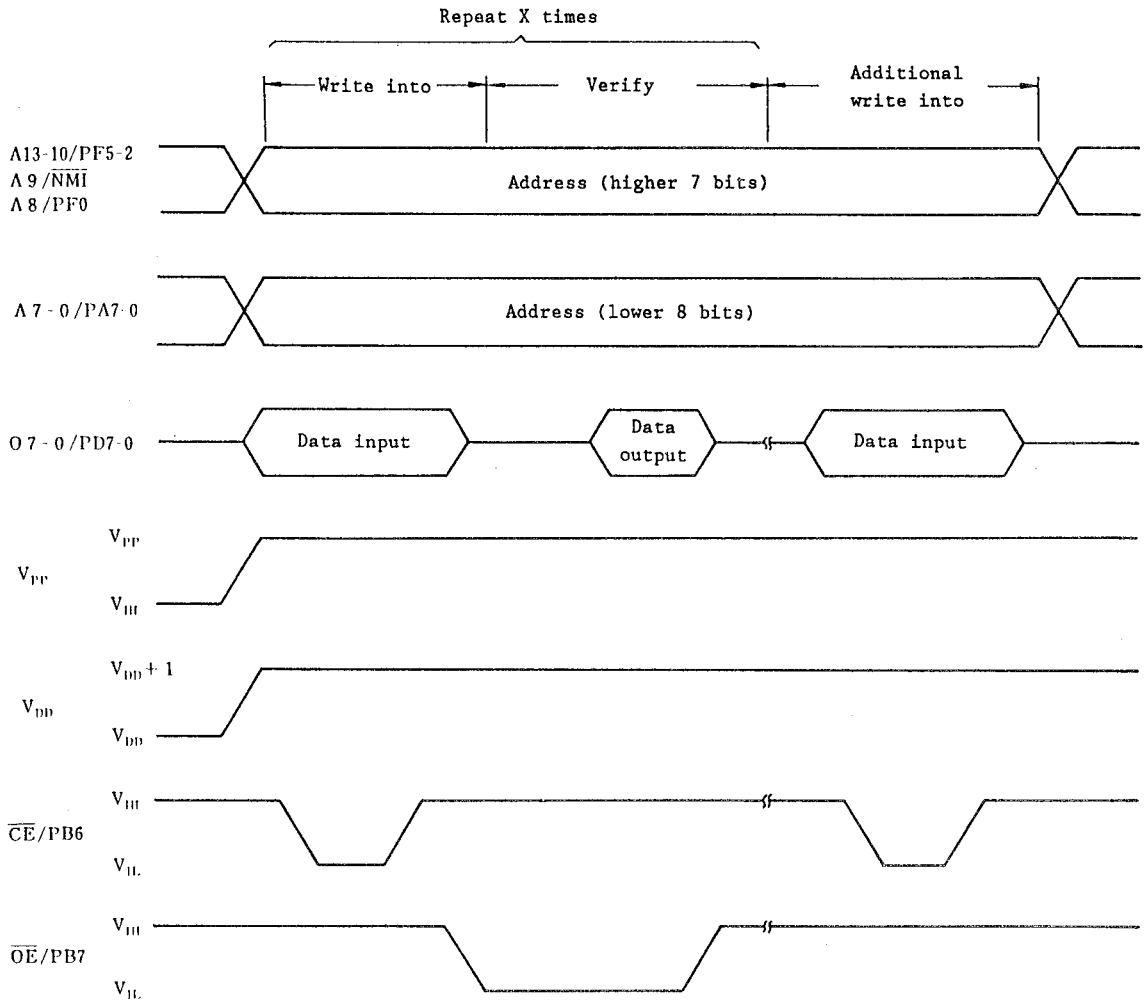
(6) Judge that the EPROM is a faulty device. Stop write operation.

(7) Supply write data. Supply X (number of (3)-(5) repetitions) x 3 ms program pulse (additional write).

(8) Increment the address.

(9) Repeat (3) to (8) until the last address is reached.

Figure 4-1. PROM Write/Verify Timing



4.3 PROM Read Procedure

The PROM contents can be read onto the external data bus (O7-O0) according to the following procedure:

(1) Pull down THE unused pins to GND via a resistor.

(2) Supply 5 V to the V_{DD} and V_{PP} pins.

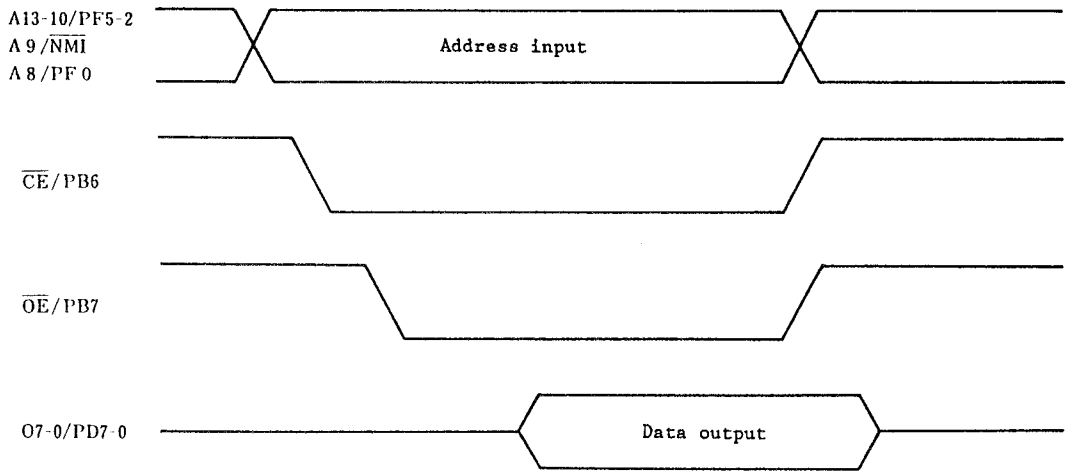
(3) Input the address of the data to be read to the A13-A0 pins.

(4) Read mode

(5) Output data to the O7-O0 pins.

Figure 4-2 shows the (2) to (5) timing.

Figure 4-2. PROM Read Timing



5. EPROM ERASE (ONLY PACKAGE PRODUCTS WITH CERAMIC WINDOW)

The μPD78CP14 enables the programmed EPROM data contents to be erased by light rays whose wavelength is shorter than about 400 nm. The programmed EPROM data contents may also be erased if the uncovered window is exposure to direct sunlight or a fluorescent light for several hours. Thus, to protect the data contents, cover the μPD78CP14 with an opaque film so as to prevent ultraviolet rays from entering it through the top window. Shading cover film whose quality is guaranteed is attached to the package product with a window containing EPROM by NEC for shipping.

For normal EPROM erase, place the μPD78CP14 under an ultraviolet light source (254 nm). The minimum amount of radiation exposure required to erase the μPD78CP14 completely is 15 $W.s/cm^2$ (ultraviolet ray strength x erase time). This corresponds to about 15 to 20 minutes when using a ultraviolet ray lamp of 12000 uW/cm^2. However, note that the erase time may be prolonged by aging of the ultraviolet lamp, dirty package window, etc. The distance between the ultraviolet lamp and the μPD78CP14 should be within 2.5 cm.

6. WINDOW SEAL (ONLY FOR PACKAGE PRODUCTS WITH CERAMIC WINDOW)

To prevent light other than EPROM erasion lamps from causing an error or light from causing the internal circuitry other than EPROM to malfunction, put a protective seal on the window except when the EPROM contents are erased.

7. ONE-TIME PROM PRODUCT SCREENING

The one-time PROM products (μPD78CP14CW, 78CP14G-36, 78CP14GF-3BE, and 78CP14L) cannot be completely tested by NEC prior to shipment because of the structures. For screening, it is recommended to verify PROM after storing the necessary data under a storage temperature of 125 and a storage time of 24 hours after writing the data.

NEC has a service of one-time PROM write to scaling to screening to verification for pay under the name of QTOP MICON. For details, ask the salesperson.

8. ELECTRICAL SPECIFICATIONS

The μPD78CP14 has a few differences as follows in electric between one-time PROM product and EPROM product. There is no different electric specifications other than the parameters listed in Table 8-1.

★ **Table 8-1. Differences in Electric Specifications between One-time PROM Product and EPROM Product**

Parameter \ Products	One-time PROM Product			EPROM product		
Operation power supply voltage range (V_{DD})	5 V ±10 %			5 V ±5 %		
Data retention current (I_{DDDR})	Conditions	TYP.	MAX.	Conditions	TYP.	MAX.
	V_{DDDR} = 2.5 V	1 μA	15 μA	V_{DDDR} = 2.5 V		300 μA
	V_{DDDR} = 5 V ± 10 %	10 μA	50 μA	V_{DDDR} = 5 V ± 5 %		1 mA

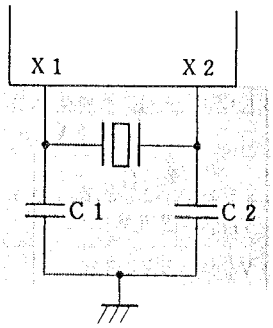
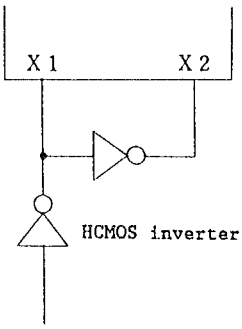
Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Test condition	Ratings	Unit
Power supply voltage	V_{DD}		-0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD}+0.5	V
	AV_{SS}		-0.5 to +0.5	V
	V_{PP}		-0.5 to +13.5	V
Input voltage	V_I	Except for $\overline{NMI}$/A9 pin	-0.5 to V_{DD}+0.5	V
		$\overline{NMI}$/A9 pin	-0.5 to +13.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Output low current	I_{OL}	All outputs	4.0	mA
		Total, all outputs	100	mA
Output high current	I_{OH}	All outputs	-2.0	mA
		Total, all outputs	-50	mA
A/D converter reference input voltage	V_{AREF}		-0.5 to AV_{DD}+0.3	V
Operation temperature	T_{opt}		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

★ Oscillator Characteristics

(One time PROM product): (Ta = -40°C to +85°C, V_{DD} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V, V_{DD} -0.8 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})

(EPROM product): Ta = -40 to +85°C, V_{DD} = +5.0 V ±5%, V_{SS} = AV_{SS} = 0 V, V_{DD} -0.8V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})

Resonator	Recommended circuit	Parameter	Test condition	MIN.	MAX.	Unit
Ceramic or crystal resonator		Oscillation frequency (f_{xx})		6	15	MHz
External clock		X1 input frequency (f_x)		6	15	MHz
		X1 input rise, fall time (t_r, t_f)		0	20	ns
		X1 input high, low level width ($t_{\phi H}$, $t_{\phi L}$)		20	167	ns

Caution 1. Put the oscillator close to the X1 and X2 pins as much as possible.

2. Do not pass any other signal line through the shaded region.

Capacitance (Ta = 25°C, $V_{DD} = V_{SS} = 0$ V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			10	pF
Output capacitance	C_O				20	pF
Input/output capacitance	C_{IO}				20	pF

DC Characteristics

(One time PROM product): (Ta = -40 to +85°C, $V_{DD} = AV_{DD}$ = +5.0 V ±10%, $V_{SS} = AV_{SS} = 0$ V) ★

(EPROM product) : (Ta = -40 to +85°C, $V_{DD} = AV_{DD}$ = +5.0 V ±5%, $V_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL1}	Except for $\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$ INT1, TI, or AN4-AN7	0		0.8	V
	V_{IL2}	$\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, or AN4-AN7	0		$0.2V_{DD}$	V
Input high voltage	V_{IH1}	Except for $\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$ INT1, TI, AN4-AN7, X1, or X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, AN4-AN7, X1, or X2	$0.8V_{DD}$		V_{DD}	V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output high voltage	V_{OH}	I_{OH} = -1.0 mA	V_{DD}-1.0			V
		I_{OH} = -100 μA	V_{DD}-0.5			V
Input current	I_I	INT1(Note 1), TI(PC3)(Note 2); 0 V ≤ V_I ≤ V_{DD}			±200	μA
Input leakage current	I_{LI}	Except for INT1, TI(PC3); 0 V ≤ V_I ≤ V_{DD}			±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}			±10	μA
AV_{DD} power supply current	AI_{DD1}	Operating mode f_{XX} = 15 MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

(to be continued)

(Cont'd)

Parameter	Symbol	Test condition			MIN.	TYP.	MAX.	Unit
V_{DD} power supply current	I_{DD1}	Operating mode f_{XX} = 15 MHz				16	32	mA
	I_{DD2}	HALT mode f_{XX} = 15 MHz				8	15	mA
Data retention voltage	V_{DDDR}	Hardware or software STOP mode			2.5			V
★ Data retention current ★	I_{DDDR}	Hardware/ Software STOP mode (Note 3)	One-time PROM product	V_{DDDR} = 2.5 V		1	15	μA
				V_{DDDR} = 5 V ± 10%		10	50	μA
			EPROM product	V_{DDDR} = 2.5 V			300	μA
				V_{DDDR} = 5 V ± 10%			1	mA

Note 1. Assume that self-bias is generated by setting the ZCM register.

2. Assume that self-bias is generated by setting the ZCM register when the control mode is set in the MCC register.

3. When self-bias is not generated.

AC Characteristics ★

(One-time PROM product: (Ta = -40°C to +85°C, $V_{DD} = AV_{DD}$ = +5.0 V ±10%, $V_{SS} = AV_{SS}$ = 0 V)

(EPROM product : (Ta = -40°C to +85°C, $V_{DD} = AV_{DD}$ = +5.0 V ±5%, $V_{SS} = AV_{SS}$ = 0 V)

Read/write Operation:

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
X1 input cycle time	t_{CYC}		66	167	ns
Address setup time to ALE ↓	t_{AL}	f_{XX}=15 MHz, CL=150 pF	30		ns
Address hold time from ALE ↓	t_{LA}		35		ns
Address → $\overline{RD}$ ↓ delay time	t_{AR}		100		ns
$\overline{RD}$ ↓ → address float time	t_{AFR}	C_L=150 pF		20	ns
Address → data input time	t_{AD}	f_{XX}=15 MHz, CL=150 pF		250	ns
ALE ↓ → data input time	t_{LDR}			135	ns
$\overline{RD}$ ↓ → data input time	t_{RD}			120	ns
ALE ↓ → $\overline{RD}$ ↓ delay time	t_{LR}		15		ns
Data hold time from $\overline{RD}$ ↑	t_{RDH}	CL=150 pF	0		ns
$\overline{RD}$ ↑ → ALE ↑ delay time	t_{RL}	f_{XX}=15 MHz, CL=150 pF	80		ns
$\overline{RD}$ low level width	t_{RR}	When data is read f_{XX}=15 MHz, CL=150 pF	215		ns
		When OP code is fetched f_{XX}=15 MHz, CL=150 pF	415		ns
ALE high level width	t_{LL}	f_{XX}=15 MHz, CL=150 pF	90		ns
Address → $\overline{WR}$ ↓ delay time	t_{AW}	f_{XX}=15 MHz, CL=150 pF	100		ns
ALE ↓ → data output time	t_{LDW}			180	ns
$\overline{WR}$ ↓ → data output time	t_{WD}	CL=150 pF		100	ns
ALE ↓ → $\overline{WR}$ ↓ delay time	t_{LW}	f_{XX}=15 MHz, CL=150 pF	15		ns
Data setup time to $\overline{WR}$ ↑	t_{DW}		165		ns
Data hold time from $\overline{WR}$ ↑	t_{WDH}		60		ns
$\overline{WR}$ ↑ → ALE ↑ delay time	t_{WL}		80		ns
$\overline{WR}$ low level width	t_{WW}		215		ns

Zero-cross Characteristics:

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Zero-cross detection input	V_{ZX}	AC coupling	1	1.8	VAC_{P-P}
Zero-cross accuracy	A_{ZX}	60-Hz sine wave		±135	mV
Zero-cross detection input frequency	f_{ZX}		0.05	1	kHz

Serial Operation:

Parameter	Symbol	Test condition		MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYK}	$\overline{SCK}$ input	(Note 1)	800		ns
		$\overline{SCK}$ input	(Note 2)	400		ns
		$\overline{SCK}$ output		1.6		μs
$\overline{SCK}$ low level width	t_{KKL}	$\overline{SCK}$ input	(Note 1)	335		ns
		$\overline{SCK}$ input	(Note 2)	160		ns
		$\overline{SCK}$ output		700		ns
$\overline{SCK}$ high level width	t_{KKH}	$\overline{SCK}$ input	(Note 1)	335		ns
		$\overline{SCK}$ input	(Note 2)	160		ns
		$\overline{SCK}$ output		700		ns
RxD setup time to $\overline{SCK}$ ↑	t_{RXK}	(Note 1)		80		ns
RxD hold time from $\overline{SCK}$ ↑	t_{KRX}	(Note 1)		80		ns
$\overline{SCK}$ ↓ → TxD delay time	t_{KTX}	(Note 1)			210	ns

Notes 1. When the clock rate is x1 in the asynchronous mode or the synchronous mode or I/O interface mode is set

2. When the clock rate is x16 or x64 in the asynchronous mode

★ **Remark** The numeric values in the table apply when f_{XX} = 15 MHz, C_L = 150pF.

Other Operations:

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
TI high, low level width	t_{TIH}, t_{TIL}		6		t_{CYC}
CI high, low level width	t_{CI1H}, t_{CI1L}	o Event count mode o Frequency measurement mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	o Pulse width measurement mode o ECNT latch, clear input o INTEIN set input	48		t_{CYC}
$\overline{NMI}$ high, low level width	t_{NIH}, t_{NIL}		10		us
INT1 high, low level width	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ high, low level width	t_{I2H}, t_{I2L}		36		t_{CYC}
AN4-7 high, low level width	t_{ANH}, t_{ANL}		36		t_{CYC}
$\overline{RESET}$ high, low level width	t_{RSH}, t_{RSL}		10		us

★ A/D Converter Characteristics

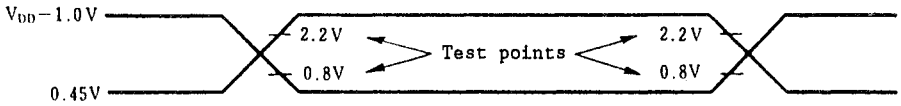
(One-time PROM product: (Ta = -40°C to +85°C, V_{DD} = 5.0V ±10%, V_{SS} = AV_{SS} = 0 V, V_{DD} -0.8 V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ V_{AREF} ≤ AV_{DD})

(EPROM product : (Ta = -40°C to +85°C, V_{DD} = 5.0V ±5%, V_{SS} = AV_{SS} = 0 V, V_{DD} -0.8 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Resolution			8			Bits
Absolute accuracy (Note)		3.4 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 167 ns			±0.8%	FSR
		4.0 ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 167 ns			±0.6%	FSR
		Ta=-10 to +70°C, 4.0 ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 167 ns			±0.4%	FSR
Conversion time	t_{CONV}	66 ns ≤ t_{CYC} ≤ 110 ns	576			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 167 ns	432			t_{CYC}
Sampling time	t_{SAMP}	66 ns ≤ t_{CYC} ≤ 110 ns	96			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 167 ns	72			t_{CYC}
★ Analog input voltage	V_{IAN}	AN0 to AN7 (including the unused pins)	0		V_{AREF}	V
Analog input impedance	R_{AN}			50		MΩ
Reference voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} current	I_{AREF1}	Operating mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} power supply current	A_{IDD1}	Operating mode f_{XX}=15 MHz		0.5	1.3	mA
	A_{IDD2}	STOP mode		10	20	μA

Note Quantization error (±1/2 LSB) is not contained.

AC Timing Test Points



AC Characteristic Calculation Expressions Dependent on t_{CYC}

Parameter	Calculation expression	MIN./MAX.	Unit
t_{AL}	2T-100	MIN.	ns
t_{LA}	T-30	MIN.	ns
t_{AR}	3T-100	MIN.	ns
t_{AD}	7T-220	MAX.	ns
t_{LDR}	5T-200	MAX.	ns
t_{RD}	4T-150	MAX.	ns
t_{LR}	T-50	MIN.	ns
t_{RL}	2T-50	MIN.	ns
t_{RR}	4T-50 (when data is read) 7T-50 (when OP code is fetched)	MIN.	ns
t_{LL}	2T-40	MIN.	ns
t_{AW}	3T-100	MIN.	ns
t_{LDW}	T+110	MAX.	ns
t_{LW}	T-50	MIN.	ns
t_{DW}	4T-100	MIN.	ns
t_{WDH}	2T-70	MIN.	ns
t_{WL}	2T-50	MIN.	ns
t_{WW}	4T-50	MIN.	ns

(to be continued)

(Cont'd)

Parameter	Calculation expression	MIN./MAX.	Unit
★ t_{CYK}	6T ($\overline{SCK}$ input (Note 1))/12T 12T ($\overline{SCK}$ input) (Note 2)	MIN.	ns
	24T ($\overline{SCK}$ output)		
★ t_{KKL}	2.5T + 5 ($\overline{SCK}$ input (Note 1))/ 5T+5 ($\overline{SCK}$ input) (Note 2)	MIN.	ns
	12T-100 ($\overline{SCK}$ output)		
★ t_{KKH}	2.5T + 5 ($\overline{SCK}$ input) (Note 1) 5T+5 ($\overline{SCK}$ input) (Note 2)	MIN.	ns
	12T-100 ($\overline{SCK}$ output)		

Note 1. When the clock rate is x16 or x64 in the asynchronous mode.

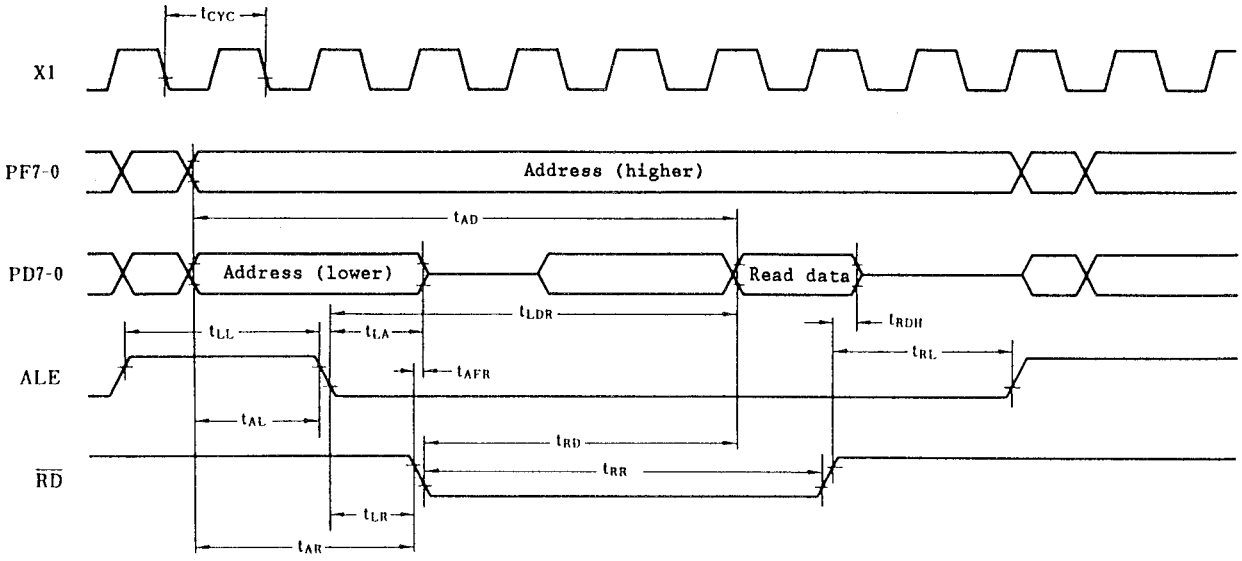
2. When the clock rate is x1 in the asynchronous mode or the synchronous mode or I/O interface mode is set

Remarks 1. $T = t_{CYC} = 1/f_{XX}$

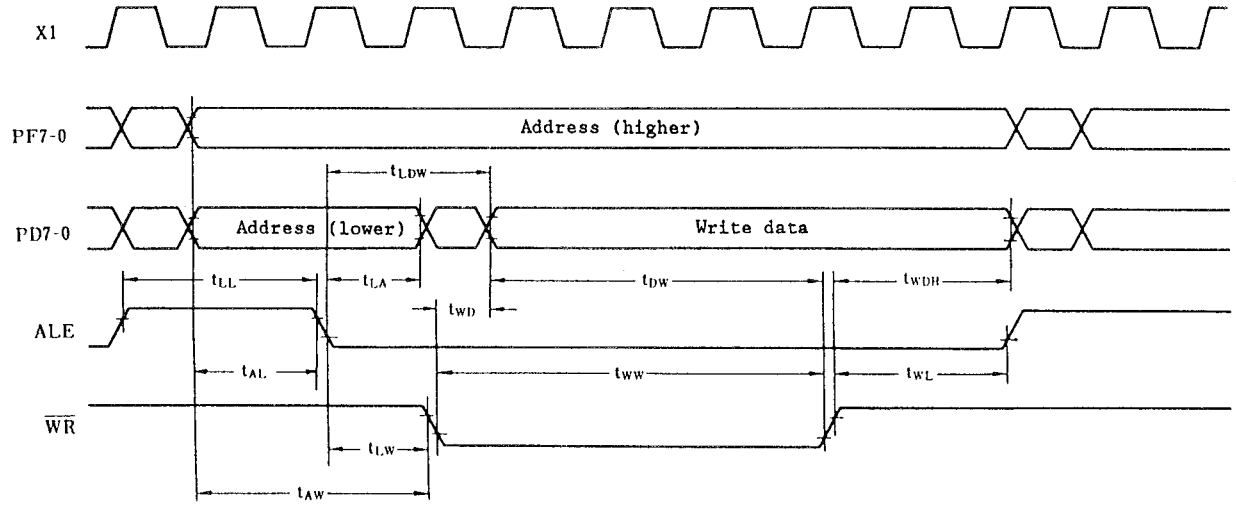
2. Parameters not listed in the table do not depend on the oscillation frequency (f_{XX}).

Timing Waveforms

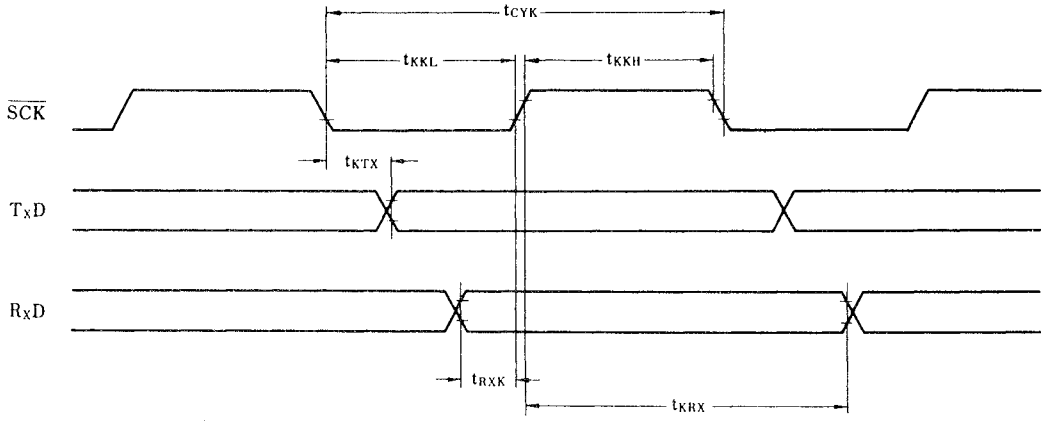
Read Operation



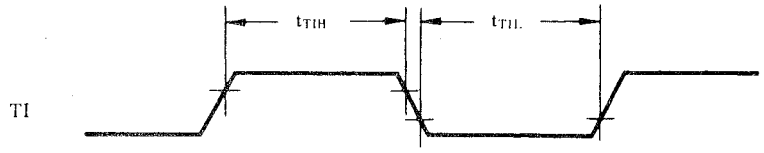
Write Operation



Serial Operation

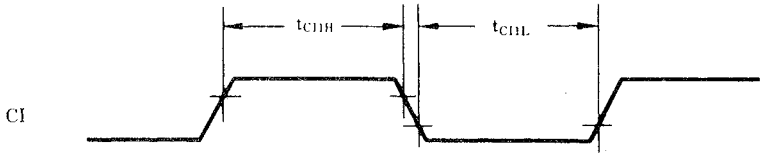


Timer Input Timing

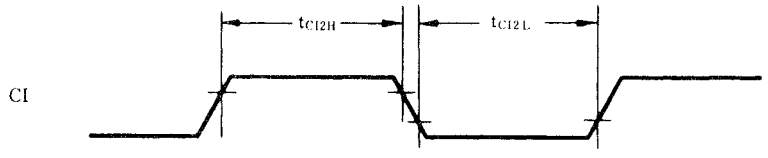


Timer/event Counter Input Timing

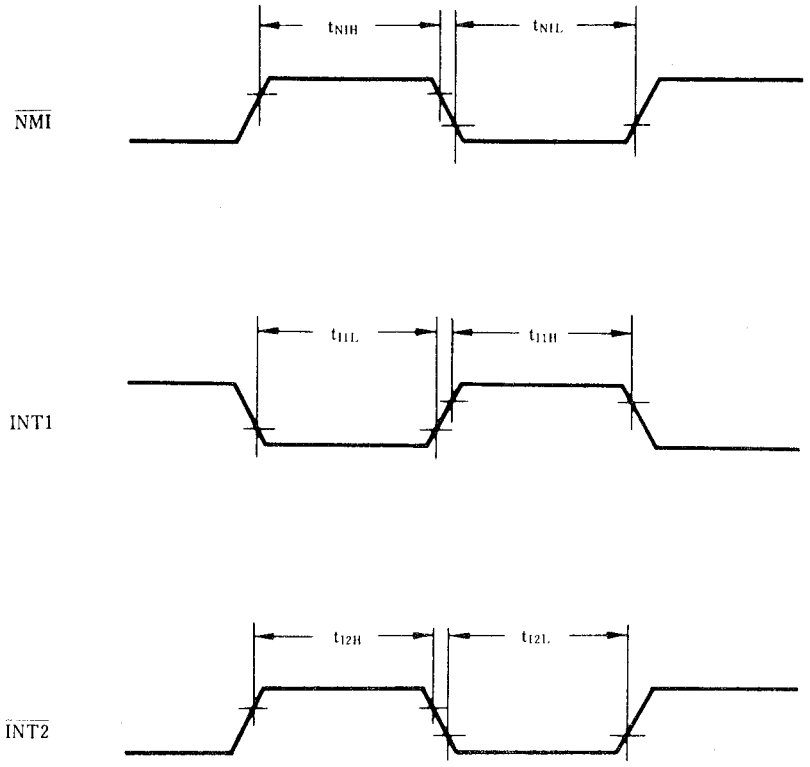
Event counter mode



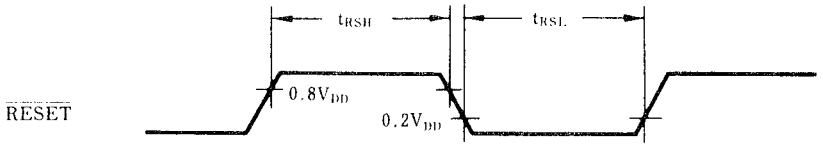
Pulse width measurement mode



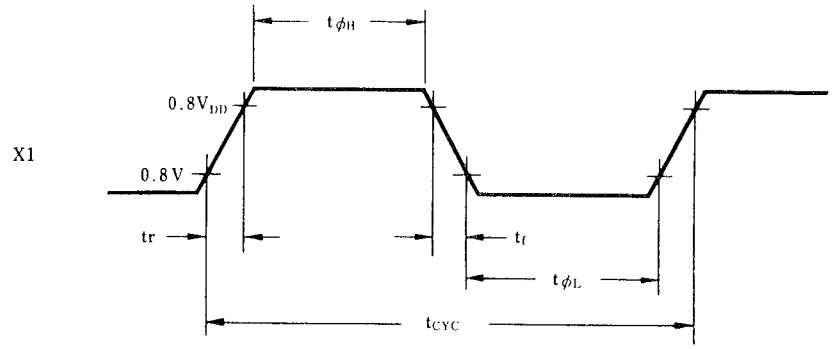
Interrupt Input Timing



Reset Input Timing



External Clock Timing

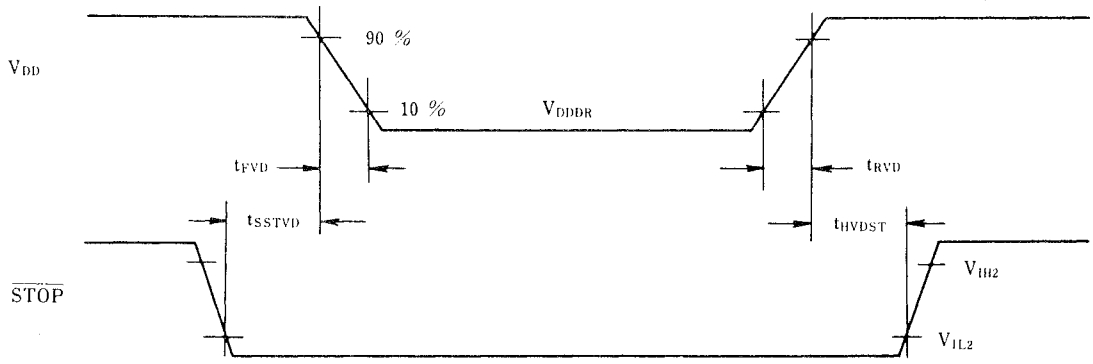


Data Memory STOP Mode Low Power Supply Voltage Data Retention Characteristics (Ta = -40°C to +85°C)

	Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit
	Data retention power supply voltage	V_{DDDR}			2.5		5.25	V
★	Data retention power supply current	I_{DDDR}	One-time PROM product	V_{DDDR} = 2.5 V		1	15	μA
				V_{DDDR} = 5 V±10%		10	50	μA
★			EPROM product	V_{DDDR} = 2.5 V			300	μA
				V_{DDDR} = 5 V ± 5%			1	mA
	V_{DD} rise, fall time	t_{RVD}, t_{FVD}			200			μs
	$\overline{STOP}$ setup time to V_{DD}	t_{SSTVD}			12T+0.5 (Note)			μs
	$\overline{STOP}$ hold time from V_{DD}	t_{HVDST}			12T+0.5 (Note)			μs

Note $T = t_{CYC} = 1/f_{XX}$

Data Retention Timing



DC Programming Characteristics (Ta = 25°C ± 5°C, MODE1 = V_{IL}, MODE0 = V_{IH}, V_{SS} = 0 V)

Parameter	Symbol	Symbol (Note)	Test condition	MIN.	TYP.	MAX.	Unit
Input high voltage	V_{IH}	V_{IH}		2.2		V_{DDP} +0.3	V
Input low voltage	V_{IL}	V_{IL}		-0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$; except for INT1, TI(PC3)			±10	μA
Output high voltage	V_{OH}	V_{OH}	I_{OH} = -1.0 mA	V_{DD} -1.0			V
Output low voltage	V_{OL}	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output leakage current	I_{LO}	-	$0 \le V_O \le V_{DDP}$, OE = V_{IH}			±10	μA
V_{DDP} power supply voltage	V_{DDP}	V_{DD}	EPROM programming mode	5.75	6.0	6.25	V
			EPROM read mode	4.5	5.0	5.5	V
V_{PP} power supply voltage	V_{PP}	V_{PP}	EPROM programing mode	12.2	12.5	12.8	V
			EPROM read mode	V_{PP} = V_{DDP}			V
V_{DDP} power supply voltage	I_{DD}	I_{DD}	EPROM programming mode			30	mA
			EPROM read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}			30	mA
V_{PP} power supply voltage	I_{PP}	I_{PP}	EPROM programming mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			30	mA
			EPROM read mode		1	100	uA

Note Corresponding μPD27C256A symbols.

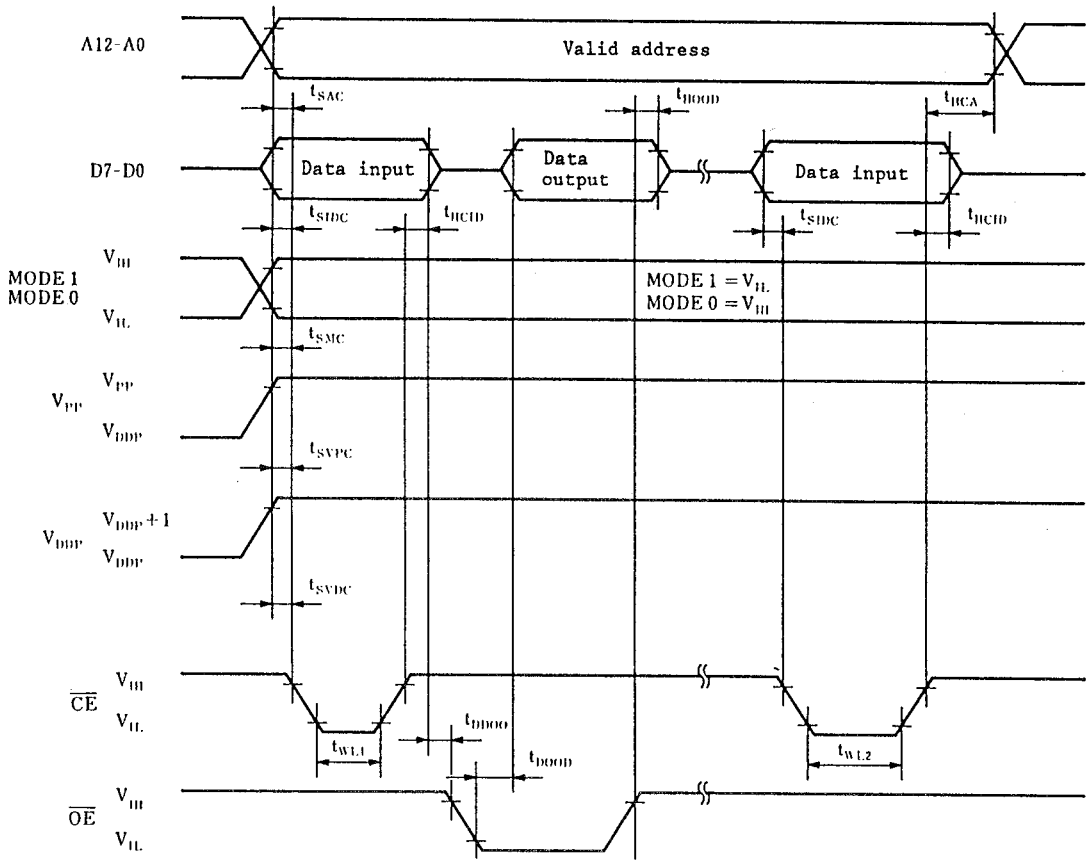
AC Programming Characteristics (Ta = 25 ± 5°C, MODE1 = V_{IL}, MODE0 = V_{IH}, V_{SS} = 0 V)

Parameter	Symbol	Symbol (Note 1)	Test condition	MIN.	TYP.	MAX.	Unit
Address setup time to $\overline{CE}\downarrow$	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}\downarrow$ delay time	t_{DDOO}	t_{OES}		2			μs
Input data setup time to $\overline{CE}\downarrow$	t_{SIDC}	t_{DS}		2			μs
Address hold time from $\overline{CE}\uparrow$	t_{HCA}	t_{AH}		2			μs
Input data hold time from $\overline{CE}\uparrow$	t_{HCID}	t_{DH}		2			μs
Output data hold time from $\overline{OE}\uparrow$	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time to $\overline{CE}\downarrow$	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} setup time to $\overline{CE}\downarrow$	t_{SVDC}	t_{VDS}		2			μs
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Added program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
EPROM programming/read mode setup time to $\overline{CE}\downarrow$ (Note 2)	t_{SMC}	-		2			μs
Address → data output time	t_{DAOD}	t_{ACC}	$\overline{OE}$ = V_{IL}			2	μs
$\overline{CE}\downarrow$ → data output time	t_{DCOD}	t_{CE}				1	μs
$\overline{OE}\downarrow$ → data output time	t_{DOOD}	t_{OE}				1	μs
Data hold time from $\overline{OE}\uparrow$	t_{HCOD}	t_{DF}		0		130	ns
Data hold time from address	t_{HAOD}	t_{OH}	$\overline{OE}$ = V_{IL}	0			ns

Note 1. Corresponding μPD27C256A symbols.

2. When MODE1 = V_{IL} and MODE0 = V_{IH}.

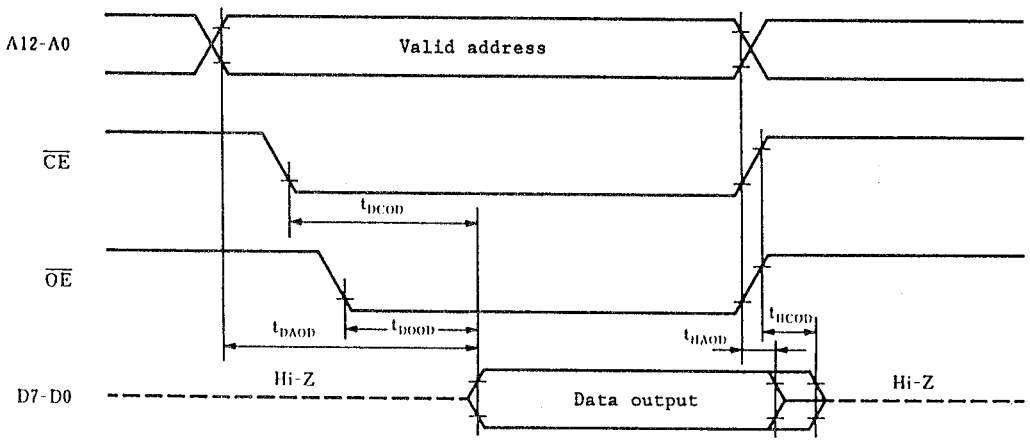
PROM Programming Mode Timing



Caution 1. Apply voltage to V_{DDP} before V_{PP} and turn off V_{DDP} after V_{PP}.

2. Do not apply voltage of +13 V or more containing overshoot to V_{PP}.

PROM Read Mode Timing

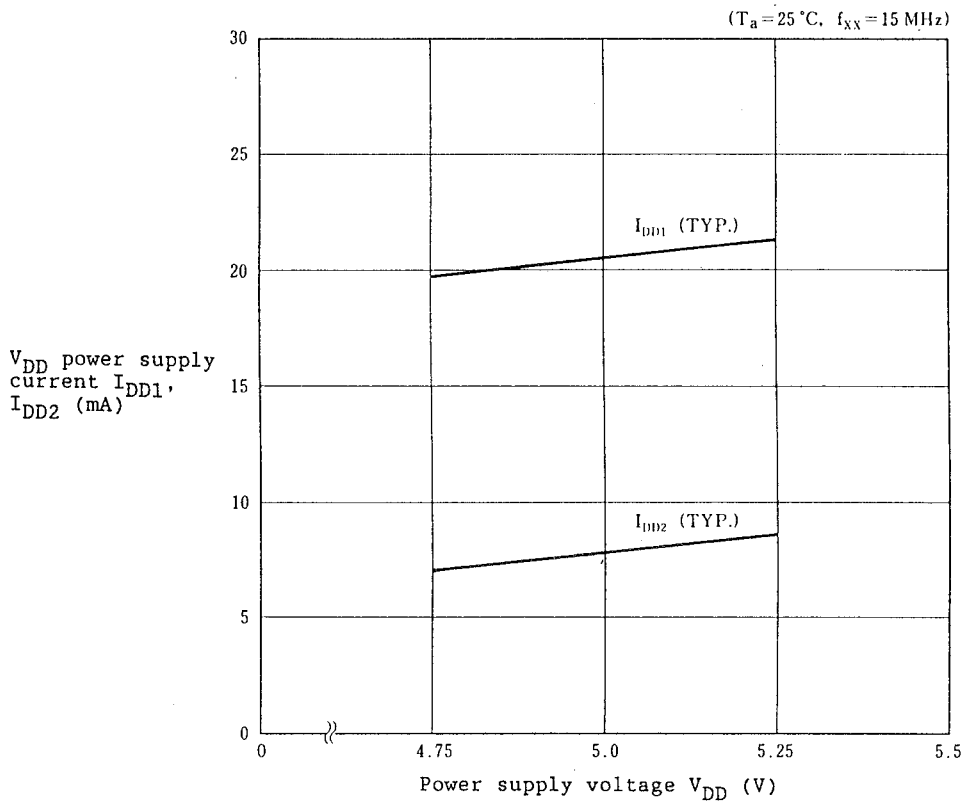


Caution 1. To read EPROM within the t_{DAOD} range, the delay time of $\overline{OE}$ input from the $\overline{CE}$ falling edge must be within $t_{DAOD}-t_{DOOD}$.

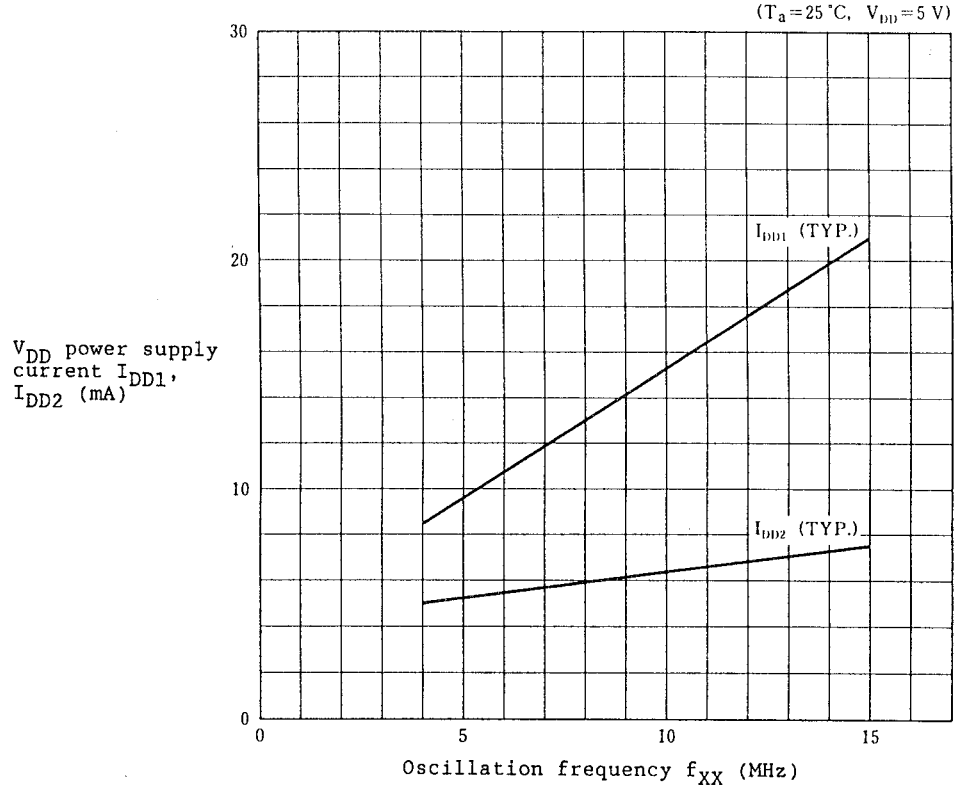
2. t_{HCOD} is the time from the state in which either $\overline{OE}$ or $\overline{CE}$ first becomes V_{IH}.

9. CHARACTERISTIC CURVES (reference value) ★

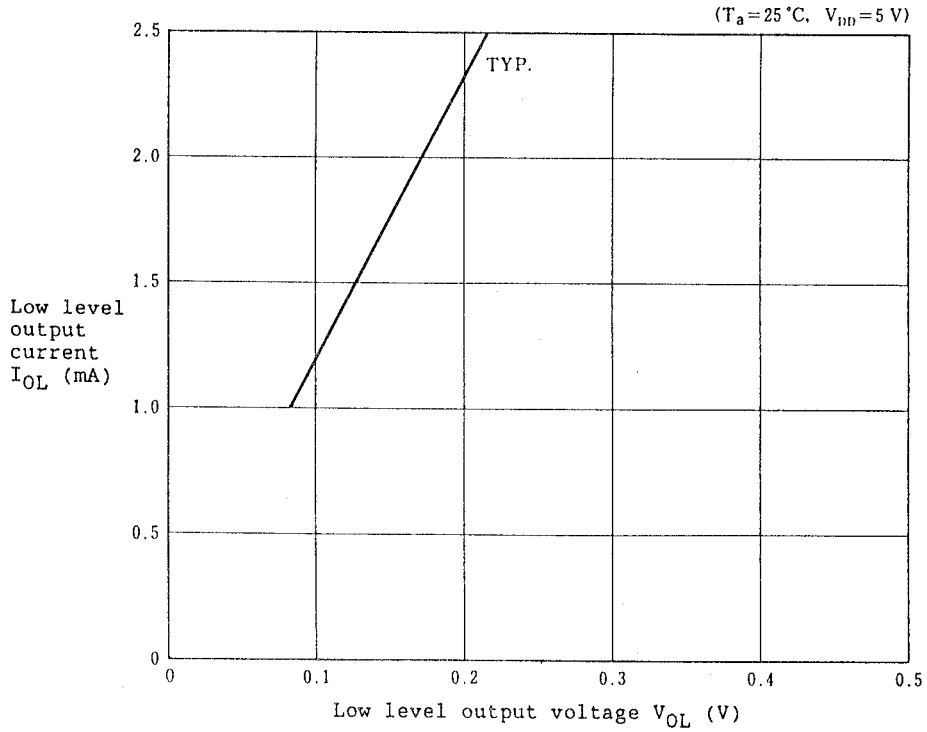
I_{DD1}, I_{DD2} vs V_{DD}



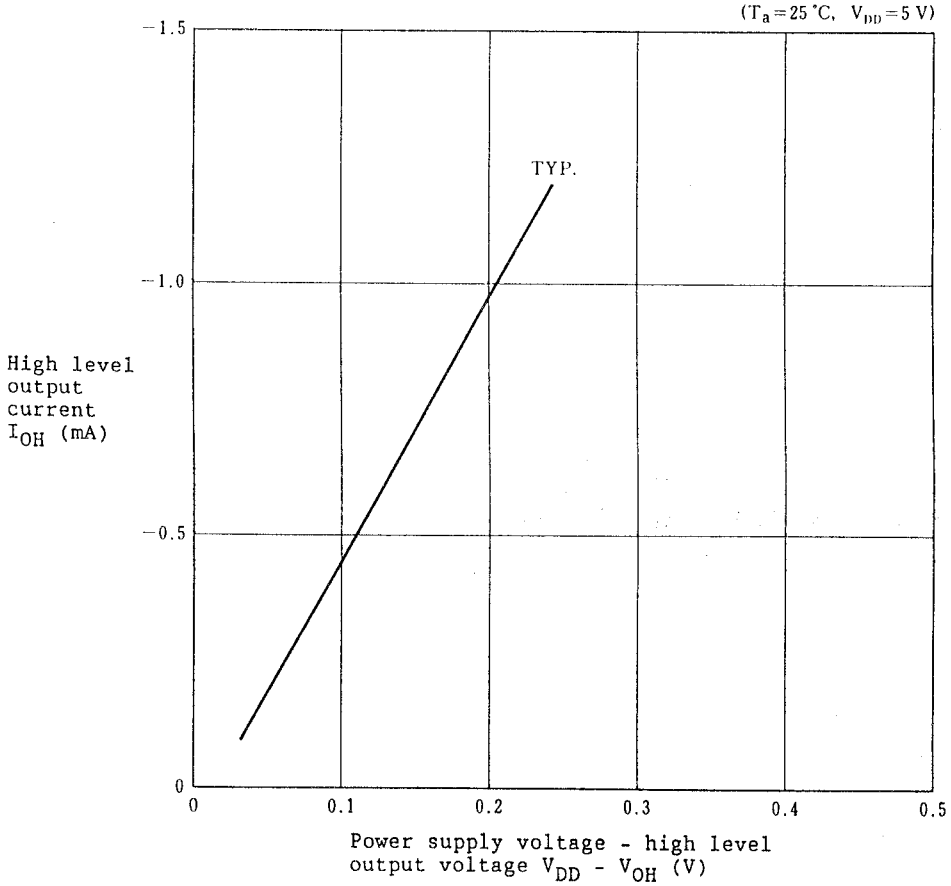
I_{DD1}, I_{DD2} vs f_{XX}



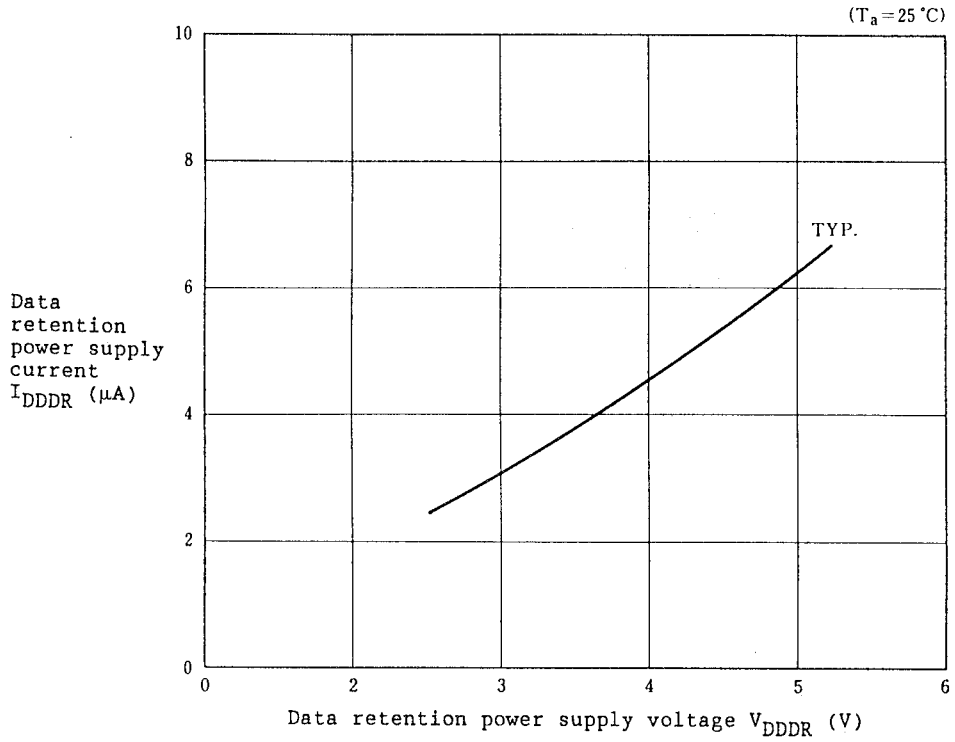
I_{OL} vs V_{OL}



I_{OH} vs V_{OH}

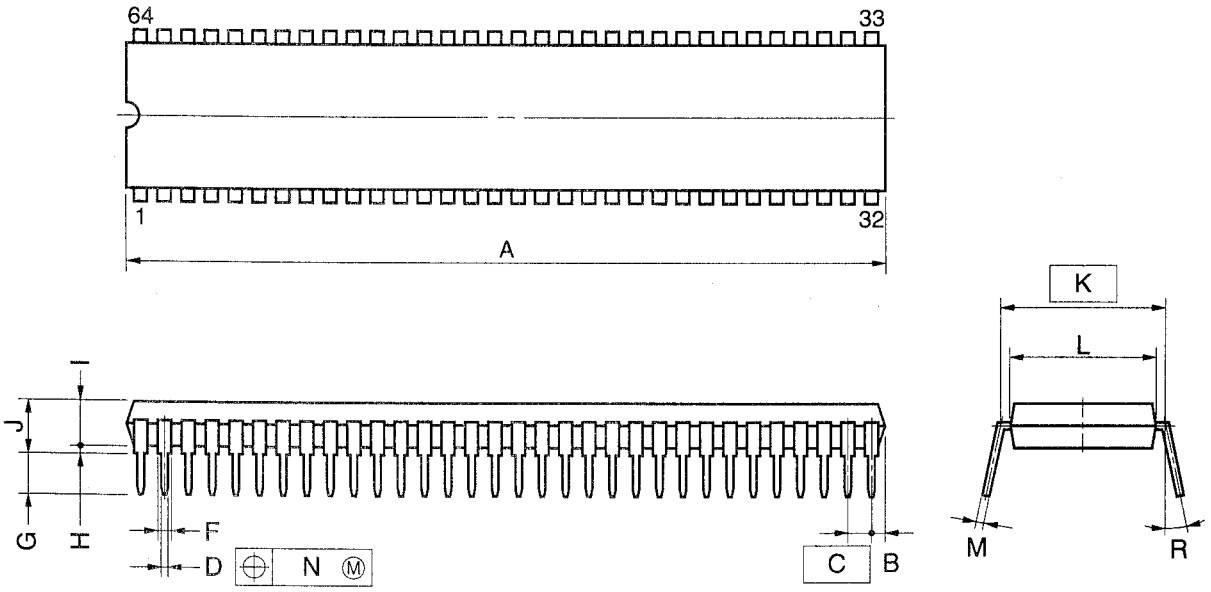


I_{DDDR} vs V_{DDDR}



10. PACKAGE INFORMATION

64 PIN PLASTIC SHRINK DIP (750 mil)



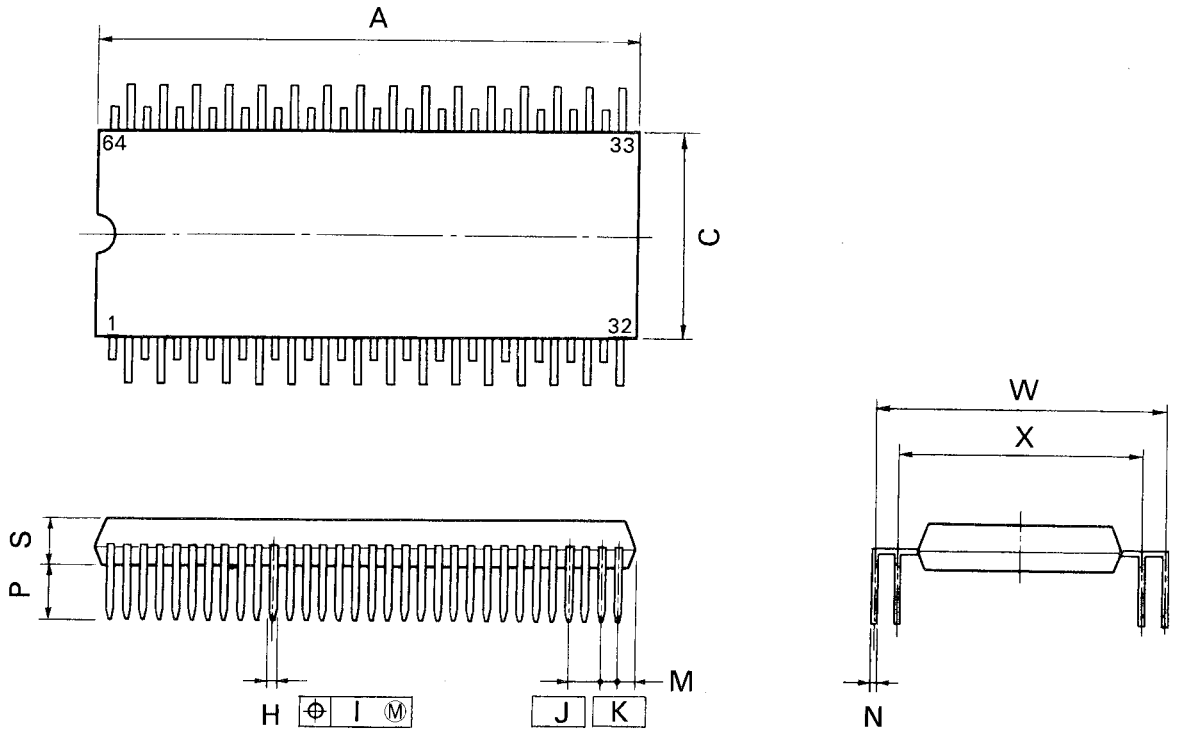
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QUIP



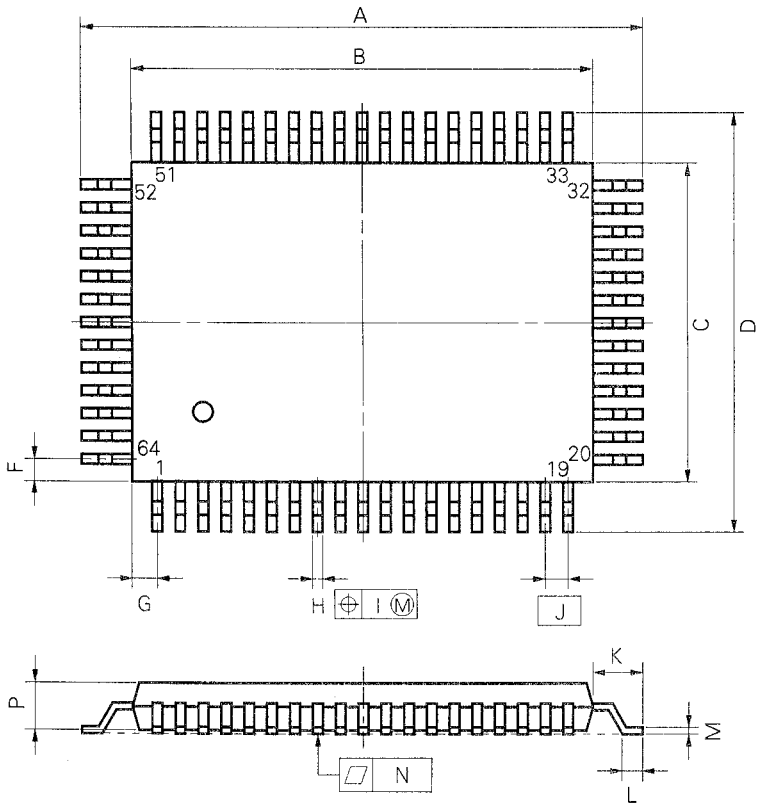
P64GQ-100-36

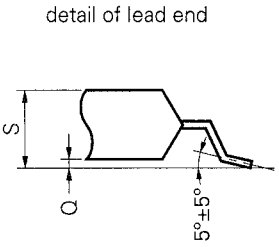
NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$41.5^{+0.3}_{-0.2}$	$1.634^{+0.012}_{-0.008}$
C	16.5	0.650
H	$0.50^{\pm0.10}$	$0.020^{+0.004}_{-0.005}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	$1.1^{+0.25}_{-0.15}$	$0.043^{+0.011}_{-0.006}$
N	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
P	$4.0^{\pm0.3}$	$0.157^{+0.013}_{-0.012}$
S	$3.6^{\pm0.1}$	$0.142^{+0.004}_{-0.005}$
W	$24.13^{\pm1.05}$	$0.950^{\pm0.042}$
X	$19.05^{\pm1.05}$	$0.750^{\pm0.042}$

64 PIN PLASTIC QFP (14×20)





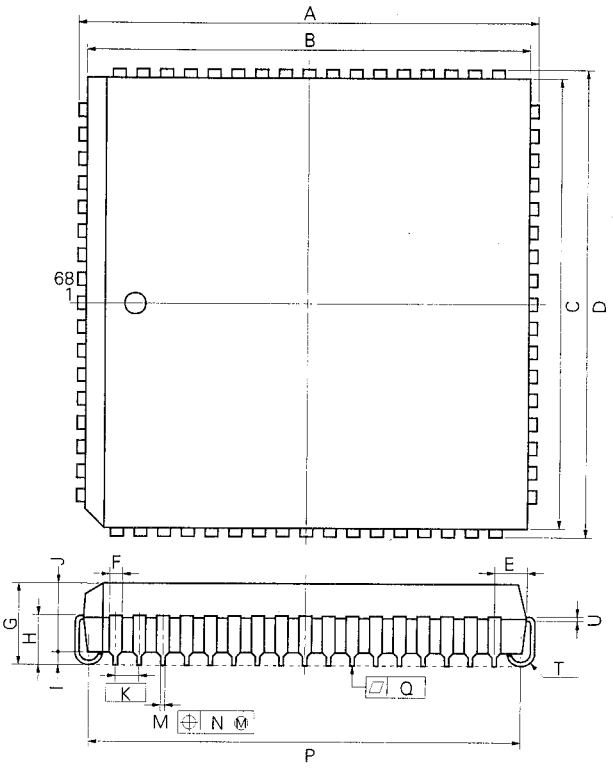
P64GF-100-3B8,3BE,3BR-1

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

68 PIN PLASTIC QFJ (□950 mil)



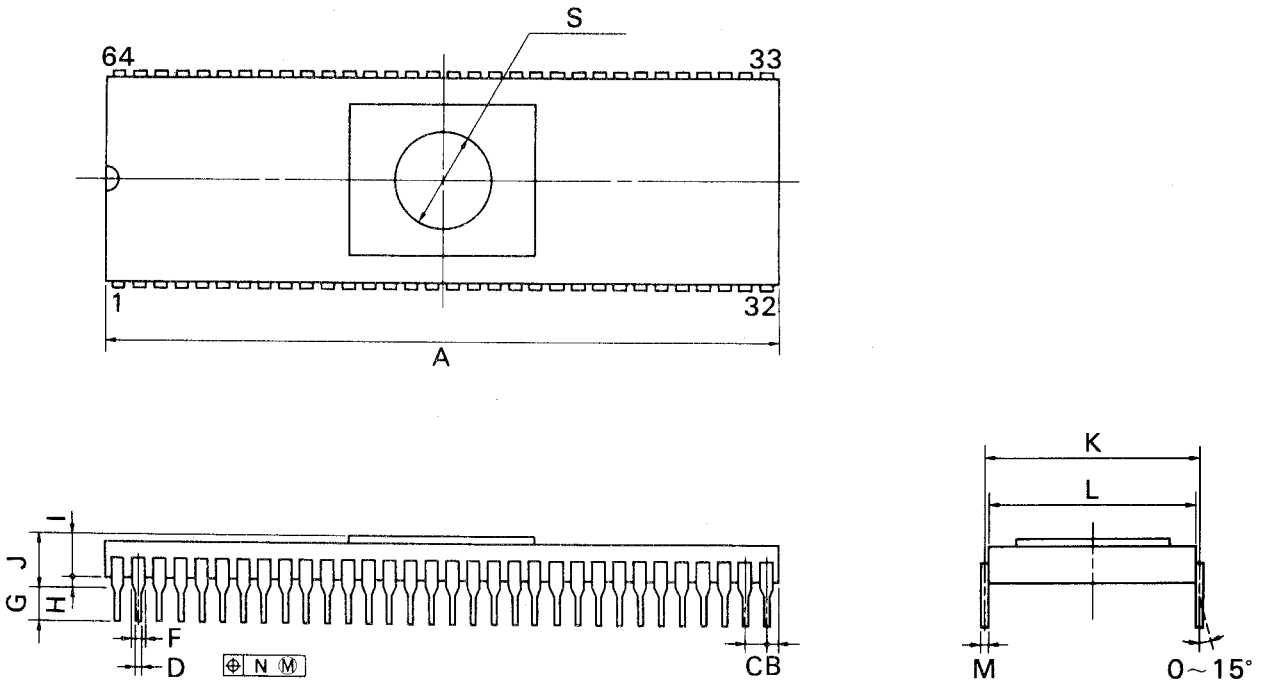
P68L-50A1-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

64PIN CERAMIC SHRINK DIP (750 mil)



P64DW-70-750A

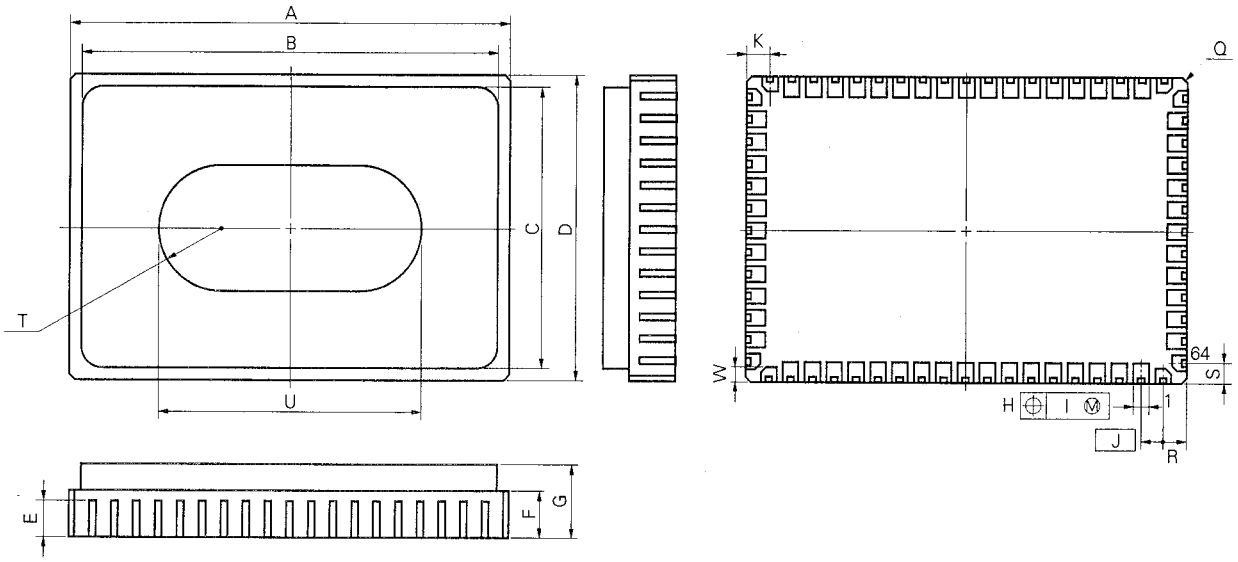
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.310 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.46^{\pm 0.05}$	$0.018^{\pm 0.002}$
F	0.8 MIN.	0.031 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	1.0 MIN.	0.039 MIN.
I	3.0	0.118
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	$0.25^{\pm 0.05}$	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01
S	$\phi 8.89$	$\phi 0.350$

64 PIN CERAMIC WQFN



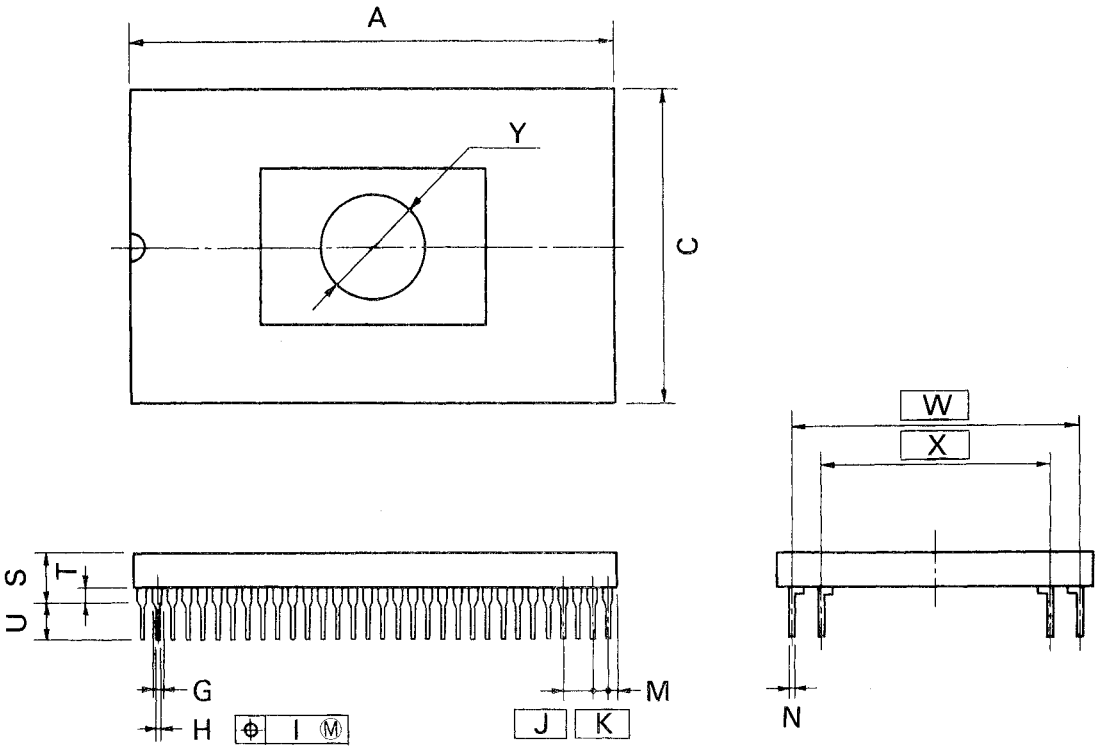
X64KW-100A-2

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	19.0	0.748
C	13.2	0.520
D	14.0±0.4	0.551±0.016
E	1.64	0.065
F	2.14	0.084
G	3.556 MAX.	0.140 MAX.
H	0.7±0.10	$0.028^{+0.004}_{-0.005}$
I	0.10	0.004
J	1.0 (T.P.)	0.039 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.25	C 0.010
R	1.0	0.039
S	1.0	0.039
T	R 3.0	R 0.118
U	12.0	0.472
W	0.8±0.2	$0.031^{+0.009}_{-0.008}$

64 PIN CERAMIC QUIP (WINDOW)



P64RQ-100-A

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	41.91 MAX.	1.650 MAX.
C	$26.67^{\pm 0.4}$	$1.050^{\pm 0.016}$
G	0.92 MIN.	0.036 MIN.
H	$0.46^{\pm 0.05}$	$0.018^{\pm 0.002}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	1.27 MAX.	0.050 MAX.
N	$0.25^{\pm 0.05}$	$0.010^{+0.002}_{-0.003}$
S	4.72 MAX.	0.186 MAX.
T	1.0 MIN.	0.039 MIN.
U	$3.5^{\pm 0.3}$	$0.138^{-0.012}_{-0.013}$
W	24.13	0.950
X	19.05	0.750
Y	ϕ8.89	ϕ0.350

11. RECOMMENDED CONDITIONS FOR SOLDERING ★

Solder the μPD78CP14 under the recommended conditions listed in Table 11-1.

For details of the recommended conditions, refer to the **Semiconductor Device Mount Manual (IEI-616).**

Consult the sales person about soldering methods and soldering conditions not listed in the table.

Table 11-1. Soldering Conditions for Surface Mount Type

(1) μPD78CP14GF-3BE: 64-pin Plastic QFP (14x20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: Within 30s (at 210°C or higher), Count: Within twice, limited number of days: Seven (Note) (after seven days, prebake at 125°C is required for 20 hours) <Attention> (1) Perform the second reflow at the time the device temperature is lowered to the room temperature from the heating by the first reflow. (2) Do not wash the soldered portion with the flux following the first reflow.	IR35-207-2
VPS	Package peak temperature: 215°C, Time: Within 40S (at 200°C or higher), Count: Within twice, limited number of days: Seven (Note) (after seven days, prebake at 125°C is required for 20 hours) <Attention> (1) Perform the second reflow at the time the device temperature is lowered to the room temperature from the heating by the first reflow. (2) Do not wash the soldered portion with the flux following the first reflow.	VP15-207-2
Wave soldering	Soldering tank temperature: 260°C or less, Time: Within 10s, Count: Once, Preheating temperature: 120°C MAX. (package surface temperature), limited number of days: Seven (after seven days, prebake at 125°C is required for 20 hours)	WS60-207-1
Pin part heating	Pin part temperature: 300°C or less, Time: Within 3s (per frame of device)	—

Note It is the number of storage days under the storage conditions of 25°C and 65% RH or less after the dry pack is opened.

Caution Do not use the soldering methods together (except the pin part heating).

(2) μPD78CP14L: 68-pin plastic QFJ (□950 mil)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
VPS	Package peak temperature: 215°C, Time: Within 40s (200°C or higher), Count: Once, limited number of days: Two (Note) (after two days, prebake at 125°C is required for 16 hours)	VP15-162-1
Pin part heating	Pin part temperature: 300°C or less, Time: Within 3s (per frame of device)	—

Note It is the number of storage days under the storage conditions of 25°C and 65% RH or less after the dry pack is opened.

Table 11-2. Soldering Conditions for Insertion Type

μPD78CP14CW: 64-pin plastic shrink DIP (750 mil)
μPD78CP14G-36: 64-pin plastic QUIP
μPD78CP14DW: 64-pin shrink DIP with a ceramic window (750 mil)
μPD78CP14R: 64-pin QUIP with a ceramic window

Soldering Method	Soldering Conditions
Wave Soldering (pin part only)	Soldering tank temperature: 260°C or less, Time: Within 10s
Pin part heating	Pin part temperature: 300°C or less, Time: Within 3s (per pin part)

Note Apply wave soldering only to the pin part and be careful so as not to bring solder injection directly into contact with the package.

12. DIFFERENCES BETWEEN μPD78CP14 AND MASK ROM PRODUCTS

Table 12-1 Differences between μPD78CP14 and Mask ROM Products

Item	μPD78CP14	μPD78C14	μPD78C12A	μPD78C11/A
Internal program memory	o PROM o 16384 x 8 bits	o Mask ROM o 16384 x 8 bits	o Mask ROM o 8192 x 8 bits	o Mask ROM o 4096 x 8 bits
Pin	PB7/$\overline{OE}$	PB7		
	PB6/$\overline{CE}$	PB6		
	$\overline{STOP}/V_{PP}$	$\overline{STOP}$		
	$\overline{NMI}$/A9	$\overline{NMI}$		
	PA7-0/A7-0	PA7-0		
	PF5-2/A13-10	PF5-2		
	PF0/A8	PF0		
	PD7-0/O7-0	PD7-0		
Mode set by using MODE pins (when MODE0 is set to 1 and MODE 1 to 0)	PROM programming mode	. Operation as μPD78C10A (ROMless mode) . External memory 16K extension mode		
MODE0 pin input/output function	Input only	Input/output		
Emulation mode	Not included	Included		
Specification of internal ROM access range by using MM register	Made	Not made		
Package	. 64-pin plastic shrink-DIP (750 mil) . 64-pin plastic QUIP . 64-pin plastic QFP (14 x 20 mil) . 68-pin QFJ (□950 mil) . 64-pin ceramic shrink DIP with a window (750 mil) . 64-pin ceramic QUIP with a window . 64-pin ceramic WQFN	. 64-pin plastic shrink DIP (750 mm) . 64-pin plastic QUIP . 64-pin plastic QUIP straight . 64-pin plastic QFP (thickness 2.7 mm) . 64-pin plastic QFP (14 x 20 mm) (thickness 2.05 mm) (Note) . 68-pin plastic QFJ (□950 mil)		

Note Only μPD78C14.

★

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD78CP14:

Language processor

87AD series relocatable assembler	This program converts programs written in mnemonics into object code that can be executed by microcomputers. In addition, the program contains the functions of automatic symbol table generation, branch instruction optimization process, etc.			
	Host machine	OS	Distribution media	Ordering code (product name)
	PC-9800 series	MS-DOS™ Ver. 2.11 to (Note) Ver. 5.00A	3.5-inch 2HD	μS5A13RA87
			5-inch 2HD	μS5A10RA87
	IBM PC/AT™	PC DOS™ (Ver. 3.1)	5-inch 2HC	μS7B10RA87

PROM write tools

Hard-ware	PG-1500	PG-1500 is a PROM programmer which enables you to program single chip microcomputers containing PROM in stand-alone or host machine operation by connecting an attached board and optional programmer adapter to PG-1500. It also enables you to program typical PROM devices of 256 bits to 4M bits.		
	PA-78CP14CW/ GF/GQ/KB/L	PROM programmer adapters for the μPD78CP14, connected to PG-1500 for use.		
	PA-78CP14CW	μPD78CP14CW, 78CP14DW		
	PA-78CP14GF	μPD78CP14GF-3BE		
	PA-78CP14GQ	μPD78CP14G-36, 78CP14R		
	PA-78CP14KB	μPD78CP14KB		
	PA-78CP14L	μPD78CP14L		
Soft-ware	PG-1500 controller	PG-1500 and a host machine are connected by a serial or parallel interface and PG-1500 is controlled on the host machine.		
		Host machine	OS	Distribution media	Part number (product name)
		PC-9800 series	MS-DOS Ver. 2.11 to (Note) Ver. 5.00A	3.5-inch 2HD	μS5A13PG1500
				5-inch 2HD	μS5A10PG1500
		IBM PC series	PC DOS (Ver. 3.1)	5-inch 2D	μS7B11PG1500

Note Task-swap function, provided to Ver. 5.00/5.00A, is not available on this software.

Remarks Operation of the assembler, PG-1500 controller, etc., is guaranteed only on the host machine under the operating system listed above.

Debugging tool

In-circuit emulator (IE-78C11-M) is provided as the program debugging tool of the μPD78CP14. The system configuration is listed below:

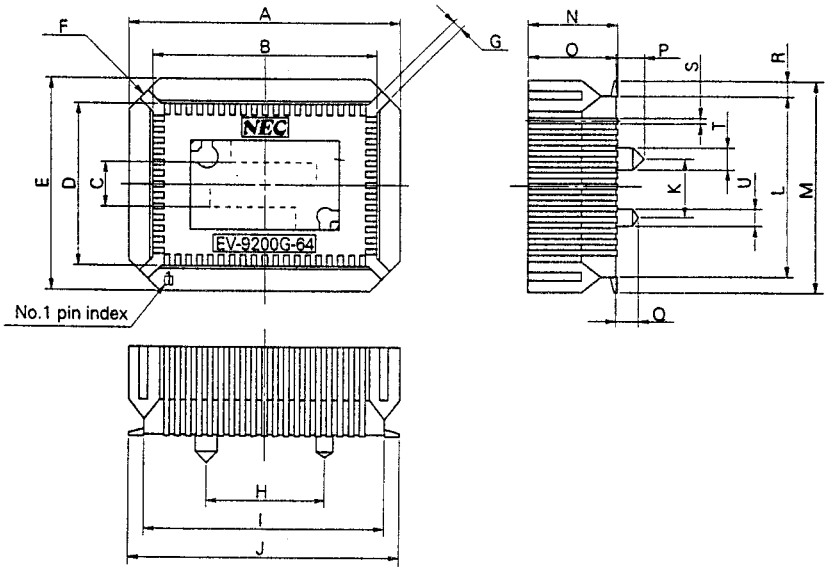
<table>
<tr><td rowspan="3">Hard-ware</td><td>IE-78C11-M</td><td colspan="4">IE-78C11-M is an in-circuit emulator for the 87AD series. For plastic quad-in-line packages, use IE-78C11-M only. For plastic shrunk-dual-in-line packages, use IE-78C11-M and a conversion socket in combination. IE-78C11-M can be connected to a host machine and PROM programmer for efficient debugging.</td></tr>
<tr><td>EV-9001-64</td><td colspan="4">Conversion socket for plastic shrunk-dual-in-line packages. Use the conversion socket and IE-78C11-M in combination.</td></tr>
<tr><td>EV-9200G-64</td><td colspan="4">Conversion socket for 64-pin WQFN. Use EV-9200G-64 and μPD78CP14KB for substitution for 64-pin plastic QFP with a window.</td></tr>
<tr><td rowspan="4">Soft-ware</td><td rowspan="4">IE-78C11-M control program</td><td colspan="4">IE-78C11-M and a host machine are connected by RS-232-C interface and IE-78C11-M is controlled on the host machine.</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number (product name)</td></tr>
<tr></tr>
<tr><td rowspan="2">PC-9800 series</td><td rowspan="2">MS-DOS (Ver. 2.11 to Ver. 3.30D)</td><td>3.5-inch 2HD</td><td>μS5A13IE78C11</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10IE78C11</td></tr>
<tr><td>IBM PC/AT</td><td>PC DOS (Ver. 3.1)</td><td>5-inch 2HC</td><td>μS7B10IE78C11</td></tr>
</table>

Remarks Operation of the assembler, IE controller, etc., is guaranteed only on the host machine under the operating system listed above.

APPENDIX B.
PACKAGE INFORMATION OF CONVERSION SOCKETS AND RECOMMENDED PATTERNS FOR BOARD FIXING

FIGURE B-1. Package Drawings of Conversion Socket (EV-9200G-64) (Reference)

Based on EV-9200G-64
(1) Package drawing (in mm)

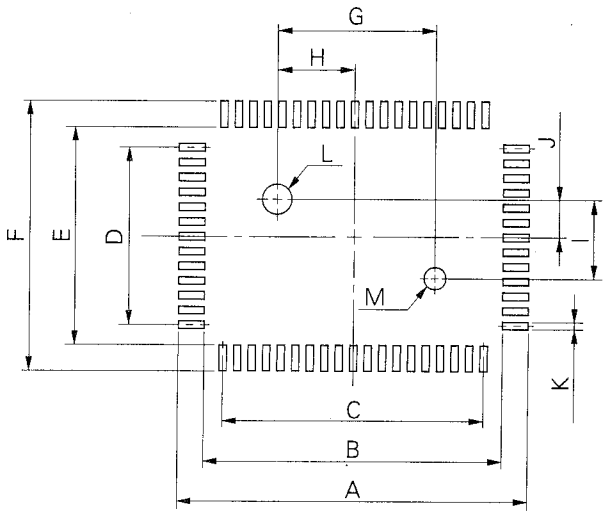


EV-9200G-64-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.30	0.799
C	4.0	0.157
D	14.45	0.569
E	19.0	0.748
F	4-C 2.8	4-C 0.11
G	0.8	0.031
H	11.0	0.433
I	22.0	0.866
J	24.7	0.972
K	5.0	0.197
L	16.2	0.638
M	18.9	0.744
O	8.0	0.315
N	7.8	0.307
P	2.5	0.098
Q	2.0	0.079
R	1.35	0.053
S	0.35±0.1	$0.014^{+0.004}_{-0.005}$
T	ϕ2.3	ϕ0.091
U	ϕ1.5	ϕ0.059

FIGURE B-2. Reccommended Patterns for Board Fixing of Conversion Socket (EV-9200G-64) (Reference)

Based on EV-9200G-64
(2) Pad drawing (in mm)



EV-9200G-64-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	1.0±0.02 × 18=18.0±0.05	$0.039^{+0.002}_{-0.001} \times 0.709 = 0.709^{+0.002}_{-0.003}$
D	1.0±0.02 × 12=12.0±0.05	$0.039^{+0.002}_{-0.001} \times 0.472 = 0.472^{+0.003}_{-0.002}$
E	15.2	0.598
F	19.9	0.783
G	11.00±0.08	$0.433^{+0.004}_{-0.003}$
H	5.50±0.03	$0.217^{+0.001}_{-0.002}$
I	5.00±0.08	$0.197^{+0.003}_{-0.004}$
J	2.50±0.03	$0.098^{+0.002}_{-0.001}$
K	0.6±0.02	$0.024^{+0.001}_{-0.002}$
L	ϕ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
M	ϕ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

NOTES FOR CMOS DEVICES

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being on output pins. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

〔MEMO〕

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