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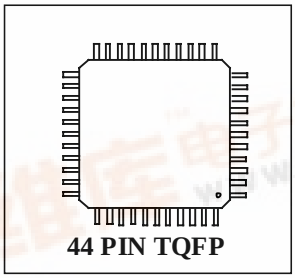
GJRF400
SINGLE CHIP RF TRANSCEIVER

The GJRF400 is a single chip integrated circuit for radio-based frequency hopping spread spectrum communication. (FHSS) The circuit is easily applied and RF-knowledge requirements are minimal. The circuit can be utilised in homes, health care and industry in various ways and can be applied in alarms, garage ports, remote controls, etc., and in more complex systems for control, monitoring and low data-rate communication between computers. A typical system consists of a microprocessor and a radio circuit plus some external components.



Features

All active RF circuits on a single chip
5mW output power
-110dBm sensitivity
9600 bits/ second data rate
3 Volt supply
16mA in receive, 25mA in transmit
4 wire connection for control
3 wire external gain control

Applications

Wireless local networks
Frequency hopping high security alarms
2 way paging
Telemetry
Environmental control systems
Wireless data repeaters
Personnel, patient logging
Access and movement monitoring
Remote Metering
Barcode Readers

Quick reference data:

Parameters	Min.	Typ.	Max.	Unit
Operating frequency	300	434	500	MHz
Transmit data rate		9600[1]	19200	bps
Receiver sensitivity		-110[2]		dBm
Output power (50Ω)		5		mW
Supply voltage	2.7	3.0	3.3	V
Supply current receive mode		16		mA
Supply current transmit mode		25		mA
Power down current		1		µA
Operating temperature range[3]	-40	25	+85	°C

[1]Modulation is applied to the VCO and is based on a transmission code where the baudrate is twice the bitrate (e.g. Manchester code). 9600bps = 19200 baud
[2]Measured at 1200 bps and frequency deviation ± 10kHz (XCO modulation). The baudrate is equal to the bit rate.
[3]Tentative specification.
Parameter temperature dependency will be specified after full characterisation.

Ordering information:

	Package	
Type number	**Name**	**Description**
GJRF400	TQFP44	44 pin plastic thin quad flat package

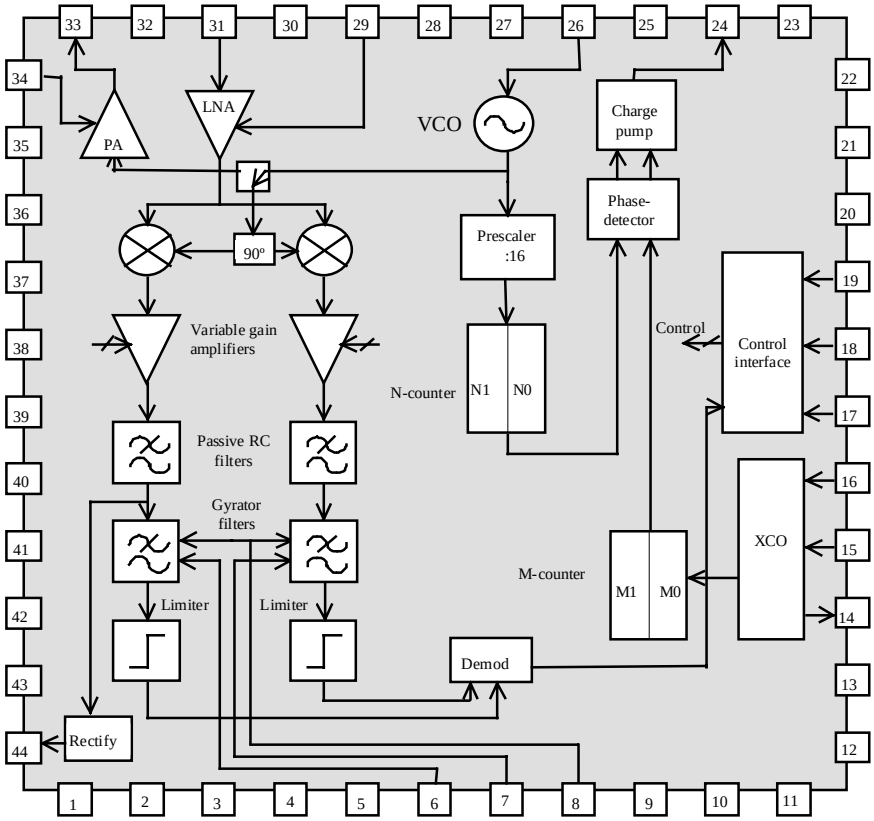


Figure 1: Transceiver Internal Blocks

Table 1: Pin description

Symbol	Pin	Description	Symbol	Pin	Description
RecC	1	rectifier capacitor	ground	23	ground for substrate
QchOut	2	Q-channel output	CmpOut	24	charge-pump (phase detector) output
IchOut	3	I-channel output	OscGnd	25	Colpitts oscillator and substrate ground
IFVdd	4	IF circuitry power	OscIn	26	Colpitts oscillator input (resonator connection)
IFGnd	5	IF circuitry ground	OscVdd	27	power for Colpitts oscillator
Vb_lp1	6	gyrator filter resistor	RFVdd	28	power for LNA and PA
Vb_lp2	7	gyrator filter resistor	LNA_C	29	external capacitor to stabilise LNA
NC	8	no connection	LNAGnd	30	LNA first stage ground
ground	9	substrate ground	RFin	31	low noise RF amplifier (LNA) input
IchC	10	I-channel amplifier capacitor	RFGnd	32	LNA, PA and substrate ground
QchC	11	Q-channel amplifier capacitor	RFout	33	power amplifier output
GuardVdd	12	guardring power	PAbias	34	external bias resistor for power amplifier
DigGnd	13	digital circuitry ground	MixerVdd	35	mixer power
ModOut	14	o/p for VCO/Xtal modulation	MixerGdd	36	mixer ground
XoscOut	15	crystal oscillator output	qc2	37	capacitor connection for Q-channel IF amplifier
XoscIn	16	crystal oscillator input	qc1	38	capacitor connection for Q-channel IF amplifier
DataIXO	17	bidirectional data	ic1	39	capacitor connection for I-channel IF amplifier
Clock	18	clock	ic2	40	capacitor connection for I-channel IF amplifier
Load	19	load	A0	41	gain set input for IF amplifier
DigVdd	20	digital circuitry power	A1	42	gain set input for IF amplifier
RxOutD	21	I/Q channel digital output	A2	43	gain set input for IF amplifier
DataC	22	data filter capacitor	RecOut	44	I channel signal level rectified output

Detailed Description

The transmitter consists of a PLL frequency synthesiser and a power amplifier. The frequency synthesiser consists of a voltage controlled oscillator (VCO), a crystal oscillator, prescaler, programmable frequency dividers and a phase-detector. The loop-filter is external for flexibility The VCO is a Colpitts oscillator and needs an external resonator and varicap. FSK modulation can be applied externally to the VCO or to the crystal oscillator. The synthesiser has two different, N and M, frequency dividers. For low bitrate applications (approximate 100 bps) FSK modulation can be implemented by switching between these dividers. The lengths of the N and M registers are 12 and 10 bits respectively. For all types of FSK modulation, data is entered at the Data IXO pin (see application circuit, Figure 7).

In receive mode the PLL synthesiser generates the local oscillator (LO) signal. The N and M values that give the LO frequency are stored in the N0 and M0 registers. The receiver is a zero intermediate frequency (IF) type in order to make channel filtering possible with low-power integrated low-pass filters. The receiver consists of a low noise amplifier (LNA) that drives a quadrature mixer pair. The mixer outputs feed two identical signal channels in phase quadrature.

Each channel includes a variable gain amplifier, a second order passive RC lowpass filter (to protect the gyrator filter from strong adjacent channel signals), a gyrator filter and finally a limiter. The main channel filter is a gyrator-capacitor implementation of a five-pole elliptic lowpass filter. The elliptic filter minimises the total capacitance required for a given selectivity and dynamic range. The lowpass cut-off frequency can be adjusted by an external resistor.

The demodulator demodulates the I and Q channel outputs and produces a digital data output. It detects the relative phase difference of the I and the Q channel signals. If the I channel signal lags the Q channel, the FSK tone frequency lies above the LO frequency (data '1'). If the I channel leads the Q channel, the FSK tone lies below the LO frequency (data '0'). The output of the receiver is available on the Data IXO pin.

A three pin serial interface is used to program the circuit.

External components are necessary for RF input and output impedance matching and decoupling of power. Other external components are VCO resonator and varicap, crystal, feedback capacitors and components for FSK modulation in VCO/crystal oscillator, loop filter, bias resistors for power amplifier and gyrator filters.

Circuit blocks

VCO

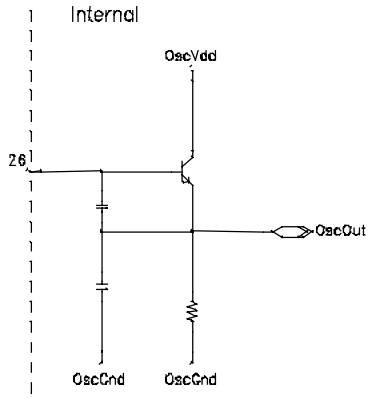


Figure 2: VCO

The VCO is basically a Colpitts oscillator. The oscillator has an external resonator and varicap. The control voltage for the varicap is derived from the phase detector via a passive loop filter.

The VCO's external components should be screened to avoid undue pick-up of external unwanted signals.

Crystal-oscillator

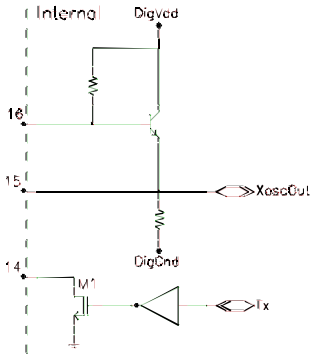


Figure 3: Crystal oscillator

As the crystal oscillator is a reference for the RF output frequency and also for the LO frequency in the receiver, very good phase and frequency stability is required. The crystal oscillator is tuned by varying a trimming capacitor. Passive components in parallel with the internal MOSFET are necessary if FSK modulation is applied to the crystal oscillator. The drift in the RF frequency is the same as the drift in crystal frequency when measured in PPM.

The circuit has been tested with a 10MHz crystal, but other crystal frequencies can be used as well.

Power Amplifier

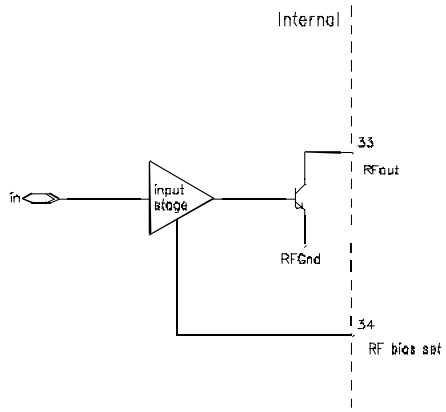


Figure 4: Power Amplifier

The amplifier is a class A amplifier, which is linearized by the effective high-frequency emitter degeneration contributed by the bond wire inductance. The last stage has an open collector, and an external load is therefore necessary. The dc current in the amplifier is adjusted with an external bias resistor. The ratio of the output current (the current flowing in the load and output transistor) to the current in the bias resistor is about 28. The maximum output current is about 15 mA, which gives a maximum bias current of 535uA. A 2.7kΩ bias resistor will give approximately this bias current. The components between the antenna and the output of the power amplifier are for impedance matching. The impedance matching circuit will depend on the type of antenna used.

The power amplifier is turned on internally after the control word is clocked into the shift register. This changes the VCO load and influences the PLL. The PA should be switched on and off externally by the microcontroller to prevent spurious components from being transmitted before the PLL stabilises.

Low noise amplifier (LNA)

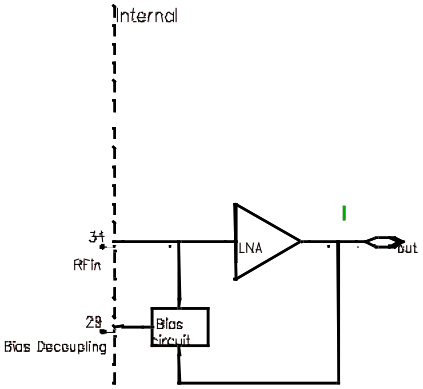


Figure 5: Low noise amplifier

A low noise amplifier in RF receivers is used to boost the incoming signal prior to the frequency conversion process. This is important in order to prevent mixer noise from dominating the overall front-end noise performance. The LNA is a two stage amplifier and has a nominal gain of 20dB at 433.92MHz. The LNA has a dc feedback loop which provides bias for the LNA. An external capacitor decouples and stabilises the overall dc feedback loop which has a large low frequency loop gain. The components between the antenna and the input of the LNA are for impedance matching. The input impedance, measured at 435MHz, is $Z_{IN} = (51 - j45)\Omega$.

IF amplifier (VGA)

Table 2: Gain setting

A2	A1	A0	Gain (dB)
0	0	0	45
0	0	1	40
0	1	0	30
0	1	1	20
1	0	0	10
1	0	1	0
1	1	0	-10
1	1	1	-20

There is one variable gain amplifier in each channel of the receiver. This amplifier is a two stage amplifier with gain from -20dB up to 45dB. Pins A2, A1 and A0 control the gain of the amplifier. The amplifier needs an external capacitor connected between the emitters of the first differential stage to eliminate the effect of offset on the output of the mixers (between pin 36 and 37 , and between pin 38 and 39). Gain is a function of A2, A1 and A0, values are given in table 2.

Rectifier

The receiver includes a half wave rectifier that rectifies the analog signal in the I-channel and converts it to a half wave rectified current that is available on the RecOut pin (pin 44). The output current is approximately 0.4µA per mV of signal amplitude.As the pick-up point of the block is after the VGA, the signal at this pin indicates the internal level at a given gain setting determined by the gain setting pins.
Tolerances in the order of ± 16 dB should be expected.The bit RecSel selects the signal being rectified, i.e. the output of the passive RC filter or the output of the gyrator filter.
RecSel is bit no 51 in the control register.

Passive RC filter

Table 3: Cut off settings

Fc1	Fc0	fc (kHz)
0	0	40
0	1	85
1	0	120
1	1	200

The passive 2nd order RC filter protects the gyrator filter from strong adjacent channel signals. The cut-off frequency can be programmed to the frequencies in table3.
Fcl is bit no 50 in the control register.
Fc0 is bit no 49 in the control register.

Gyrator filters

Table 4: Gyrator filter cut off settings

Rb_{lp} (kΩ)	GmBias	$fc_{lowpass}$ (kHz)
91	0	11
62	0	14.5
30	0	21
20	1	30.5
13	1	47
6.8	1	84

The main receiver channel filter is a gyrator-capacitor implementation of a five-pole elliptic lowpass filter. The lowpass cut-off frequencies can be adjusted by external resistors. Table 4 shows the cut-off frequency of the gyrator filter as a function of bias resistor value. The input signal amplitude should not exceed 100mVpp for the gyrator filter to work properly. When BiasS = 1 the gyrator filter in the I and the Q-channel uses the same bias circuit. The external bias resistor Rblp must be connected to pin Vb_lp1. When BiasS = 0 the lowpass filters uses separate bias circuits. External resistors must be connected to both Vb_lp1 and Vb_lp2. Resistor connected to Vb_lp1 controls the cut-off frequency of the I-channel lowpass filter.
GmBias is bit no 55 in the control register.
BiasS is bit no 53 in the control register.

Limiter

The limiter serves as a zero crossing detector, thus removing amplitude variations in the IF signal, while retaining only the phase variations. It consists of two amplifier stages. The first is a non-inverting one which needs an external capacitor to provide correct dc levels. Its gain is approx. 23.5dB. Gain can be reduced by adding a resistor in series with the capacitor. The second stage has about 50dB gain. The limiter outputs are ideally suited to measure the I-Q phase difference, since its outputs are square waves with sharp edges.

Demodulator

The demodulator demodulates the I and Q channel outputs and produces a digital data output. It detects the relative phase difference of the I and the Q channel signal. If the I channel signal lags the Q channel, the FSK tone frequency lies above the LO frequency (data ‘1’). If the I channel leads the Q channel, the FSK tone lies below the LO frequency (data ‘0’). The output of the receiver is available on the Data IXO pin.
The output of the demodulator is filtered by a first order RC lowpass filter (internal resistor R=100kΩ and external capacitor, pin 22) and then amplified by a Schmitt trigger to produce clean data output. The bandwidth of the filter must be adjusted to the bitrate.

Programming

A three line bus is used to program the circuit; the three lines being: Data IXO, Clock and Load. Data IXO is bi-directional and is used to transmit data, receive data and to program the circuit. The 3-line serial bus interface allows control over the frequency dividers and the selective powering up of Tx, Rx and Synthesiser circuit blocks.

The interface consists of a 59-bit programming register. Data is entered on the Data IXO line with the most significant bit first. The first bit entered is p1, the last one p59. The bits in the programming register are arranged as shown in table 5.

Table 5: Bit allocation

MSB			Register bit allocation		
p1 - p12	p13 - p24	p25 - p34	p35 - p44	p45	p46
N1	N0	M1	M0	BypassLNA	'0'

Register bit allocation						
p47	p48	p49	p50	p51	p52	p53
RxOutD	RxOutD_S	Fc0	Fc1	RecSel	RxOut	BiasS

Register bit allocation					LSB
p54	p55	p56	p57	p58	p59
'0'	GmBias	Mod1	Mod0	R_T	Pd

Table 6: Bit Description

N1	frequency divider N1, 12 bits
N0	frequency divider N0, 12 bits
M1	frequency divider M1, 10 bits
M0	frequency divider M0, 10 bits
BypassLNA	1 = the LNA is bypassed
RxOutD	1 = the I or Q channel digital output is active on the RxOutD pin
RxOutD_S	Selects between the I ('1') and Q ('0') channel digital output
Fc0	Bit to program the cut-off frequency of the RC filters
Fc1	Bit to program the cut-off frequency of the RC filters
RecSel	0 = the rectifier rectifies the output of the I-channel gyrator filter 1 = the rectifier rectifies the output of the I-channel passive RC filter
RxOut	0 = the gyrator filter outputs are active on the IchOut and QchOut pins 1 = the RC filter outputs are active on the IchOut and QchOut pins
BiasS	1 = the I and Q channel lowpass filter uses the same bias circuit, pin Vb_lp1 0 = the I and Q channel lowpass filter uses separate bias circuit, pin Vb_lp1 (I) ,Vb_lp2 (Q)
GmBias	1 = FSK frequency deviation > 30kHz 0 = FSK frequency deviation < 30kHz
Mod1 Mod0	Mod1 = 0, Mod0 = 0: No modulation Mod1 = 0, Mod0 = 1: FSK modulation by switching between different dividers Mod1 = 1, Mod0 = 0: FSK modulation can be applied to the VCO Mod1 = 1, Mod0 = 1: FSK modulation can be applied to the crystal oscillator
R_T	0 = receive mode 1 = transmit mode
Pd	0 = power up 1 = power down

When FSK modulation is applied to the VCO or to the crystal oscillator the PLL is using the dividers N0 and M0. When Mod1 = 0 and Mod0 = 1 it is possible to switch between the different dividers in the PLL.

The switching is controlled by Data IXO. When Data IXO = 0 the PLL uses dividers N0 and M0. When Dat IXO = 1 the PLL uses dividers N1 and M1. Switching between the different dividers can be used to implement low bitrate FSK modulation.

Example 3:

f_{RF} = 433.92MHz, frequency deviation: ±40kHz, f_{XCO} = 10.00MHz (Modulation is applied to the VCO.)

Table 7: Bit function and position

	N1	N0	M1	M0	Bypass LNA	p46	RxOutD	RxOutD_S	Fc0	Fc1
transmit	518	518	191	191	0	0	0	0	1	0
receive	518	518	191	191	0	0	0	0	1	0
	RecSel	RxOut	BiasS	p54	GmBias	Mod1	Mod0	R_T	Pd	
transmit	1	0	1	0	1	1	0	1	0	
receive	1	0	1	0	1	1	0	0	0	

Binary form: (MSB to the left):

```
Transmit:    001000000110  001000000110  0010111111  0010111111  000010101011010
Receive:     001000000110  001000000110  0010111111  0010111111  000010101011000
```

The 59 bit control-word is first read into a shift-register, and is then loaded into a parallel register by a pulse on the Load line. The circuit then goes directly into the specified mode (receive, transmit, etc.). The time the circuit takes to stabilise in the new mode (for instance the time the synthesiser uses to lock on the specified frequency) is used to clock the next control-word into the shift-register. In transmit mode the power amplifier is not active until the next control-word is clocked into the shift-register. Every bit of the control-word that is clocked into the shift-register is counted.

When all the bits have been shifted into the register (59 bits) the counter disables further bits to be clocked in. All clock-pulses after this time are discarded. The circuit is now ready to receive or transmit. The circuit remains in the specified mode until the next load pulse.

As long as the circuit has power the values in the registers are kept. When the power is turned on (for instance when batteries are changed) a pulse on the Load line is necessary to reset the registers and the counter

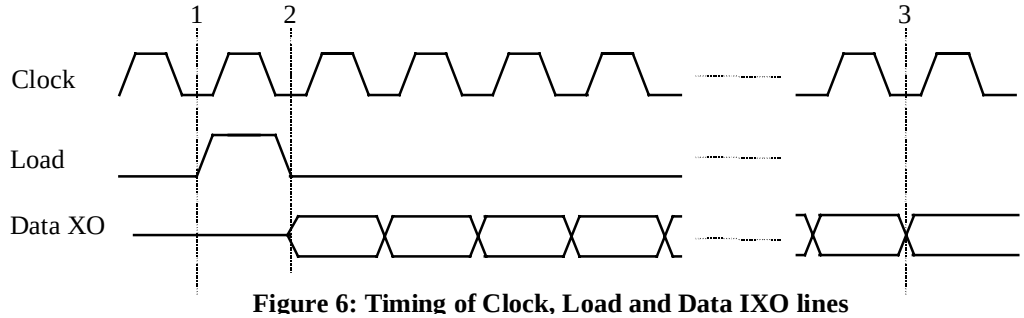


Figure 6: Timing of Clock, Load and Data IXO lines

1: Control-word is loaded into the second register
2: On the first positive clock edge a new control-word starts to be clocked into the shift register
3: After 59 clock pulses the circuit is ready to receive, transmit or sleep. The Data IXO line is now Independent of the Clock line. The Clock line should now be static to minimise noise.

Table 8: Serial I/O Timing Data

Parameter	Min.	Typ.	Max.	Unit
Set up time data to clock		50		ns
Hold time data to clock		+20		ns
Strobe pulse width		50		ns
Clock frequency		10		MHz
Clock pulse width (high)		50		ns

Table 9: Digital I/O Electrical specifications

Parameter	Min.	Typ.	Max.	Unit
Logic Low		0.2		VDD
Logic High		0.7		VDD
3 State Leakage Current		100		nA

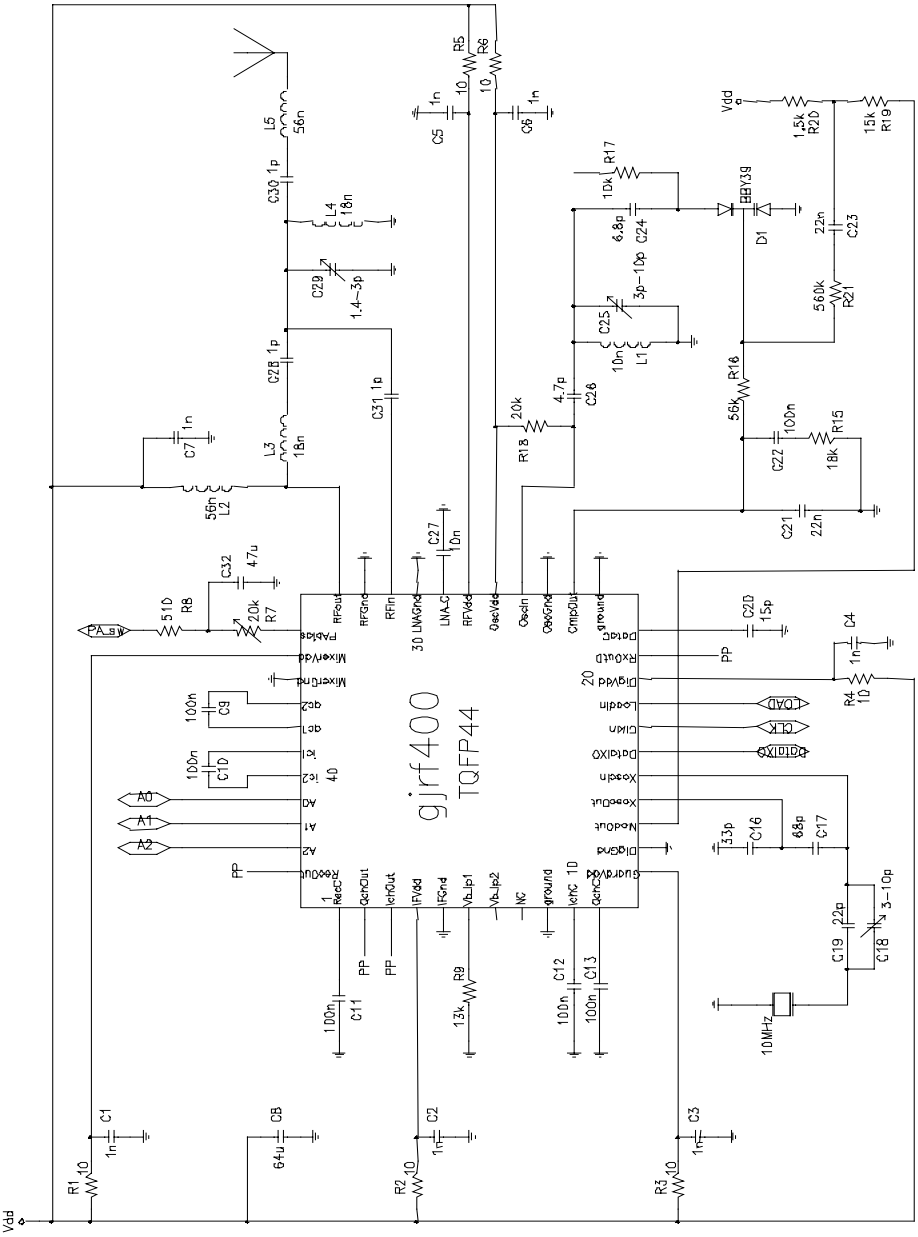


Figure 7: Typical application circuit with direct VCO modulation

Parameters : RF =433.93MHz fXCO = 10MHz. MRx= 257. NRx = 697. MTx= 250 NTx = 678
frequency deviation= ±10kHz. bitrate= 1200bps.

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