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Genesys Logic, Inc.

# GL813 - USB 2.0 CompactFlash Card Reader Controller

*Specification 1.2*

*April 12, 2002*

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# Contents



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# 1. General Description

The GL813 is a high performance, low cost USB2.0 CompactFlash-single card reader controller. With the integration of GenesysLogic own design USB 2.0 high speed UTMI transceiver, the GL813 has made a conspicuous improvement with full speed USB 1.1 card readers on data transfer rate between PC host and flash memory card.

There are totally 4 endpoints in GL813 controller, Control, Bulk In, Bulk Out, and Interrupt. Complies with USB 480Mbps specification ver. 2.0 and USB Storage Class specification ver. 1.0. (Bulk only protocol), the GL813 can support not only plug and play but also Windows ME/ 2000/ XP default driver. For the EMI consideration, the GL813 uses 12MHZ crystal and slew-rate controlled pads to reduce the EMI issue.

The GL813 is 48-pin LQFP package (9mmX9mm) to make the best cost competitive for the high speed single flash card reader design and applications. Also we provide 100-pin LQFP package (14mmX14mm) with external ROM/ Flash for design flexibility.

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## 2. Features

- Complies with Universal Serial Bus specification rev. 2.0.
- Complies with Compact Flash specification rev. 1.4.
- Complies with USB Storage Class specification ver.1.0. (Bulk only protocol)
- Operating system supported: Win XP/ 2000/ ME/ 98/ 98SE; Mac OS 9.X/ X.
- Supports 4 endpoints: Control/ Bulk Read/ Bulk Write/ Interrupt.
- 64/ 512 bytes Data Payload for full / high speed Bulk Endpoint.
- Supports 8-bit / 16-bit Standard PIO mode interface.
- Embedded USB 2.0 UTMI transceiver.
- Embedded 7.5 MIPS RISC CPU.
- Supports external ROM/ Flash modes for design flexibility. (100-pin LQFP)
- Supports Power Down mode and USB suspend indicator.
- Supports USB 2.0 TEST mode features.
- 12MHz external clock to provide better EMI3.3V power input.
- 5V tolerance pad for Compact Flash Card interface.
- Supports EEPROM to customize USB VID / PID and String Descriptors.
- Available in 48-pin (9mmX9mm) / 100-pin (14mmX14mm) LQFP package.

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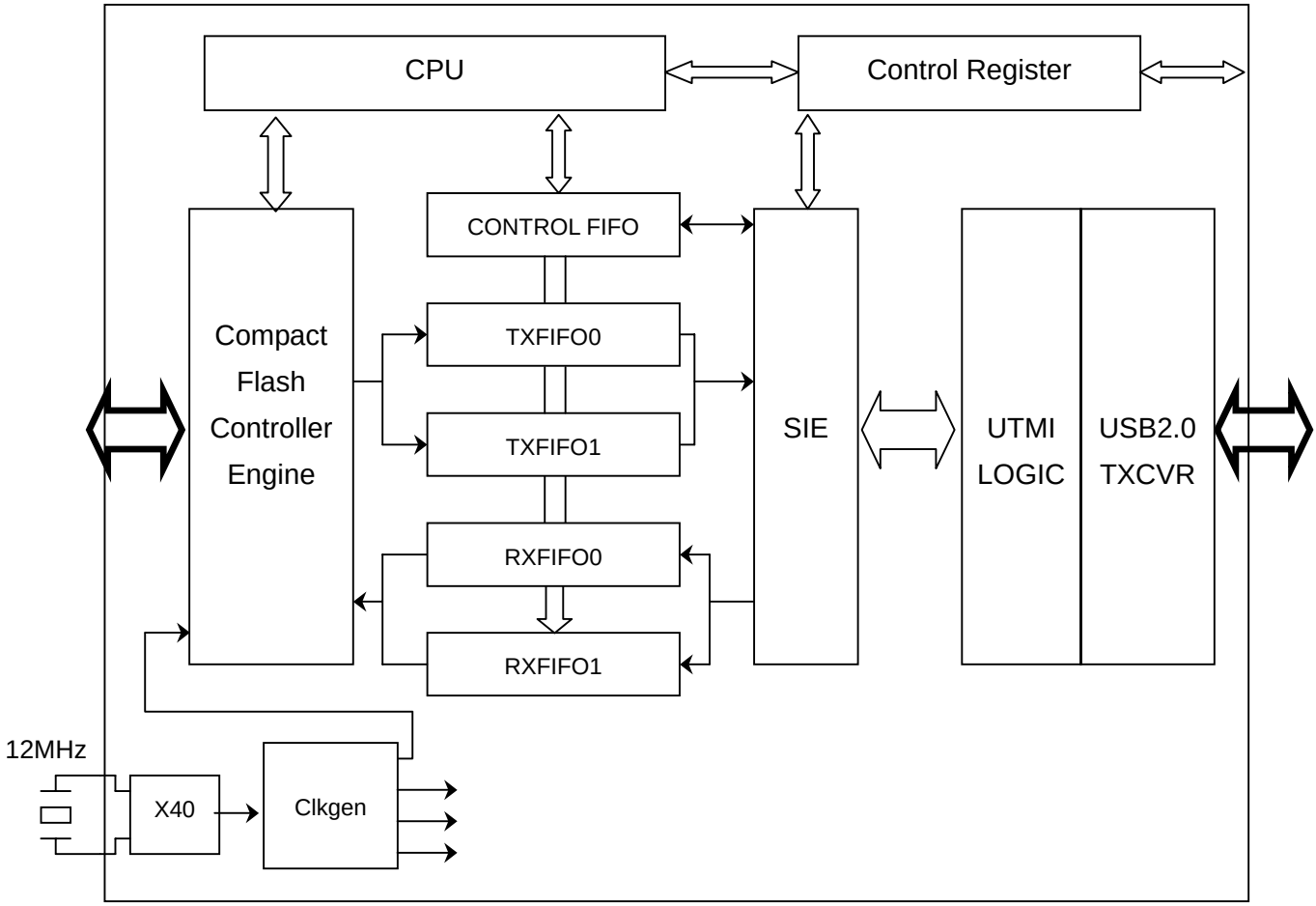
# 3. Function Block

## 3.1 Block Diagram

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## 3.2 Functional Overview

### 3.2.1 USB 2.0 TXCVR

The USB 2.0 Transceiver is the analog circuitry to handle the USB HS/FS signaling.

### 3.2.2 UTMI Logic

The UTMI Logic is compliant to Intel's UTMI specification 1.01. This block handles the low level USB protocol and signaling. The major jobs of UTMI Logic is data and clock recovery, NRZI encoding/decoding, Bit Stuffing/De-stuffing, USB2.0 test modes supporting and serial / parallel conversion.

### 3.2.3 PLL

40XPLL block will provide 480MHz for USB HS data transmission.

### 3.2.4 CLKGEN

CLKGEN is the clock generator block for the logic blocks. It generates 15MHz clock for micro controller, 12MHz for PIO mode, and 30MHz clock for UTMI, SIE, and FIFO.

### 3.2.5 CPU

The CPU is the control center of GL813. It's an 8-bit micro controller operating in 15MHz, 7.5 MIPS. After receiving a USB command, it decodes the host command, then it re-assigns tasks to the CompactFlash controller engine, GPIO, FIFO, and response proper data/ status to USB host.

### 3.2.6 CompactFlash Controller Engine

The CompactFlash controller engine is extended from standard ATA/ ATAPI protocol. It supports PIO mode data transfers.

### 3.2.7 FIFOs

*Control FIFO* is used as Control Read / Write FIFO. *TXFIFO0* / *TXFIFO1* are two sets of 512-byte ping-pong FIFO for Bulk Read endpoint. It buffers data from CompactFlash controller engine, and re-direct to USB SIE logic. *RXFIFO0* / *RXFIFO1* are two sets of 512-byte ping-pong FIFO for Bulk Write endpoint. It buffers data from USB SIE logic, and re-direct to CompactFlash controller engine.

### 3.2.8 Control Registers

Control Register configures GL813 to proper operation. For example, CPU can set register to generate wakeup event, enter suspend, transmits proper USB packet to host.

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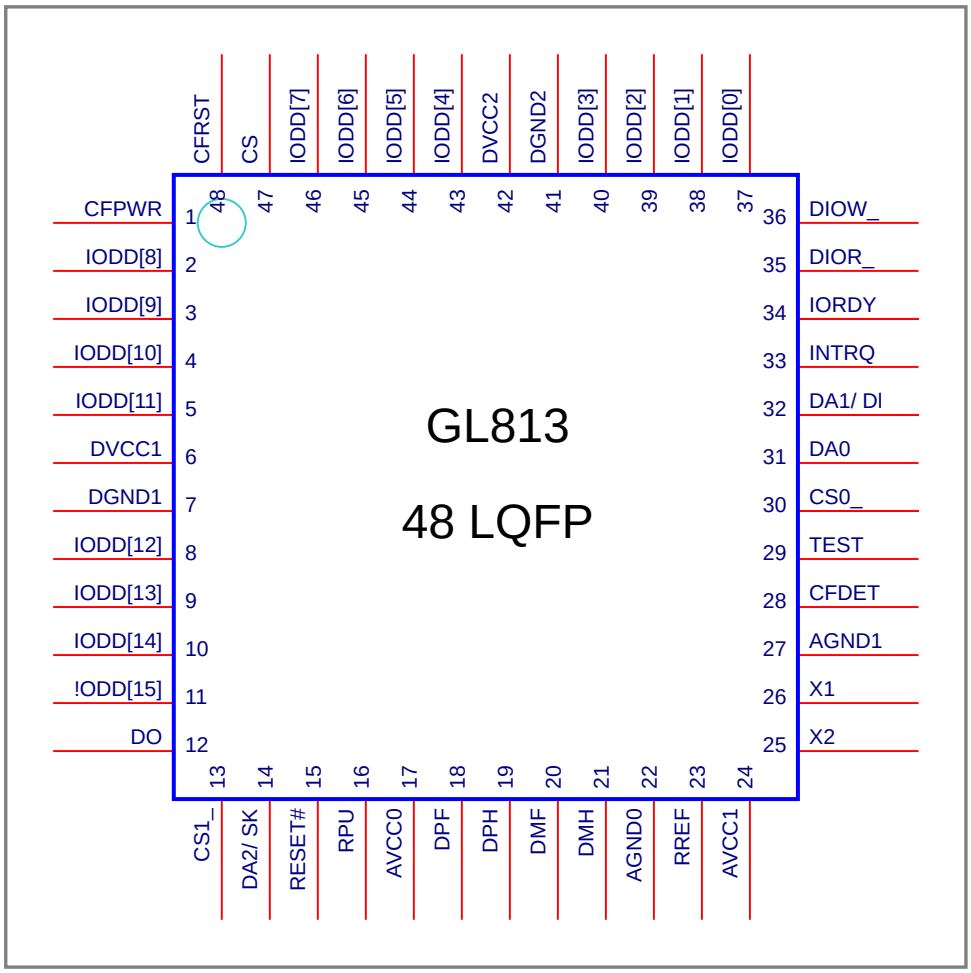
# 4. Pinning Information

## 4.1 48-pin LQFP




| Pin # | Name | I/O | Pad Type | Description |
|---|---|---|---|---|
| 1 | **CFPWR** | B | Tri-state | Compact flash card power control |
| 2~5 | **IODD [8:11]** | I | Tri-state | IDE data bus 8~11 |
| 6 | **DVCC1** | P | Power | Digital VCC |
| 7 | **DGND1** | P | Power | Digital ground |
| 8~11 | **IODD [12:15]** | B | Tri-state | IDE data bus 12~15 |
| 12 | **DO** | I | Tri-state | DO from EEPROM |
| 13 | **CS1_** | O | Tri-state | IDE chip select 1 |

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| Pin # | Name | I/O | Pad Type | Description |
|---|---|---|---|---|
| 14 | **DA2 / SK** | O | Tri-state | IDE address 2 / SK to EEPROM |
| 15 | **RESET#** | I | Pull-high | HW reset |
| 16 | **RPU** | A | U20mia | 3.3v output |
| 17 | **AVCC0** | P | Power | Analog VCC |
| 18 | **DPF** | B | U20mia | Full speed DP |
| 19 | **DPH** | B | U20mia | High speed DP |
| 20 | **DMF** | B | U20mia | Full speed DM |
| 21 | **DMH** | B | U20mia | High speed DM |
| 22 | **AGND0** | P | Power | Analog ground |
| 23 | **RREF** | | U20mia | Reference resister connect (*) |
| 24 | **AVCC1** | P | Power | Analog VCC |
| 25 | **X2** | B | Clock | Crystal output |
| 26 | **X1** | I | Clock | Crystal input, 12Mhz |
| 27 | **AGND1** | P | Power | Analog ground |
| 28 | **CFDET** | I | Tri-state | Compact flash card detect |
| 29 | **TEST** | I | Pull-low | TEST mode input |
| 30 | **CS0_** | O | Tri-state | IDE Chip select 0 |
| 31 | **DA0** | O | Tri-state | IDE address 0 |
| 32 | **DA1 / DI** | O | Tri-state | IDE address 1 / DI to EEPROM |
| 33 | **INTRQ** | I | Tri-state | IDE Interrupt request |
| 34 | **IORDY** | I | Tri-state | IDE IO ready |
| 35 | **DIOR_** | O | Tri-state | IDE read signal |
| 36 | **DIOW_** | O | Tri-state | IDE write signal |
| 37~40 | **IODD [0:3]** | B | Tri-state | IDE data bus 0~3 |
| 41 | **DGND2** | P | Power | Digital ground |
| 42 | **DVCC2** | P | Power | Digital VCC |
| 43~46 | **IODD [4:7]** | B | Tri-state | IDE data bus 4~7 |
| 47 | **CS** | O | Tri-state | CS to EEPROM |
| 48 | **CFRST** | B | Tri-state | Compact Flash Card HW reset |

(*) RREF must be connected with a 510 ohm resister to ground.

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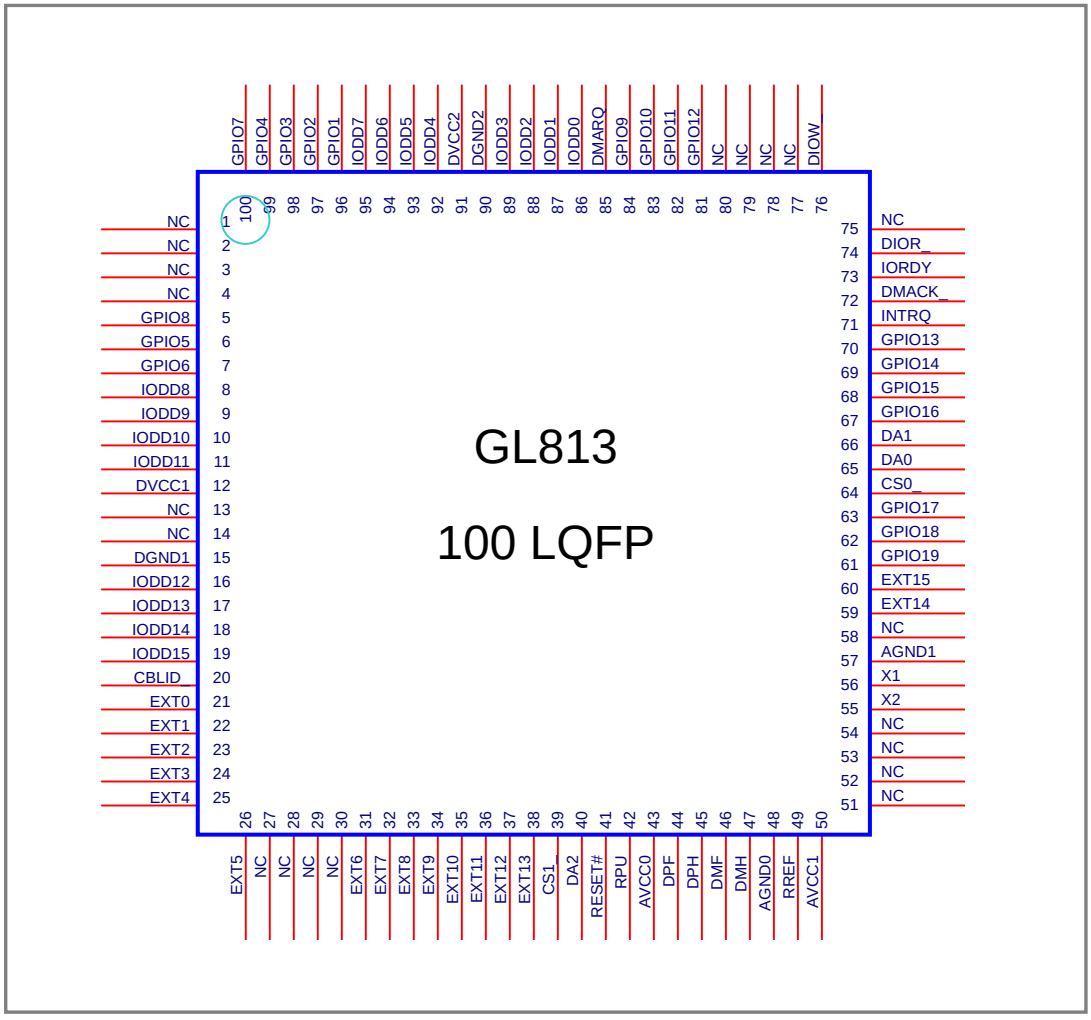
## 4.2 100-pin LQFP

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| Pin # | Name | I/O | Pad Type | Description |
|---|---|---|---|---|
| 1 | **NC** | - | - | - |
| 2 | **NC** | - | - | - |
| 3 | **NC** | - | - | - |
| 4 | **NC** | - | - | - |
| 5 | **GPIO8** | B | Tri-state | GPIO8 (*) |
| 6 | **GPIO5** | B | Tri-state | GPIO5 |
| 7 | **GPIO6** | B | Tri-state | GPIO6 |
| 8~11 | **IODD [8:11]** | B | Tri-state | IDE data bus 8 ~ 11 |
| 12 | **DVCC1** | P | Power | Digital VCC |
| 13 | **NC** | - | - | - |
| 14 | **NC** | - | - | - |
| 15 | **DGND1** | P | Power | Digital ground |
| 16~19 | **IODD [12:15]** | B | Tri-state | IDE data bus 12 ~ 15 |
| 20 | **CBLID_** | I | Tri-state | Cable select input |
| 21 | **NC/ECPURD/EROMD0** | I | Pull-low | NC: Embedded CPU mode<br>ECPURD: Read signal when external CPU mode<br>EROMD0: Data0 when external ROM mode |
| 22 | **NC/ECPUWR/EROMD1** | I | Pull-low | NC: Embedded CPU mode<br>ECPUWR: Write signal when external CPU mode<br>EROMD1: Data1 when external ROM mode |
| 23 | **NC/ECPUA5/EROMD2** | I | Pull-low | NC: Embedded CPU mode<br>ECPUA5: Address5 when external CPU mode<br>EROMD2: Data2 when external ROM mode |
| 24 | **NC/ECPUA4/EROMD3** | I | Pull-low | NC: when embedded CPU mode<br>ECPUA4: Address4 when external CPU mode<br>EROMD3: Data3 when external ROM mode |
| 25 | **NC/ECPUA3/EROMD4** | I | Pull-low | NC: Embedded CPU mode<br>ECPUA3: Address3 when external CPU mode<br>EROMD4: Data4 when external ROM mode |

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| Pin # | Name | I/O | Pad Type | Description |
|---|---|---|---|---|
| 26 | **NC/ECPUA2/EROMD5** | I | Pull-low | NC: Embedded CPU mode<br>ECPUA2: Address2 when external CPU mode<br>EROMD5: Data5 when external ROM mode |
| 27 | **NC** | - | - | - |
| 28 | **NC** | - | - | - |
| 29 | **NC** | - | - | - |
| 30 | **NC** | - | - | - |
| 31 | **NC/ECPUA1/EROMD6** | I | Pull-low | NC: Embedded CPU mode<br>ECPUA1: Address1 when external CPU mode<br>EROMD6: Data6 when external ROM mode |
| 32 | **NC/ECPUA0/EROMD7** | I | Pull-low | NC: Embedded CPU mode<br>ECPUA0: Address0 when external CPU mode<br>EROMD7: Data7 when external ROM mode |
| 33 | **NC/ECPUD7/EROMD8** | B | Pull-low | NC: Embedded CPU mode<br>ECPUD7: Data7 when external CPU mode<br>EROMD8: Data8 when external ROM mode |
| 34 | **NC/ECPUD6/EROMD9** | B | Pull-low | NC: Embedded CPU mode<br>ECPUD6: Data6 when external CPU mode<br>EROMD9: Data9 when external ROM mode |
| 35 | **NC/ECPUD5/EROMD10** | B | Pull-low | NC: Embedded CPU mode<br>ECPUD5: Data5 when external CPU mode<br>EROMD10: Data10 when external ROM mode |
| 36 | **NC/ECPUD4/EROMD11** | B | Pull-low | NC: Embedded CPU mode<br>ECPUD4: Data4 when external CPU mode<br>EROMD11: Data11 when external ROM mode |
| 37 | **NC/ECPUD3/EROMD12** | B | Pull-low | NC: Embedded CPU mode<br>ECPUD3: Data3 when external CPU mode<br>EROMD12: Data12 when external ROM mode |

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| Pin # | Name | I/O | Pad Type | Description |
|---|---|---|---|---|
| 38 | **NC/ECPUD2/EROMD13** | B | Pull-low | NC: Embedded CPU mode<br>ECPUD2: Data2 when external CPU mode<br>EROMD13: Data13 when external ROM mode |
| 39 | **CS1_** | O | Tri-state | Chip select 1 |
| 40 | **DA2** | O | Tri-state | IDE address 2 |
| 41 | **RESET#** | I | Pull-high | Reset pin |
| 42 | **RPU** | A | U20mia | 3.3v output |
| 43 | **AVCC0** | P | Power | Analog VCC |
| 44 | **DPF** | B | U20mia | Full speed DP |
| 45 | **DPH** | B | U20mia | High speed DP |
| 46 | **DMF** | B | U20mia | Full speed DM |
| 47 | **DMH** | B | U20mia | High speed DM |
| 48 | **AGND0** | P | Power | Analog ground |
| 49 | **RREF** | | U20mia | Reference resister connect (*) |
| 50 | **AVCC1** | P | Power | Analog VCC |
| 51 | **NC** | - | - | - |
| 52 | **NC** | - | - | - |
| 53 | **NC** | - | - | - |
| 54 | **NC** | - | - | - |
| 55 | **X2** | B | Clock | Crystal output |
| 56 | **X1** | I | Clock | Crystal input, 12Mhz |
| 57 | **AGND1** | P | Power | Analog ground |
| 58 | **NC** | - | - | - |
| 59 | **NC/ECPUD1/EROMA0** | B | Pull-low | NC: Embedded CPU mode<br>ECPUD1: Data1 when external CPU mode<br>EROMA0: Address0 when external ROM mode |
| 60 | **NC/ECPUD0/EROMA1** | B | Pull-low | NC: Embedded CPU mode<br>ECPUD0: Data0 when external CPU mode<br>EROMA1: Address1 when external ROM mode |
| 61 | **GPIO19** | B | Pull-low | GPIO19 |
| 62 | **GPIO18/GPIO18/EROMA11** | B | Pull-low | GPIO18: for embedded or external CPU mode<br>EROMA11: Address11 when external ROM mode |

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| Pin # | Name | I/O | Pad Type | Description |
|---|---|---|---|---|
| 63 | **GPIO17/GPIO17/EROM A10** | B | Pull-low | GPIO17: For embedded or external CPU mode<br>EROMA10: Address10 when external ROM mode |
| 64 | **CS0_** | O | Tri-state | Chip select 0 |
| 65 | **DA0** | O | Tri-state | IDE address 0 |
| 66 | **DA1** | O | Tri-state | IDE address 1 |
| 67 | **GPIO16/GPIO16/EROM A9** | B | Pull-low | GPIO16: For embedded or external CPU mode<br>EROMA9: Address9 when external ROM mode |
| 68 | **GPIO15/GPIO15/EROM A8** | B | Pull-low | GPIO15: For embedded or external CPU mode<br>EROMA8: Address8 when external ROM mode |
| 69 | **GPIO14/GPIO15/EROM A7** | B | Pull-low | GPIO14: For embedded or external CPU mode<br>EROMA7: Address7 when external ROM mode |
| 70 | **GPIO13/GPIO14/EROM A6** | B | Pull-low | GPIO13: For embedded or external CPU mode<br>EROMA6: Address6 when external ROM mode |
| 71 | **INTRQ** | I | Tri-state | IDE interrupt input |
| 72 | **DMACK_** | O | Tri-state | IDE acknowledge |
| 73 | **IORDY** | I | Pull-high | IDE ready |
| 74 | **DIOR_** | O | Tri-state | IDE read signal |
| 75 | **NC** | - | - | - |
| 76 | **DIOW_** | O | Tri-state | IDE write signal |
| 77 | **NC** | - | - | - |
| 78 | **NC** | - | - | - |
| 79 | **NC** | - | - | - |
| 80 | **NC** | - | - | - |
| 81 | **GPIO12/GPIO13/EROM A5** | B | Pull-low | GPIO12: For embedded or external CPU mode<br>EROMA5: Address5 when external ROM mode |
| 82 | **GPIO11/GPIO12/EROM A4** | B | Pull-low | GPIO11: For embedded or external CPU mode<br>EROMA4: Address4 when external ROM mode |

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| Pin # | Name | I/O | Pad Type | Description |
|---|---|---|---|---|
| 83 | **GPIO10/GPIO10/EROMA3** | B | Pull-low | GPIO10: For embedded or external CPU mode<br>EROMA3: Address3 when external ROM mode |
| 84 | **GPIO9/GPIO9/EROMA2** | B | Pull-low | GPIO9: For embedded or external CPU mode<br>EROMA2: Address2 when external ROM mode |
| 85 | **DMARQ** | I | Pull-low | IDE request |
| 86~89 | **IDEDD [0:3]** | B | Tri-state | IDE data bus 0~3 |
| 90 | **DGND2** | P | Power | Digital ground |
| 91 | **DVCC2** | P | Power | Digital VCC |
| 92~95 | **IDEDD [4:7]** | B | Tri-state | IDE data bus 4~7 |
| 96 | **GPIO1** | B | Pull-high | GPIO1 |
| 97 | **GPIO2** | B | Pull-high | GPIO2 |
| 98 | **GPIO3** | B | Pull-high | GPIO3 |
| 99 | **GPIO4** | B | Pull-low | GPIO4 |
| 100 | **GPIO7** | B | Pull-low | GPIO 7 (*) |

(*) When operating in default mode: GPIO7 is the IDE reset input, GPIO8 is used to control the power input of IDE device.

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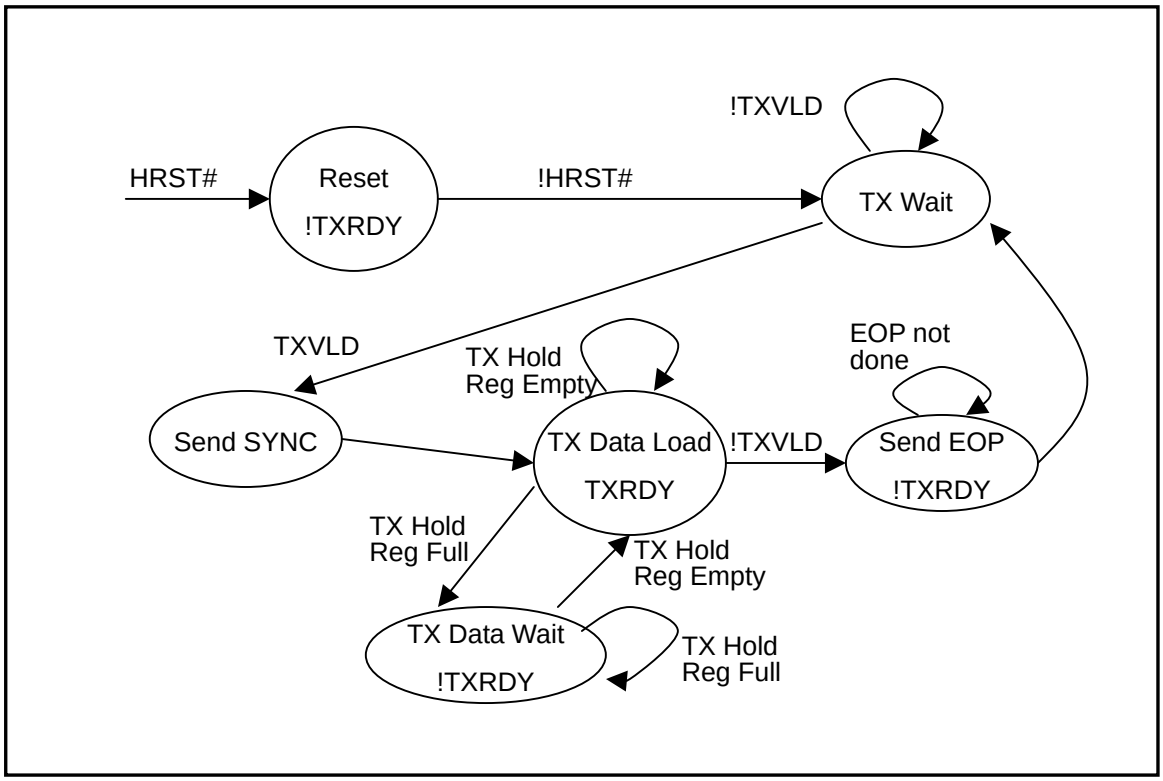
# 5. Functional Description

## 5.1 Transmit Operation

### 5.1.1 Transmit State Diagram




- Transmit must be asserted to enable any transmissions.
- The SIE asserts TXVLD to begin a transmission.
- The SIE negates TXVLD to end a transmission.
- After the SIE asserts TXVLD it can assume that the transmission has started when it detects TXRDY asserted.
- The SIE assumes that the UTM has consumed a data byte if TXRDY and TXVLD are asserted.
- The SIE must have valid packet information (PID) asserted on the Data bus coincident with the assertion of TXVLD. Depending on the UTM implementation, TXRDY may be asserted by the Transmit State Machine as soon as one CLK after the assertion of TXVLD.
- TXVLD and TXRDY are sampled on the rising edge of CLKOUT.
- The Transmit State Machine does not automatically generate Packet ID's (PIDs) or

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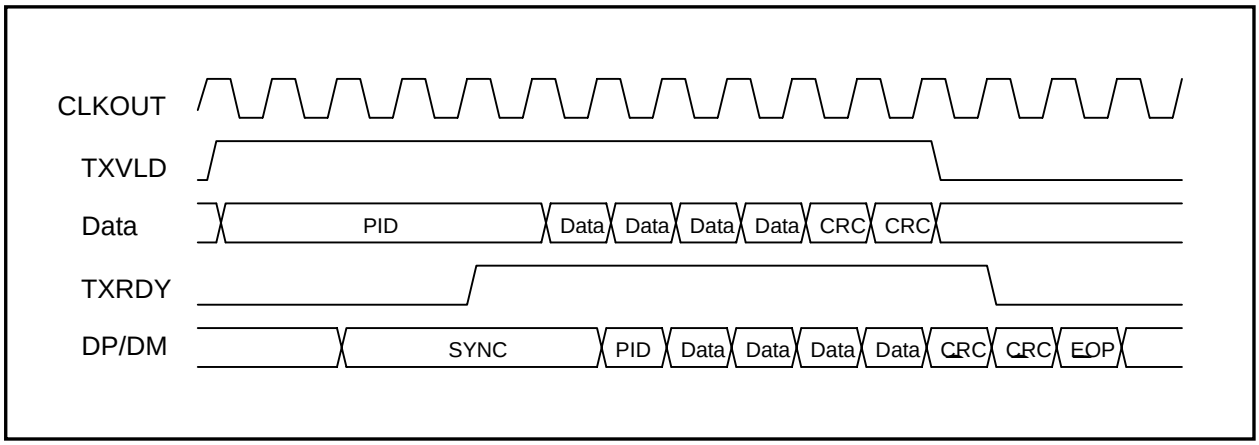
CRC. When transmitting, the SIE is always expected to present a PID as the first byte of the data stream and if appropriate, CRC as the last bytes of the data stream.

- The SIE must use LINEST0/1 to verify a Bus Idle condition before asserting TXVLD in the TX Wait state.

### 5.1.2 Transmit Timing for Data Packet




The SIE negates TXVLD to complete a packet. Once negated, the Transmit State Machine will never reassert TXRDY until after the EOP has been loaded into the Transmit Shift Register. Note that the UTM Transmit State Machine can be ready to start another package immediately, however the SIE must confirm to the minimum inter-packet delays identified in the USB 2.0 Specification.

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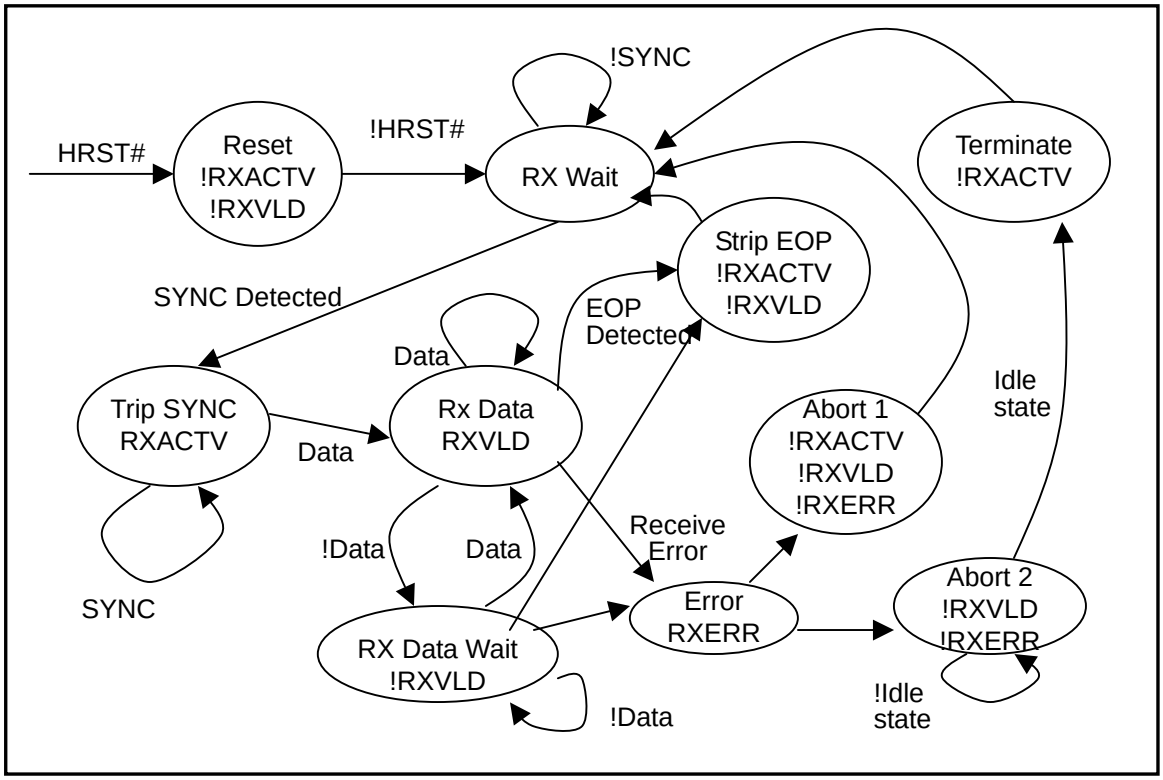
## 5.2 Receive Operation

### 5.2.1 Receive State Diagram




- RXACTV and RXVLD are sampled on the rising edge of CLKOUT.
- In the RX Wait state the receiver is always looking for SYNC.
- The Macrocell asserts RXACTV when SYNC is detected (Strip SYNC state).
- The Macrocell negates RXACTV when an EOP is detected (Strip EOP state).
- When RXACTV is asserted, RXVLD will be asserted if the RX Holding Register is full.
- RXVLD will be negated if the RX Holding Register was not loaded during the previous byte time. This will occur if 8 stuffed bits have been accumulated.
- The SIE must be ready to consume a data byte if RXACTV and RXVLD are asserted (RX Data state).
- In FS mode, if a bit stuff error is detected then the Receive State Machine will negate RXACTV and RXVLD, and return to the RXWait state.

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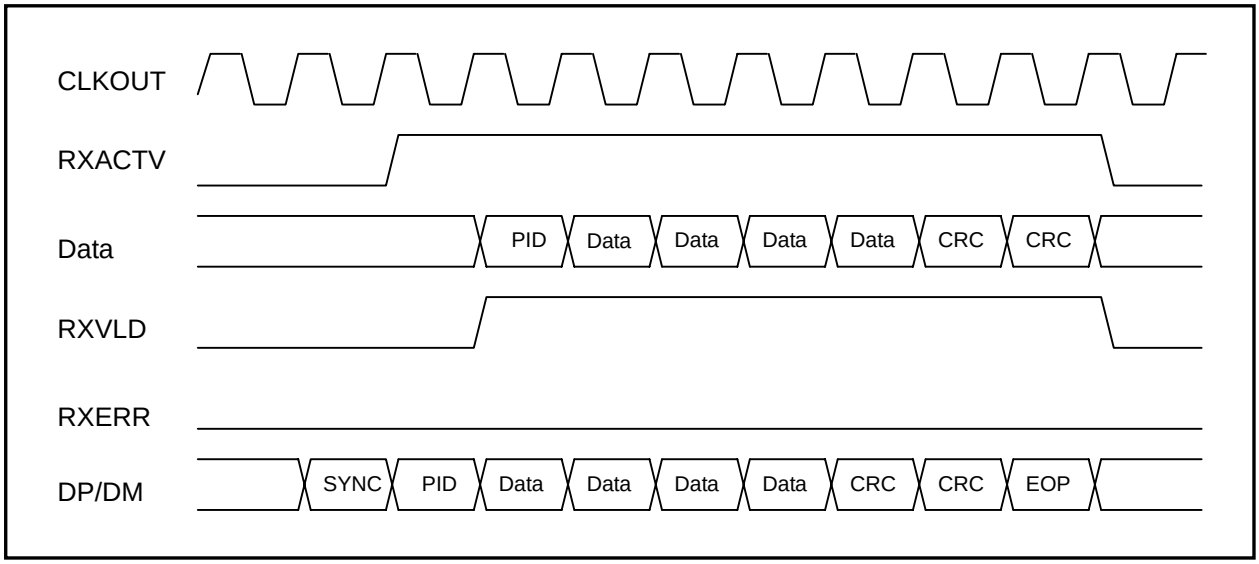
### 5.2.2 Receive Timing for Data Packet (with CRC-16)




Note that the USB 2.0 transceiver does not decode Packet ID's (PIDs). They are passed to the SIE for decoding.

This timing example is in HS mode. When a HS/FS UTM is in FS mode there are approximately 40 clock cycles every byte time. The Receive State Machine assumes that the SIE captures the data on the data bus if RXACTV and RXVLD are asserted. In FS mode, RXVLD will only be asserted for one clock per byte time.

Note that the receive and transmit sections of the transceiver operate independently. The receiver will receive any packets on the USB. The transceiver does not identify whether the packet that it is receiving from the upstream or the downstream port. The SIE must ignore receive data while it is transmitting.

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# 6. Electrical Characteristics

## 6.1 Absolute Maximum Ratings

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | -0.3 | +3.6 | V |
| $V_I$ | DC input voltage | -0.3 | $V_{CC}$ + 0.3 | V |
| $V_{I/O}$ | DC input voltage range for I/O | -0.3 | $V_{CC}$ + 0.3 | V |
| $V_{AI/O}$ | DC input voltage for USB D+/D- pins | -0.3 | $V_{CC}$ + 0.3 | V |
| $V_{I/OZ}$ | DC voltage applied to outputs in High Z state | -0.3 | $V_{CC}$ + 0.3 | V |
| $V_{ESD}$ | Static discharge voltage | 4000 | | V |
| $T_A$ | Ambient Temperature | 0 | 100 | $^oC$ |

## 6.2 Recommended Operating Conditions

| Item | Value |
|---|---|
| Supply Voltage | +3.3V to + 3.6V |
| Ground Voltage | 0V |
| $F_{osc}$ | 12 MHz ± 100 ppm |
| Operating Temperature | 0 $^oC$ ~ 70 $^oC$ |

## 6.3 DC Characteristics (Digital Pins)

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $P_D$ | Power Dissipation | | | | mA |
| $V_{DD}$ | Power Supply Voltage | 3 | 3.3 | 3.6 | V |
| $I_O$ | DC output sink current excluding D+/ D-/ VCC/ GND | 8 | | | mA |
| $V_{IL}$ | LOW level input voltage | | | 0.9 | V |
| $V_{IH}$ | HIGH level input voltage | 2.0 | | | V |
| $V_{TLH}$ | LOW to HIGH threshold voltage | 1.3 | 1.43 | 1.56 | V |
| $V_{THL}$ | HIGH to LOW threshold voltage | 1.3 | 1.43 | 1.56 | V |

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| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{HYS}$ | Hysteresis voltage | - | 0 | - | V |
| $V_{OL}$ | LOW level output voltage when $I_{OL}$=8mA | | | 0.4 | V |
| $V_{OH}$ | HIGH level output voltage when $I_{OH}$=8mA | 2.4 | | | V |
| $I_{OLK}$ | Leakage current for pads with internal pull up or pull down resistor | | | 46 | μA |
| $R_{DN}$ | Pad internal pull down resister | 79K | 105K | 152K | Ohms |
| $R_{UP}$ | Pad internal pull up resister | 78K | 104K | 146K | Ohms |

## 6.4 DC Characteristics (D+/D-)

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | D+/D- static output LOW ($R_L$ of 1.5K to 3.6V ) | | | 0.3 | V |
| $V_{OH}$ | D+/D- static output HIGH ($R_L$ of 15K to GND ) | 2.8 | | 3.6 | V |
| $V_{DI}$ | Differential input sensitivity | 0.2 | | | V |
| $V_{CM}$ | Differential common mode range | 0.8 | | 2.5 | V |
| $V_{SE}$ | Single-ended receiver threshold | 0.2 | | | V |
| $C_{IN}$ | Transceiver capacitance | | | 20 | pF |
| $I_{LO}$ | Hi-Z state data line leakage | -10 | | +10 | μA |
| $Z_{DRV}$ | Driver output resistance | 28 | | 43 | Ohms |

## 6.5 Switching Characteristics

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{X1}$ | X1 crystal frequency | 11.97 | 12 | 12.03 | MHz |
| $T_{CYC}$ | X1 cycle time | | 83.3 | | ns |
| $T_{X1L}$ | X1 clock LOW time | $0.45T_{cyc}$ | | | ns |
| $T_{X1H}$ | X1 clock HIGH time | $0.45T_{cyc}$ | | | ns |
| $T_{r30pf}$ | Output pad rise time from 10% to 90% swing with 30pF loading | | | | ns |
| $T_{f30pf}$ | Output pad fall time from 10% to 90% swing with 30pF loading | | | | ns |

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| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{r50pf}$ | Output pad rise time from 10% to 90% swing with 50pF loading | | | | ns |
| $T_{f50pf}$ | Output pad fall time from 10% to 90% swing with 50pF loading | | | | ns |
| $T_{rUSB}$ | D+/D- rise time with 50pF loading | 4 | | 20 | ns |
| $T_{fUSB}$ | D+/D- fall time with 50pF loading | 4 | | 20 | ns |

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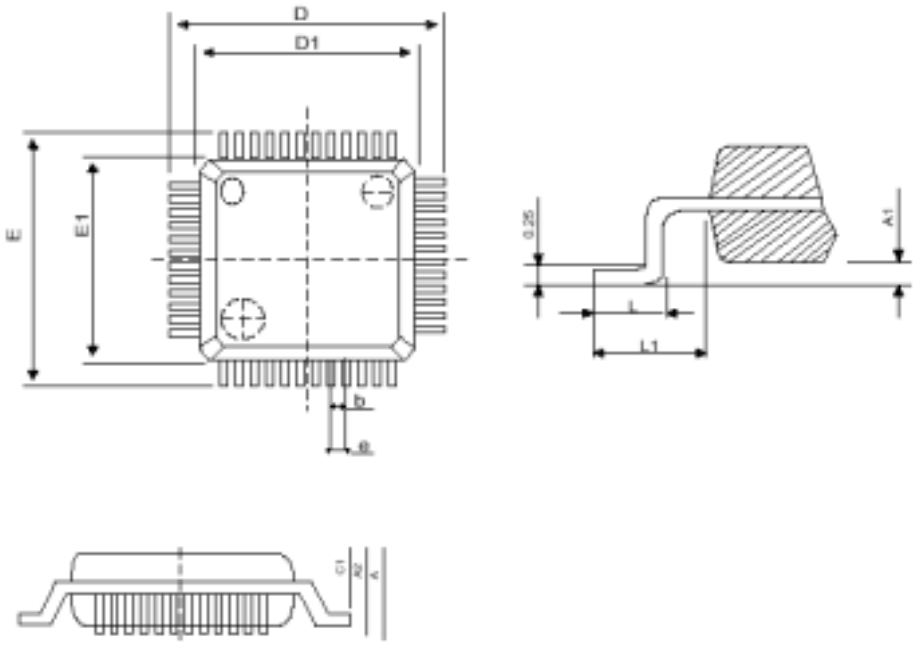
# 7. Package Dimension

## 7.1 48-pin LQFP




| SYMBOL | MIN | MAX |
|---|---|---|
| A | | 1.6 |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| C1 | 0.09 | 0.16 |
| D | 9.00BSC | |
| D1 | 7.00BSC | |
| E | 9.00BSC | |
| E1 | 7.00BSC | |
| e | 0.5BSC | |
| b | 0.17 | 0.27 |
| L | 0.45 | 0.75 |
| L1 | 1 REF | |

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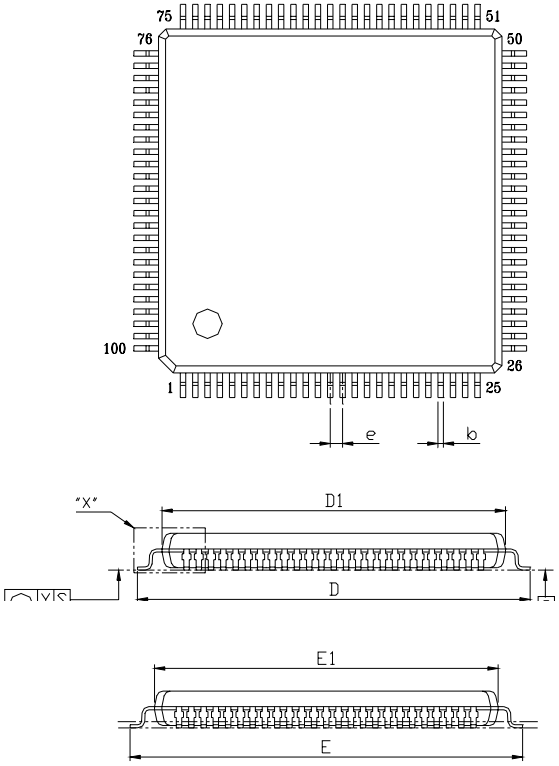
## 7.2 100-pin LQFP




| SYMBOL | DIMENSION (MM) | | | DIMENSION (MIL) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.60 | | | 63 |
| A1 | 0.05 | | 0.15 | 2 | | 6 |
| A2 | 1.35 | 1.40 | 1.45 | 53 | 55 | 57 |
| b | 0.17 | 0.22 | 0.27 | 7 | 9 | 11 |
| b1 | 0.17 | 0.20 | 0.23 | 7 | 8 | 9 |
| c | 0.09 | | 0.20 | 4 | | 8 |
| c1 | 0.09 | | 0.16 | 4 | | 6 |
| D | 16.00 BSC | | | 630 BSC | | |
| D1 | 14.00 BSC | | | 551 BSC | | |
| E | 16.00 BSC | | | 630 BSC | | |
| E1 | 14.00 BSC | | | 551 BSC | | |
| e | 0.50 BSC | | | 20 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 18 | 24 | 30 |
| L1 | 1.00 REF | | | 39 REF | | |
| R1 | 0.08 | | | 3 | | |
| R2 | 0.08 | | 0.20 | 3 | | 8 |
| Y | | | 0.075 | | | 3 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | | | 0° | | |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| s | 0.20 | | | 8 | | |

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# 8. Revision History

| Version | Description | Date |
|---|---|---|
| 1.0 | First draft | 2002/03/20 |
| 1.1 | Correction and supplement of Electrical Characteristics data | 2002/04/03 |
| 1.2 | Add 100-pin LQFP package related data | 2002/04/12 |

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