PRELIMINARY DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8139GR-7JH

Single Chip Transceiver Silicon MMIC for PHS

DESCRIPTION

The μPC8139GR-7JH is a silicon microwave monolithic IC (SiMMIC) developed as a transceiver for Personal Handyphone System (PHS).

This IC is a highly integrated single chip, suitable for PHS, including a quadrature modulator, up converter, and AGC circuit for adjusting the output level in the transmitter block, a 2nd down converter and RSSI circuit in the receiver block, and a transistor for 2nd VCO.

This low power IC employs NEC's proprietary bipolar process NESAT™ IV (f_T = 20 GHz) and also has a built-in power save function, which contributes to lowering power consumption of the RF block.

This IC is packaged in a small, thin 30 pin plastic TSSOP (225 mil).

FEATURES

- Low voltage operation, low current consumption
  V_{CC} = 2.7 to 4.0 V, I_{CC} = 32.5 mA at transmitter, I_{CC} = 4.8 mA at receiver, 3.2 mA/@V_{CC} = 3 V at 2nd VCO block
- LPF is installed to suppress leakage of transmitter's local (L01) harmonics.
  Spurious within transmission band (LO1 × 7, 8): –55 dBc (MAX.)
- On-chip AGC circuit for adjusting the output level: GCR = 20 dB (MIN.) /@f_{RFout} = 1906.55 MHz
- High-performance
  Output level: P_{RFout} = –13 dBm (TYP.) /@f_{RFout} = 1906.55 MHz, $V_{I/Q}$ = 500 mV_{P-P} (Differential phase)
  Error vector magnitude: EVM = 1.0% rms (TYP.)
  Adjacent channel leak power: P_{adj} = –68 dBc (TYP.) /@Δf = ±600 kHz
  RSSI output dynamic range: 83 dB
- CR phase shifter is adopted.

APPLICATION

- Digital cordless telephone: PHS
- PHS application equipment: PDA, PC card, etc.

ORDERING INFORMATION

Part Number	Package	Supplying Form
μPC8139GR-7JH-E1	30-pin plastic TSSOP (225 mil)	Embossed tape 16 mm-wide. Pin 1 is in pull-out direction. 2.5 kp/reel

Remark To order evaluation samples, contact your local NEC sales office. (Part Number for sample order: μPC8139GR-7JH)

Caution This product is an electrostatic sensitive device.

The information in this document is subject to change without notice.

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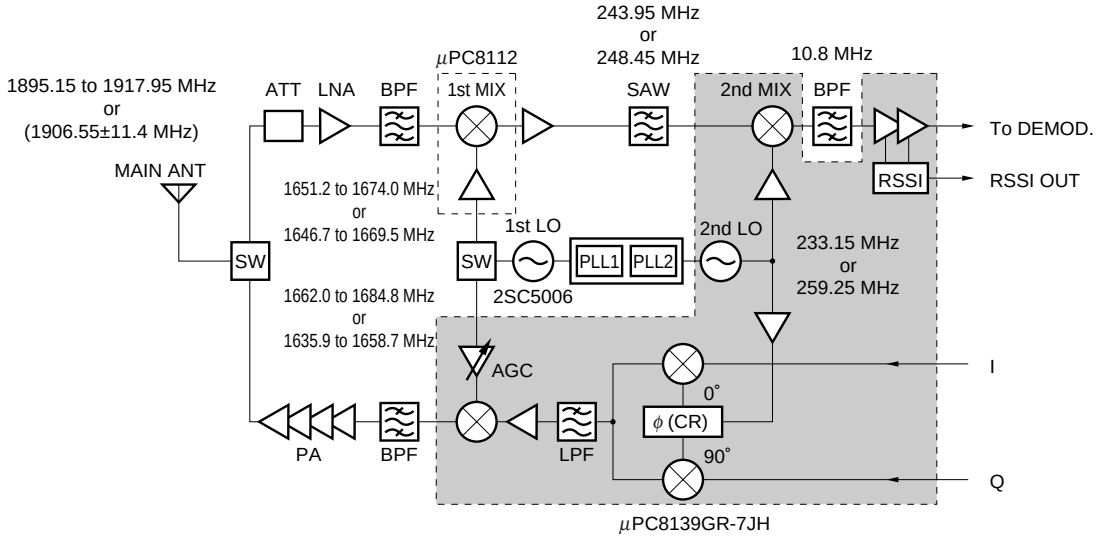
SYSTEM APPLICATION EXAMPLE

[PHS]

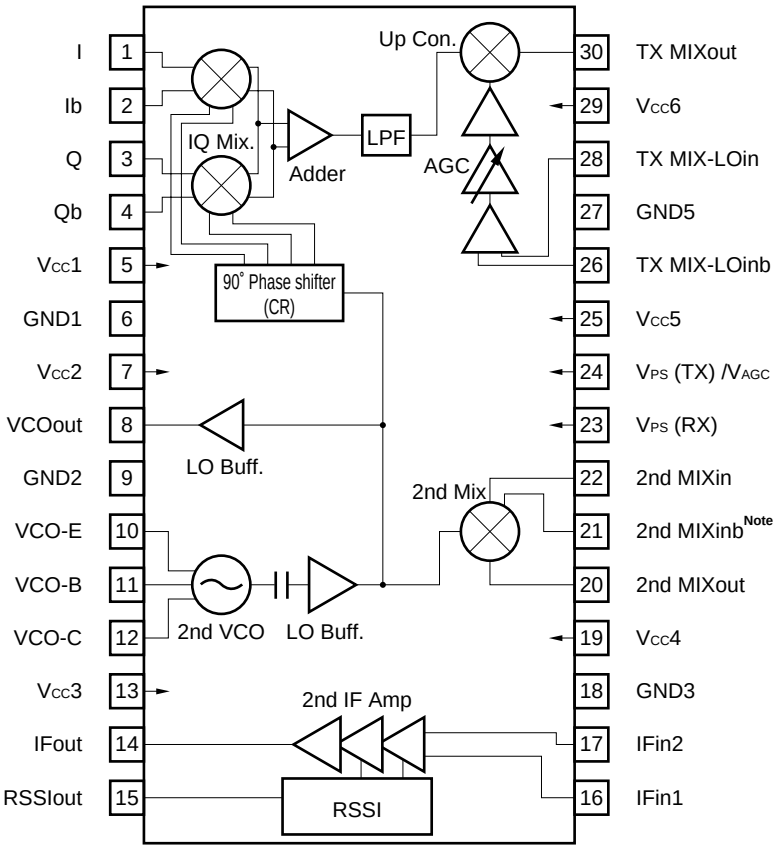


QUADRATURE MODULATOR IC SERIES PRODUCT LIST

Part Number	Function	I_{CC} (mA)	f_{LO1in} (MHz)	f_{MODout} (MHz)	Up Converter f_{RFout} (MHz)	Phase Shifter Type	Application Field	Package
μPC8101GR	150-MHz quadrature modulator	15 /@2.7 V	100 to 300	50 to 150	External	F/F	CT-2, etc.	20 pin SSOP (225 mil)
μPC8104GR	RF up converter + IF quadrature modulator	28 /@3.0 V	100 to 400		900 to 1900	Multiplier + F/F	Various digital communica-tions	
μPC8105GR	400-MHz quadrature modulator	16 /@3.0 V	100 to 400		External	Multiplier + F/F	Various digital communica-tions	16 pin SSOP (225 mil)
μPC8110GR	1-GHz direct quadrature modulator	24 /@3.0 V	800 to 1000		Direct modulation	Multiplier + F/F	PDC800 MHz, etc.	20 pin SSOP (225 mil)
μPC8125GR	On-chip AGC function RF up converter + IF quadrature modulator	36 /@3.0 V	220 to 270		1800 to 2000	Multiplier + F/F	PHS	
μPC8126GR	On-chip local PreMIX 1-GHz direct quadrature modulator	35 /@3.0 V	915 to 960		Direct modulation	Multiplier + F/F	PDC800 MHz, etc.	
μPC8126K								28 pin QFN
μPC8129GR	LO × 2 frequency input type IF quadrature modulator + RF up converter	28 /@3.0V	200 to 800	100 to 400	800 to 1900	F/F	GSM, DCS1800, etc.	20 pin SSOP (225 mil)
μPC8158K	On-chip AGC function RF up converter + IF quadrature modulator	28 /@3.0 V	100 to 300		800 to 1500	CR	PDC800 M/1.5 G	28 pin QFN

For an outline of the quadrature modulator IC series, see the application note “Usage of μPC8101, 8104, 8105, 8125, and 8129” (document number P13251E).

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS (Top View)



Note Pin 21 was specified to function as the GND4 in the initial design sample, however in subsequent design samples and commercial products it functions as the 2nd MIXinb.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{CC}	Pins 5, 7, 12, 13, 19, 25, 29, 30 T_A = +25°C	4.5	V
Power save pin voltage	V_{PS}	Pin 23, Pin 24, T_A = +25°C	4.5	V
Power dissipation	P_D	T_A = +80°C Note	TBD	mW
Operating ambient temperature	T_A		–30 to +80	°C
Storage temperature	T_{stg}		–55 to +150	°C
Pin current of Pin 8	$I_{8\ pin}$		4	mA
Pin current of Pin 10	$I_{10\ pin}$		4	mA
Collector to base voltage in VCO	V_{CBO}	Pin 12 → Pin 11	4.5	V
Collector to emitter voltage in VCO	V_{CEO}	Pin 12 → Pin 10	4.5	V
Emitter to base voltage in VCO	V_{EBO}	Pin 10 → Pin 11	3.0	V

Note When mounted on 50 × 50 × 1.6 mm double sided copper clad epoxy glass board

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{CC}	Pins 5, 7, 12, 13, 19, 25, 29, 30	2.7	3.0	4.0	V
Power save pin voltage	V_{PS}	Pin 23, Pin 24	0	–	V_{CC}	V
Operating ambient temperature	T_A		–30	+25	+80	°C
TX up converter output frequency	$f_{TX\ •\ MIXout}$		1800	–	2000	MHz
TX up converter LO input frequency	$f_{TX\ •\ MIX\text{-}LOin}$	$P_{TX\ •\ MIX\text{-}LOin}$ = –10 dBm	1500	–	1800	MHz
TX up converter input frequency	$f_{TX\ •\ MIXin}$		220	–	270	MHz
IQ-MOD output frequency	f_{MODout}					
2nd VCO oscillating frequency (IQ-MOD LO, 2nd MIX LO input frequency)	f_{2ndVCO} ($f_{MOD\ •\ LOin}$, $f_{2ndMIX\text{-}LOin}$)					
2nd MIX input frequency	$f_{2ndMIXin}$					
2nd MIX output frequency	$f_{2ndMIXout}$		8	10.8	12	MHz
2nd IF amplifier input frequency	$f_{2ndIFin}$		8	10.8	12	MHz
2nd IF amplifier output frequency	$f_{2ndIFout}$					
I/Q input frequency	$f_{I/Qin}$	$V_{I/Qin}$ = 600 $mV_{P\text{-}P}$ (MAX.), Double phase	DC	–	10	MHz
TX up converter LO input level	$P_{TX\ •\ MIX\text{-}LOin}$		–15	–10	–5	dBm
2nd MIX input level	$P_{2ndMIXin}$		–90	–	–10	dBm
2nd IF amplifier input level	$P_{2ndIFin}$		23	–	108	dBμ VEMF
I/Q input amplitude	$V_{I/Qin}$	Double phase input I/Q (DC) = Ib/Qb (DC) = V_{CC}/2	–	500	600	$mV_{P\text{-}P}$

ELECTRICAL SPECIFICATIONS (1)

T_A = +25°C, V_{CC} = 3.0 V, unless otherwise specified, V_{PS-TX}/V_{AGC} = 3.0 V, V_{PS-RX} = 3.0 V (high), I/Q (DC) = Ib/Qb (DC) = $V_{CC}/2$ = 1.5 V, $V_{I/Qin}$ = 500 mV_{P-P} (double phase input) , $f_{I/Qin}$ = 24 kHz, $\pi/4$DQPSK modulated wave input Transmission rate: 384 kbps, Filter roll-off rate : α = 0.5, MOD pattern: all zero, $f_{MOD \cdot LOin}$ = 233.15 MHz, $P_{MODLOin}$ = –7 dBm, $f_{TX \cdot MIX-LOin}$ = 1673.4 MHz, $P_{TX \cdot MIX-LOin}$ = –10 dBm, $f_{TX \cdot MIXout}$ = 1906.55 MHz + $f_{I/Qin}$

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Total characteristics							
Total circuit current (TX + RX + VCO)		$I_{CC\ (TOTAL)}$	No signal input	33	40.5	49	mA
Transmitter block total characteristics (quadrature modulator + up converter + AGC circuit)							
Total circuit current (TX)		$I_{CC\ (TX-TOTAL)}$	No signal input	27	32.5	39.5	mA
Dark current at power save (TX)		$I_{CC\ (PS)\ TX-TOTAL}$	$V_{PS} \leq$ 0.5 V (Low), No signal input	–	0.1	5	μA
Transmitter block (quadrature modulator + up converter + AGC circuit)							
Total output level		$P_{TX \cdot MIXout}$	V_{AGC} = 3.0 V	–17	–13	–	dBm
Local carrier leak		LOL	$f_{MODin \cdot LOin} + f_{TX \cdot MIX-LOin}$	–	–40	–30	dBc
Image rejection (side-band leak)		ImR		–	–40	–30	dBc
I/Q 3rd order inter-modulation distortion		$IM_{3\ (I/Q)}$		–	–50	–30	dBc
AGC circuit gain control range		GCR	V_{AGC} = 3 V → 1 V	20	35	–	dB
Error vector magnitude (vector error)		EVM	MOD pattern: PN 9	–	1.0	5	%rms
Adjacent channel leak power		P_{adj}	Δf = ±600 kHz, MOD pattern: PN 9	–	–68	–60	dBc
Spurious within transmission band 1		Pout (7 MOD• LO)	$f_{MOD \cdot LOin}$ = 259.25 MHz $f_{MOD \cdot LOin} \times 7$, $f_{MOD \cdot LOin} \times 7$ (Image)	–	–65	–55	dBc
Spurious within transmission band 2		Pout (8 MOD• LO)	$f_{MOD \cdot LOin}$ = 233.15 MHz $f_{MOD \cdot LOin} \times 8$, $f_{MOD \cdot LOin} \times 8$ (Image)	–	–65	–55	dBc
Power saving response time	Rise time	$T_{PS-TX\ (Rise)}$	V_{PS-TX} = 0 V → 3 V	–	2	5	μs
	Fall time	$T_{PS-TX\ (Fall)}$	V_{PS-TX} = 3 V → 0 V	–	2	5	μs
I/Q input impedance		$Z_{I/Q}$	Value between Pins I/Ib and Q/Qb	–	180	–	kΩ
I/Q input bias current		$I_{I/Q}$	Value of each pin when $V_I = V_{Ib} = V_Q = V_{Qb}$	3.5	7	16	μA
Power save low Note 1		$V_{PS-TX\ (Low)}$		0	–	0.5	V
Power save high Note 2		$V_{PS-TX\ (High)}$		0.9	–	V_{CC}	V

Notes 1. Power save pin applied voltage in sleep mode

2. Power save pin applied voltage in active mode

ELECTRICAL SPECIFICATIONS (2)

T_A = +25°C, V_{CC} = 3.0 V, unless otherwise specified, V_{PS} = 3.0 V (high), $f_{2ndMIXin}$ = 243.95 MHz, $P_{2ndMIXin}$ = –40 dBm, $f_{2ndMIX\text{-}LOin}$ = 233.15 MHz, $P_{2ndMIX\text{-}LOin}$ = –7 dBm, $f_{2ndMIXout}$ = 10.8 MHz, $f_{2ndIFin}$ = 10.8 MHz, $P_{2ndIFin}$ = –15 dBm, $f_{2ndIFout}$ = 10.8 MHz

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Receiver block total characteristics							
Total circuit current (RX)		$I_{CC\ (RX\text{-}TOTAL)}$	No signal input	3.5	4.8	6	mA
Dark current at power save		$I_{CC\ (PS\text{-}RX\ TOTAL)}$	$V_{PS\text{-}RX} \leq 0.3$ V (Low), No signal input	–	0.1	5	μA
Power save response time	Rise time	$T_{PS\text{-}RX\ (Rise)}$	$V_{PS\text{-}RX}$ = 0 V → 3 V	–	2	5	μs
	Fall time	$T_{PS\text{-}RX\ (Fall)}$	$V_{PS\text{-}RX}$ = 3 V → 0 V	–	2	5	μs
Power save low [Note 1]		$V_{PS\text{-}RX\ (Low)}$		0	–	0.3	V
Power save high [Note 2]		$V_{PS\text{-}RX\ (High)}$		2.5	–	V_{CC}	V
Receiver block 1 (2nd down converter)							
2nd MIX conversion gain		CG_{2ndMIX}	Combining capacitance with SG	6	10	14	dB
1-dB compression output level		$P_{1dB2ndMIX}$		–	93	–	dBμV
Input 3rd order intercept point		$IIP3_{\ (2ndMIX)}$	$f_{2ndMIXin1}$ = 243.95 MHz, $f_{2ndMIXin2}$ = 244.25 MHz	–	94	–	dBμV
2nd MIX noise figure		NF_{2ndMIX}	At I/O LC matching	–	8	–	dB
2nd MIX local leak 1		$ISL_{\ (2ndLO)1}$	Pin 10 input –7-dBm input [Note 3]	–	52	–	dBμV
2nd MIX local leak 2		$ISL_{\ (2ndLO)2}$	Pin 10 input –7-dBm input [Note 4]	–	24	–	dBμV
2nd MIX output resistance		$Z_{2ndMIXout}$	Pin 20	–	330	–	Ω
Receiver block 2 (IF amplifier)							
Limiting sensitivity		S_L	–3 dB point	–	27	32	dBμVEMF
2nd IF amplifier gain		G_V	$P_{2ndIFin}$ = 13 dBμVEMF	–	80	–	dB
2nd IF amplifier phase shift		S_P	$P_{2ndIFin}$ = 63 to 98 dBμVEMF [Note 5]	–	6	–	deg
2nd IF amplifier output amplitude		V_O	10 kΩ//10 pF [Note 6]	0.5	0.62	0.75	$V_{P\text{-}P}$
2nd IF amplifier output rise time		t_R		–	13	25	ns
2nd IF amplifier output fall time		t_F		–	10	20	ns
2nd IF amplifier input resistance		R_{in}	Pin 16, Pin 17	–	330	–	Ω
2nd IF amplifier input capacitance		C_{in}	Pin 16, Pin 17	–	TBD	–	pF
2nd IF amplifier output duty ratio		V_O (duty)		–	52	–	%
2nd IF amplifier output bias level		V_O (DC)		–	1.5	–	V

Notes 1. Power save pin applied voltage in sleep mode

2. Power save pin applied voltage in active mode

3. Leak to 2nd MIX output pin (Pin 20) of 2nd MIX-LO

4. Leak to 2nd MIX input pin (Pin 22) of 2nd MIX-LO

5. RBW of network analyzer = 3 Hz

6. 10 pF is a value including all capacitance connected to the pins (wiring pattern)

ELECTRICAL SPECIFICATIONS (3)

T_A = +25°C, V_{CC} = 3.0 V, unless otherwise specified, V_{PS} = 3.0 V (high), $f_{2ndMIXin}$ = 243.95 MHz, $P_{2ndMIXin}$ = –40 dBm, $f_{2ndMIX\text{-}LOin}$ = 233.15 MHz, $P_{2ndMIX\text{-}LOin}$ = –7 dBm, $f_{2ndMIXout}$ = 10.8 MHz, $f_{2ndIFin}$ = 10.8 MHz, $P_{2ndIFin}$ = –15 dBm, $P_{2ndIFout}$ = 10.8 MHz

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Receiver block 3 (RSSI)						
RSSI linearity	L_R	V_{IF} = 33 to 98 dBμVEMF	–	±1.5	±2.0	dB
RSSI slope	S_R		–	28	–	mV/dB
RSSI intercept	I_R		–	4	–	dBμVEMF
RSSI output voltage 1	V_{R1}	$V_{2ndIFin}$ = 33 dBμVEMF	0.6	0.8	1	V
RSSI output voltage 2	V_{R2}	$V_{2ndIFin}$ = 63 dBμV	1.44	1.68	1.92	V
RSSI output voltage 3	V_{R3}	$V_{2ndIFin}$ = 98 dBμV	2.4	2.7	2.9	V
RSSI output voltage 4	V_{R4}	No signal input	–	0.5	–	V
RSSI output temperature stability	S_T	T_A = –30°C to +80°C	–	±2.0	–	dB
RSSI output dynamic range	D_R		75	83	–	dB
RSSI rise time	t_{rf1}		–	1	5	μs
RSSI fall time	t_{rf2}		–	1	5	μs
RSSI output ripple	R_R	10 pF[Note]	–	30	–	$mV_{P\text{-}P}$
RSSI output resistance	R_{OR}		28	35	42	kΩ

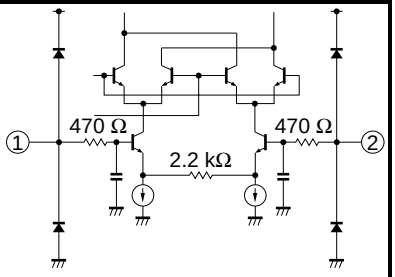
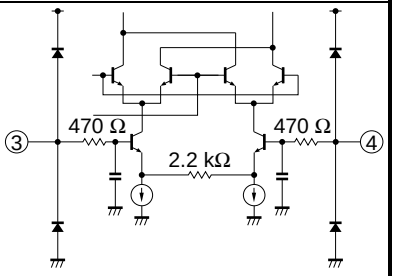
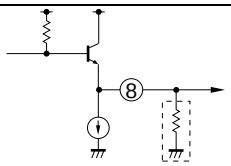
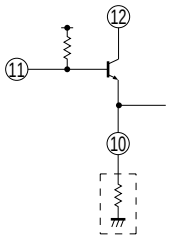
Note 10 pF is a value including all capacitance (wiring capacitance) connected to the pins

ELECTRICAL SPECIFICATIONS (4)

T_A = +25°C, V_{CC} = 3.0 V

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Common block (2nd VCO)						
Total circuit current (2nd VCO)	$I_{CC\ (2ndVCO)}$	3 kΩ is attached to pin 10 externally (without pull-down resistance for pin 8)	2.5	3.2	3.5	mA
2nd VCO output level	P_{2ndVCO}	Pin 8 pull-down resistance is 1 kΩ	–10	–	–	dBm
2nd VCO oscillating frequency	f_{2ndVCO}		220	–	270	MHz

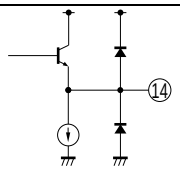
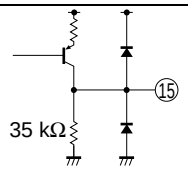
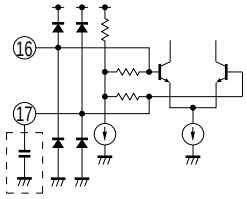
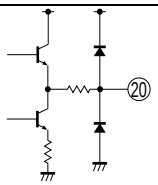
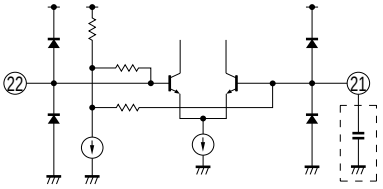
PIN FUNCTIONS

Pin No.	Symbol	Applied Voltage (V)	Pin Voltage Note (V)	Function and Description	Internal Equivalent Circuit
1	I	Vcc/2	–	Input pin for I signal. The input impedance is about 180 kΩ.	
2	Ib	Vcc/2	–	Input pin for Ib signal. The input impedance is about 180 kΩ. Single ended input is also possible. In the case of single ended input, input only the DC voltage of Vcc/2.	
3	Q	Vcc/2	–	Input pin for Q signal. The input impedance is about 180 kΩ.	
4	Qb	Vcc/2	–	Input pin for Qb signal. The input impedance is about 180 kΩ. Single ended input is also possible. In the case of single ended input, input only the DC voltage of Vcc/2.	
5	Vcc1	2.7 to 4.0	–	Power supply voltage pin for the quadrature modulator block.	———
6	GND1	0	–	Ground pin for the quadrature modulator block. Form as wide a ground pattern as possible to minimize its impedance.	———
7	Vcc2	2.7 to 4.0	–	Power supply voltage pin for the VCO block.	———
8	VCOout	–	1.6	Oscillator output pin. The output level can be adjusted with an external pull-down resistor.	
9	GND2	0	–	Ground pin for the VCO block. Form as wide a ground pattern as possible to minimize its impedance.	———
10	VCO_E	–	2.1	Emitter pin for oscillator. Ground with an external pull-down resistor. It can be oscillated by performing feedback with a resonance circuit mounted externally between this pin and Pin 11.	
11	VCO_B	–	2.9	Base pin for oscillator. It can be oscillated by performing feedback with a resonance circuit mounted externally between this pin and Pin 10.	
12	VCO_C	2.7 to 4.0	–	Collector pin for oscillator. Open collector.	

: External attachment

Note The pin voltage is measured on Vcc=3.0 V.

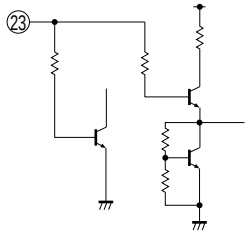
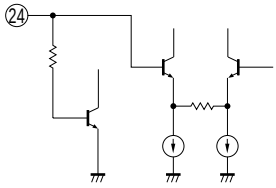
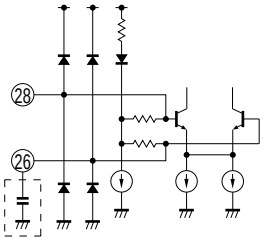
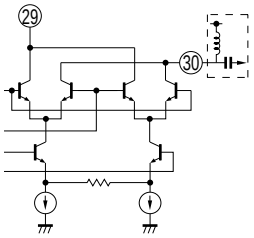
PIN FUNCTIONS

Pin No.	Symbol	Applied Voltage (V)	Pin Voltage Note (V)	Function and Description	Internal Equivalent Circuit
13	$V_{CC}3$	2.7 to 4.0	–	Supply voltage pin for the IF amplifier and RSSI block.	
14	IFout	–	1.5	Output pin for the IF amplifier.	
15	RSSIout	–	0.5 (No input signal)	Output pin for the RSSI. The output resistance is about 35 kΩ.	
16	IFin1	–	1.9	Input pin for the IF amplifier. The input resistance is about 330 Ω.	
17	IFin2	–	1.9	Input pin for the IF amplifier. The input resistance is about 330 Ω.	
18	GND3	0	–	Ground pin for the IF amplifier, RSSI block, and 2nd down converter block. Form as wide a ground pattern as possible to minimize its impedance.	
19	$V_{CC}4$	2.7 to 4.0	–	Power supply voltage pin for the 2nd down converter block.	
20	2nd MIXout	–	1.5	Output pin for the 2nd down converter. The output resistance is about 330 Ω.	
21	2nd MIXinb	–	1.9	Bypass pin for the 2nd down converter block. Ground this pin through an external capacitor.	
22	2nd MIXin	–	1.9	Input pin for the 2nd down converter. High impedance input.	

: External attachment

Note The pin voltage is measured on Vcc=3.0 V.

PIN FUNCTIONS

Pin No.	Symbol	Applied Voltage (V)	Pin Voltage Note (V)	Function and Description	Internal Equivalent Circuit
23	$V_{PS\ (RX)}$	0 to V_{CC}	–	Power save pin for the receiver block (IF amplifier, RSSI, 2nd down converter). This pin is interlocked to the internal regulator and can control the following. V_{PS} (V) / IC stat 2.5 to V_{CC} / ON (Active Mode) 0 to 0.3 / OFF (Sleep Mode)	
24	$V_{PS\ (TX)}$/ V_{AGC}	0 to V_{CC}	–	Power save pin for the transmitter block (quadrature modulator, up converter, AGC circuit). This pin is interlocked to the internal regulator and can control the following. V_{PS} (V) / IC stat 0.9 to V_{CC} / ON (Active Mode) 0 to 0.5 / OFF (Sleep Mode)	
25	V_{CC}5	2.7 to 4.0	–	Supply voltage for the AGC block.	———
26	TX MIX-LOinb	–	2.0	Bypass pin for the local input of the up converter. Ground this pin through an external capacitor.	
28	TX MIX-LOin	–	2.0	Local input pin for the up converter. High impedance input.	
27	GND5	0	–	Ground pin for the AGC and up converter. Form as wide a ground pattern as possible to minimize its impedance.	———
29	V_{CC}6	2.7 to 4.0	–	Supply voltage pin for the up converter block.	
30	TX MIXout	2.7 to 4.0	–	RF output pin for the up converter block. This is an open collector output, so an impedance matching circuit should be attached externally.	

: External attachment

Note The pin voltage is measured on Vcc=3.0 V.

RELATION BETWEEN I/Q PIN INPUT SIGNAL POTENTIAL AND UPPER LIMIT AMPLITUDE

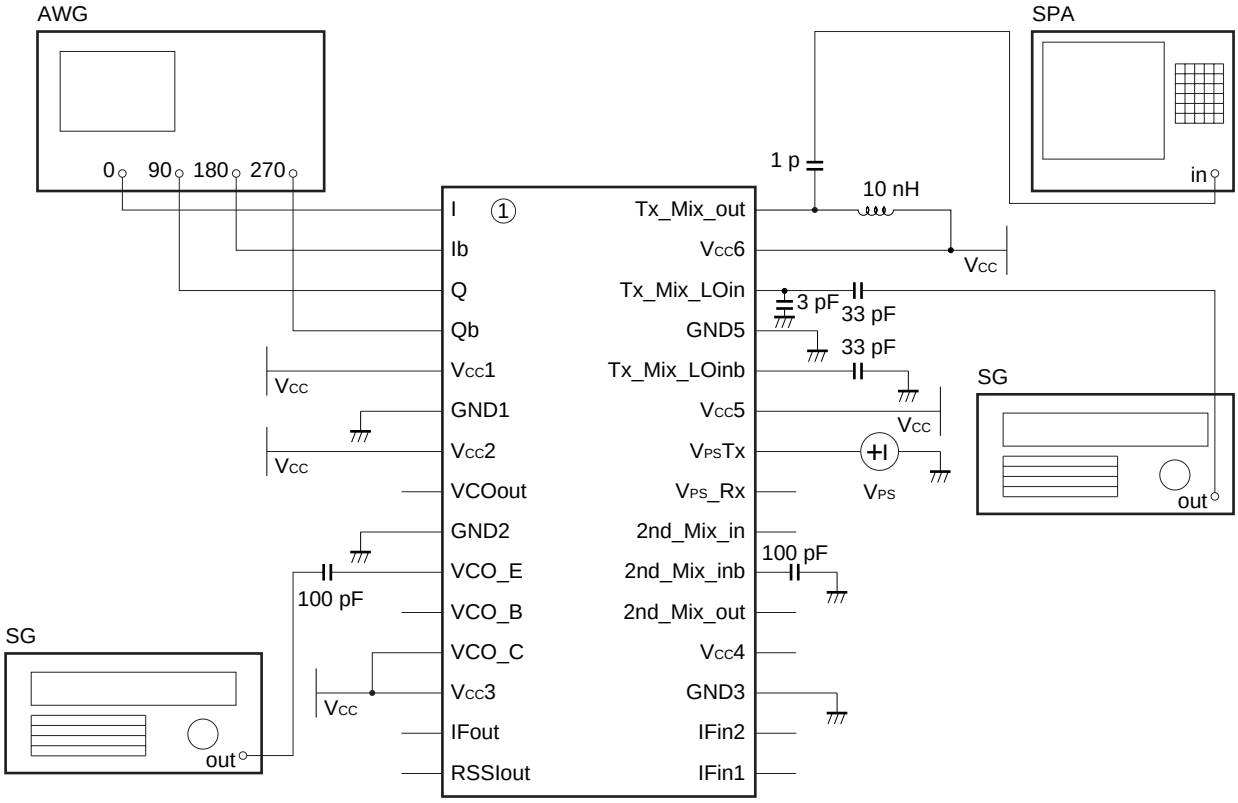
Power Supply Voltage (V) V_{CC}	I/Q bias voltage (V) $V_{CC}/2$ = I = Ib = Q = Qb	Input Amplitude (mV_{P-P})	
		Single ended Input I = Q	Differential Phase Input I = Ib = Q = Qb
2.7	1.35	≤400	≤600
to	to		
3.0	1.5	≤800	≤600
to	to		
4.0	2.0	≤1000	≤600

COMPARISON OF I/Q INPUT AMPLITUDES IN THE SAME TX OUTPUT LEVEL

Power Supply Voltage (V) V_{CC}	I/Q bias voltage (V) $V_{CC}/2$ = I = Ib = Q = Qb	Input Amplitude (mV_{P-P})		Reference Characteristics TX Total Output Level (dBm) $P_{TX-MIXout}$
		Single ended Input I = Q	Differential Phase Input I = Ib = Q = Qb	
2.7	1.35	400	200	–20
3.0	1.5	800	400	–14
4.0	2.0	1200	600	–10.5

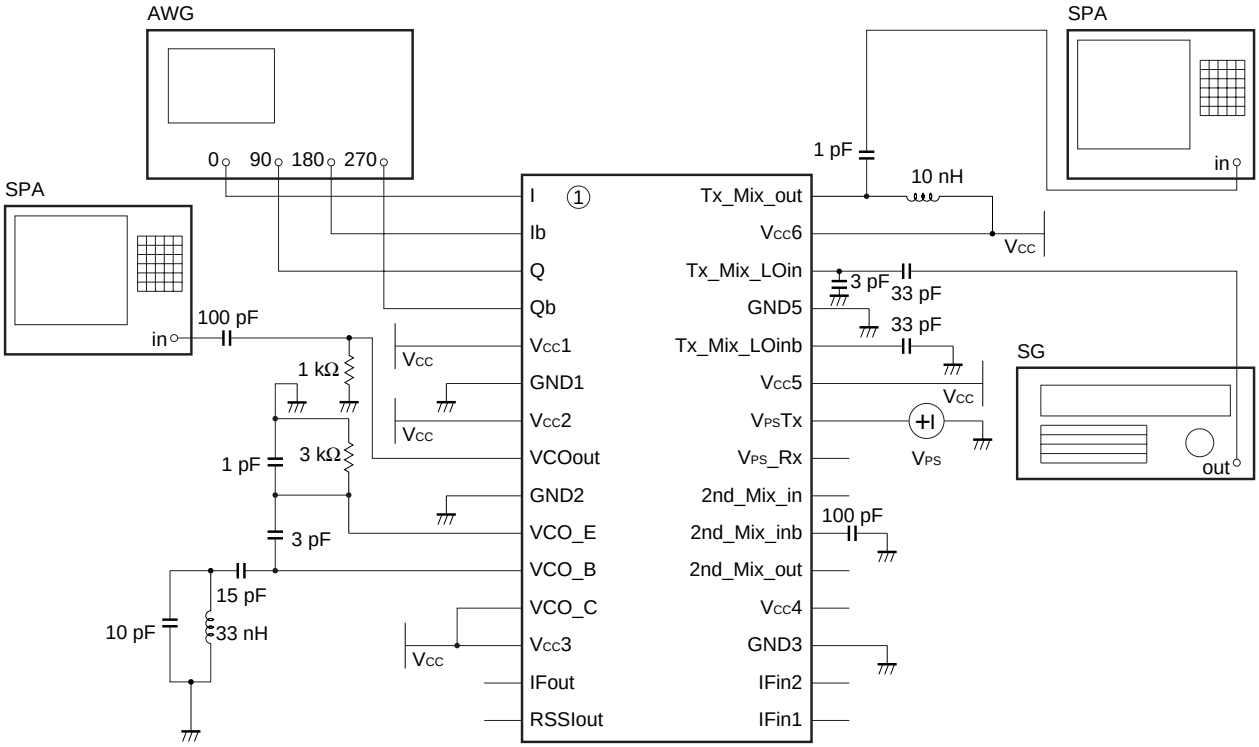
TEST CIRCUIT 1

Transmitter Block (Quadrature Modulator + Up Converter + AGC Circuit)



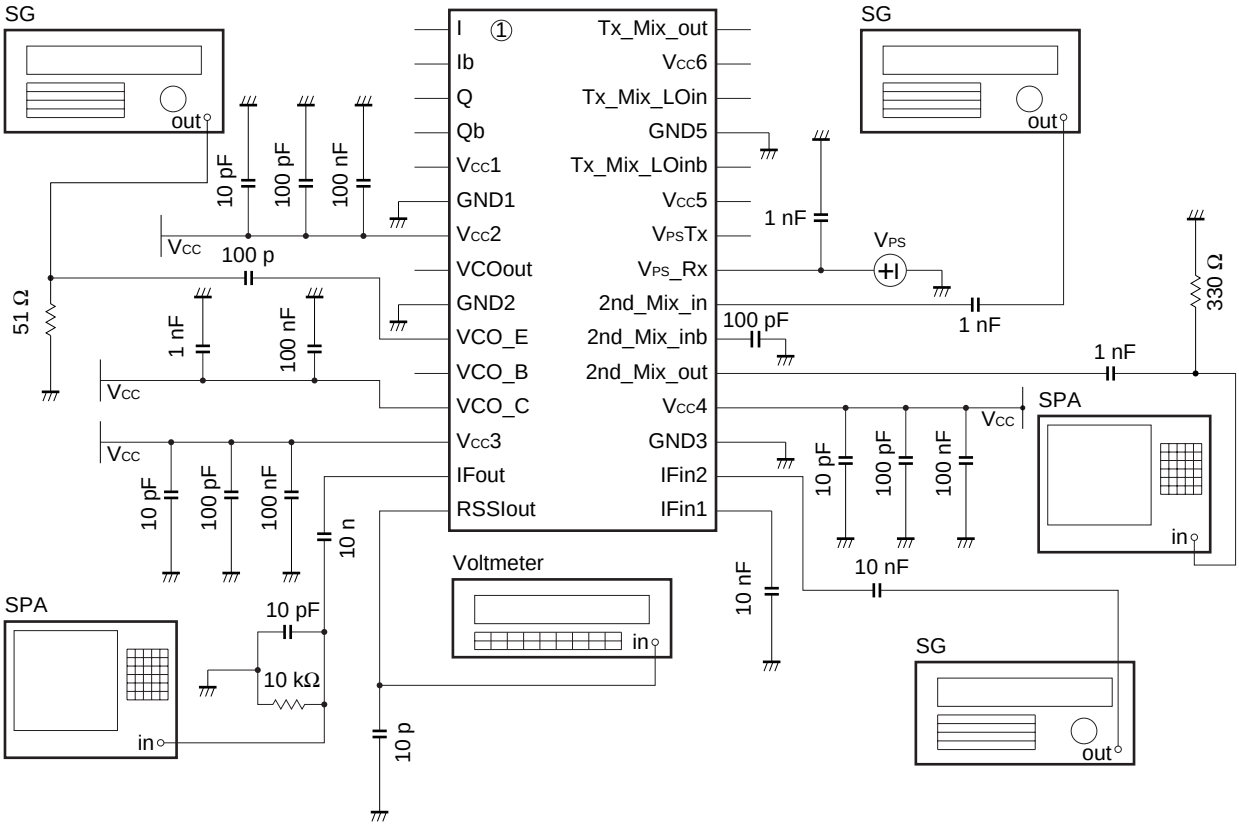
TEST CIRCUIT 2

Transmitter Block + Common Block (Quadrature Modulator + Up Converter + AGC Circuit + 2nd VCO)



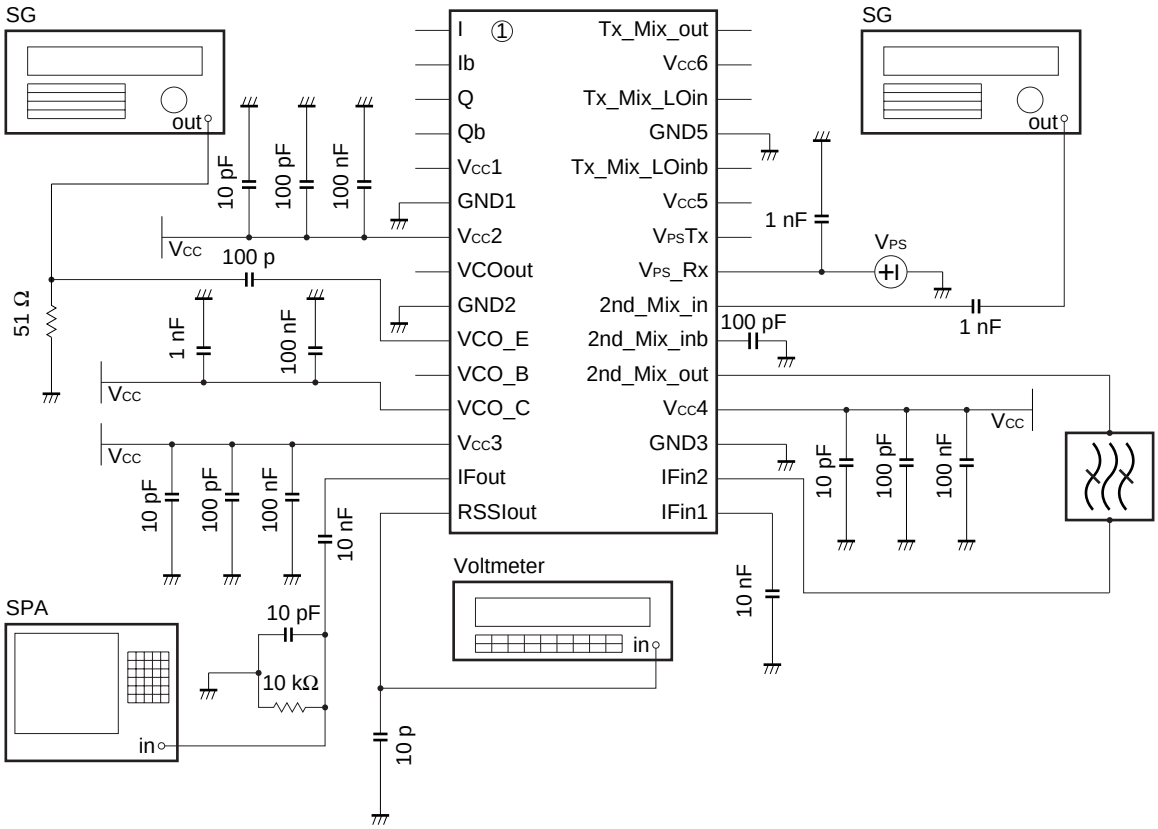
TEST CIRCUIT 3

Receiver Block (2nd Down Converter + 2nd IF Amplifier + RSSI)

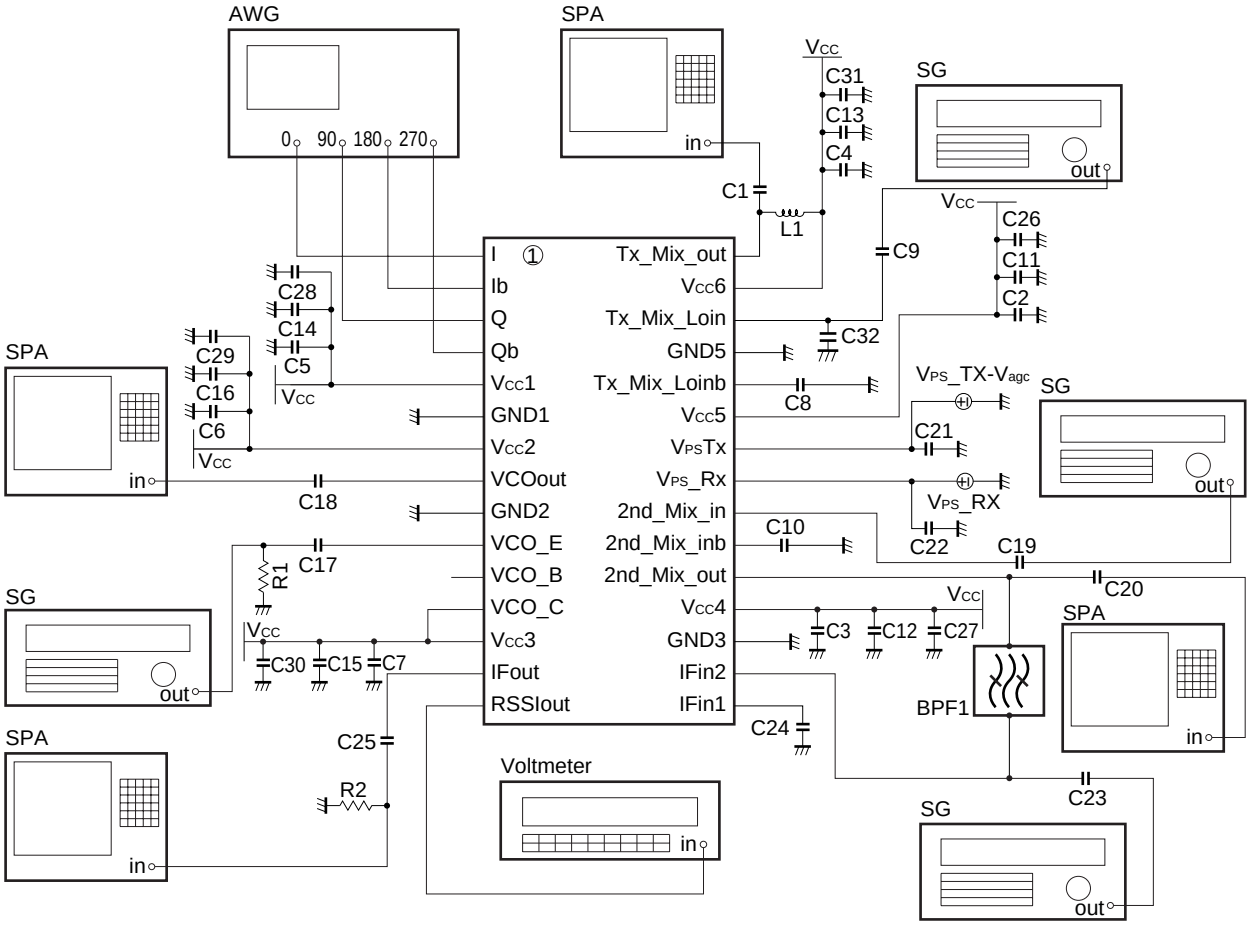


TEST CIRCUIT 4

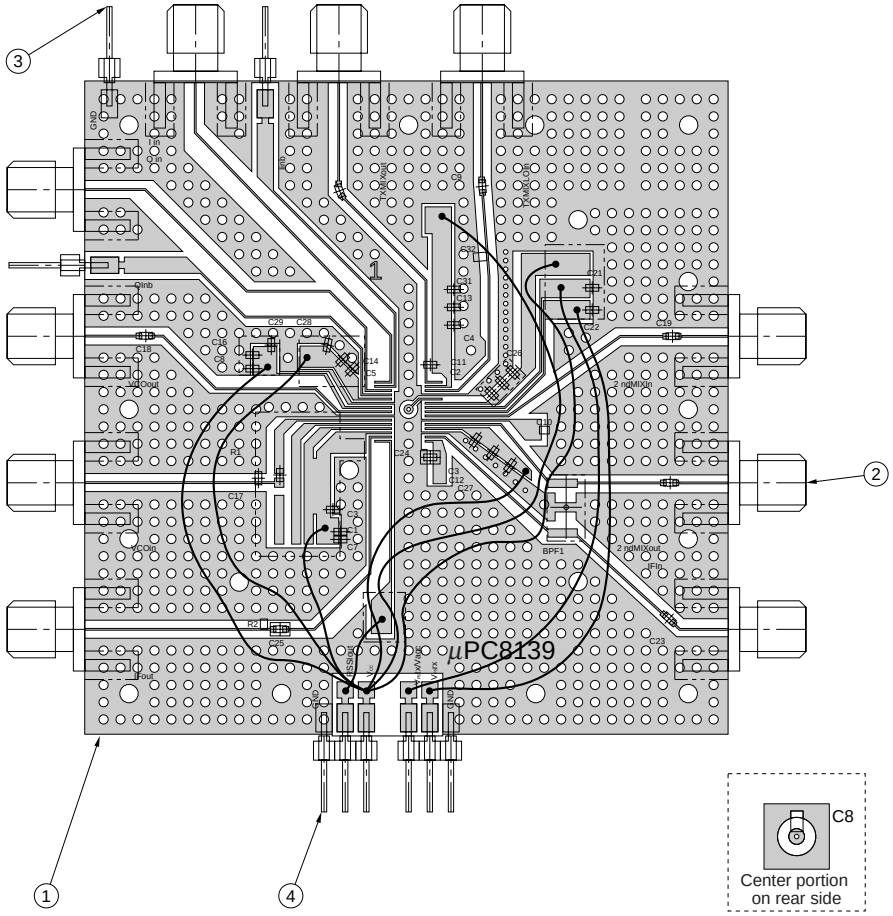
Receiver Block (2nd Down Converter + 2nd IF Amplifier + RSSI)



TEST CIRCUIT TOTAL CONFIGURATION



EXAMPLE OF THE TEST CIRCUIT MOUNTED ON PRINTED CIRCUIT BOARD



Parts List

Symbol	Name	Value	Model name • Specifications	Manufacturer	Quantity
BPF1	BPF		CFEC10.8 MK1	Murata Mfg.	1
L1	Chip inductor	10 nH	TFL0816-10N	SSM	1
R2	Chip resistor	10 kΩ	RR0816R-103-D	SSM	1
R1	Chip resistor	51 Ω	RR0816R-510-D	SSM	1
C32	Chip capacitor	3 pF	GRM39B030J50PB	Murata Mfg.	1
C26 to 31	Chip capacitor	100 nF	GRM39B104J50PB	Murata Mfg.	6
C23 to 25	Chip capacitor	10 nF	GRM39B103J50PB	Murata Mfg.	3
C19 to 22	Chip capacitor	1 nF	GRM39B102J50PB	Murata Mfg.	4
C10 to 18	Chip capacitor	100 pF	GRM39B101J50PB	Murata Mfg.	8
C8 to 9	Chip capacitor	33 pF	GRM39B330J50PB	Murata Mfg.	2
C2 to 7	Chip capacitor	10 pF	GRM39B100J50PB	Murata Mfg.	7
C1	Chip capacitor	1 pF	GRM39B010J50PB	Murata Mfg.	1
④	PCC pin		A2-3PA-2.54DSA	Hirose Electric	2
③	PCC pin		A2-1PA-2.54DSA	Hirose Electric	3
②	SMA connector		142-0701-881	JHONSON	10
①	Polyimide substrate		R4775 (t0.2)	Matsushita Electric Works	1

Notes on the board

(1) Copper patterning on a polyimide board of 76 × 76 × 0.2 mm in size.

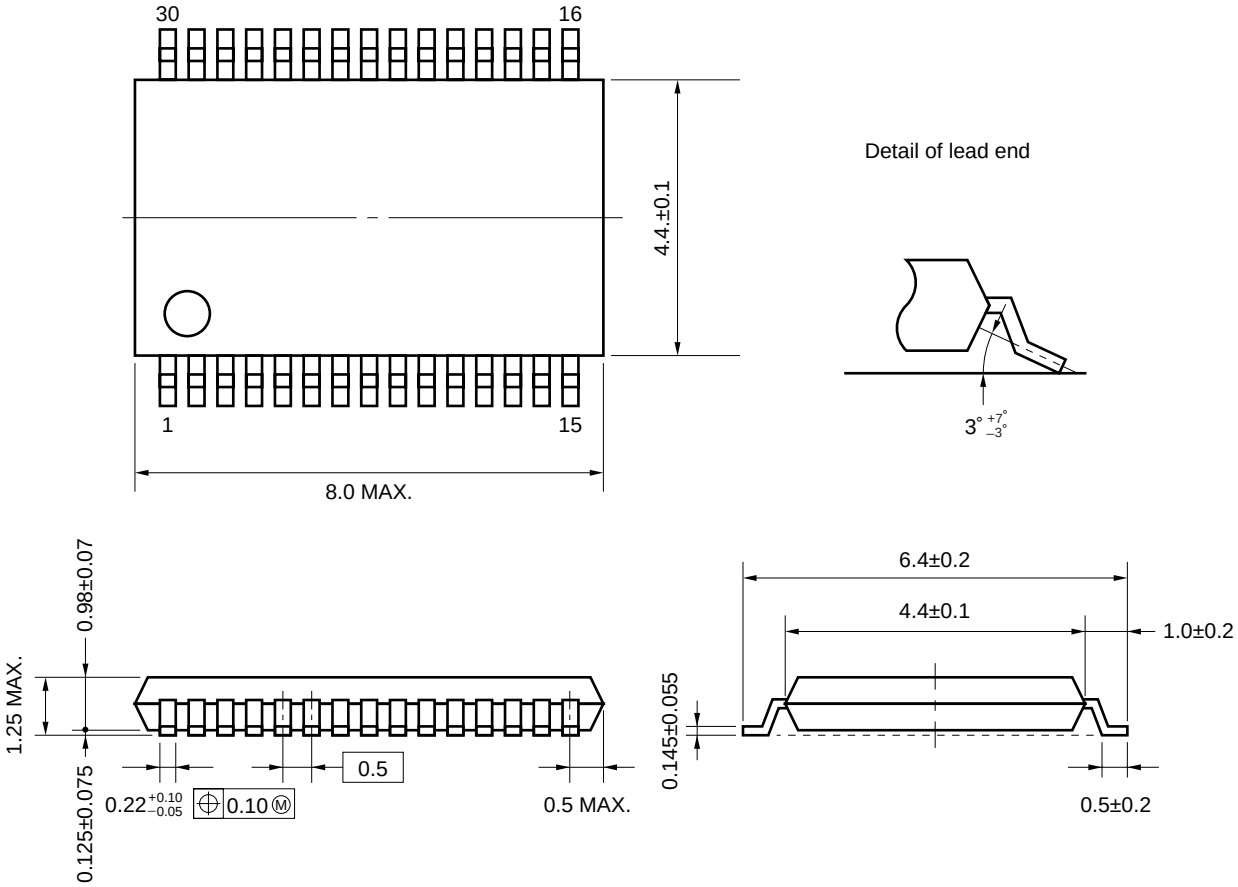
(2) Full grounding on rear side.

(3) Solder coating over patterns.

(4) ○ and ◯ indicate through holes.

PACKAGE DIMENSIONS

30-pin plastic TSSOP (225 mil) (Unit: mm)



CAUTIONS ON USE

1. **Observe precautions for handling because this IC is an electrostatic sensitive device.**
2. **Form as wide a ground pattern as possible to minimize its impedance.**
3. **Keep the track length of the ground pins as short as possible (to prevent malfunction).**
4. **Connect a bypass capacitor to the Vcc pin.**

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions.

For soldering methods and conditions other than the recommended conditions, consult an NEC sales representative.

μPC8139GR-7JH

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C. Duration: 30 sec. max. (210°C or above) Number of times: 2, Exposure limit: None[Note]	IR35-00-2
VPS	Package peak temperature: 215°C. Duration: 40 sec. max. (200°C or above) Number of times: 2, Exposure limit: None[Note]	VP15-00-2
Wave soldering	Soldering bath temperature : 260°C max. Duration: 10 sec. max. Number of times: 1, Exposure limit: None[Note]	WS60-00-1
Partial heating method	Pin temperature: 300°C max. Duration: 3 sec. max. (per side of device) Exposure limit: None[Note]	

Note Storage period (days) after opening the dry pack. Storage conditions: 25°C and 65% RH or less (This product is not dry packed.)

Caution Do not use different soldering methods together (except for pin partial heating.)

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**

M4 96.5