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GENNUM CORPORATION

PRO-LINX™ GS7025 Serial Digital Receiver

PRELIMINARY DATA SHEET

FEATURES

- **SMPTE 259M-C compliant (270Mb/s)**
- **automatic cable equalization (typically greater than 350m of high quality cable)**
- **serial data outputs muted and serial clock remains active when input data is lost**
- **operation independent of SAV/EAV sync signals**
- **signal strength indicator output**
- **carrier detect with programmable threshold level**
- **power savings mode (output serial clock disable)**
- **large IJT, typically 0.56UI beyond loop bandwidth**
- **robust lock detect**

APPLICATIONS

Cable equalization plus clock and data recovery for all high speed serial digital interface applications involving SMPTE 259M-C.

DESCRIPTION

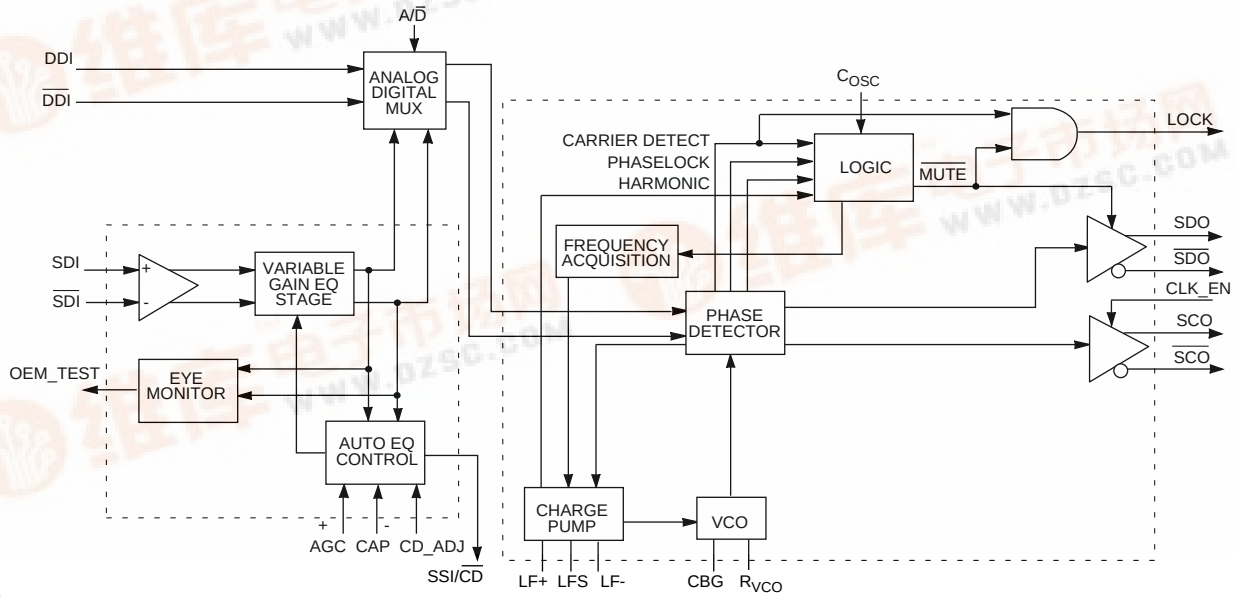
The GS7025 provides automatic cable equalization and high performance clock and data recovery for serial digital signals. The GS7025 receives either single-ended or differential serial digital data and outputs differential clock and retimed data signals at PECL levels (800mV). The on-board cable equalizer provides up to 35dB of gain at 135MHz which typically results in equalization of greater than 350m of high quality cable at 270Mb/s.

The GS7025 requires only one external resistor to set the VCO centre frequency and provides adjustment free operation.

The GS7025 has dedicated pins to indicate signal strength, carrier detect, and LOCK. Optional external resistors allow the carrier detect threshold level to be customized to the user's requirement. In addition, the GS7025 provides an 'Output Eye Monitor Test' (OEM_TEST) for diagnostic testing of signal integrity after equalization, prior to reslicing. The serial clock outputs can also be disabled to reduce power. The GS7025 operates from a single +5 or -5 volt supply.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS7025-CQM	44 pin MQFP Tray	0°C to 70°C
GS7025-CTM	44 pin MQFP Tape	0°C to 70°C



BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage (V_S)	5.5V
Input Voltage Range (any input)	V_{CC} + 0.5 to V_{EE} - 0.5V
Operating Temperature Range	0°C ≤ T_A ≤ 70°C
Storage Temperature Range	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, T_A = 25°C unless otherwise stated, R_{LF} = 1.8k, C_{LF1} = 15nF, C_{LF2} = 3.3pF

PARAMETER	CONDITION	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
Supply Voltage		4.75	5	5.25	V		1
Supply Current	CLK_EN = 0	-	115		mA		1
	CLK_EN = 1	-	125				
SDI Common Mode Voltage		-	2.5	-	V		1
DDI Common Mode Input Voltage Range		V_{EE}+(V_{DIFF}/2)	0.4 to 4.6	V_{CC}-(V_{DIFF}/2)	V	2	1
DDI Differential Input Drive		200	800	2000	mV		1
SSI/CD Output Current	Source, C_{LMAX} = 50pF, R_L = open cct.	-	-	18	µA		3
	Source, C_{LMAX} = 50pF, R_L=5K	-	-	110	µA		3
	Sink	-	1.0	1.5	mA		3
AGC Common Mode Voltage		-	2.7	-	V		1
OEM_TEST Bias Potential		-	4.5	-	V	5	1
A/$\overline{D}$	High	2.0	-	-	V		1
	Low	-	-	0.8			
270, CLK_EN, IN _ENABLE Input Voltage	High	2.0	-	-	V		1
	Low	-	-	0.8			
CLK_EN Input Voltage	High	2.5	-	-	V		1
	Low	-	-	0.8			

DC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 5.0V, T_A = 25°C unless otherwise stated, R_{LF} = 1.8k, C_{LF1} = 15nF, C_{LF2} = 3.3pF

PARAMETER	CONDITION	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
LOCK Output Sink Current		500	-	-	µA	3	1
CLK_EN Source Current	Low	-	26	55	µA		1

NOTES
1. TYPICAL - measured on characterization board.
2. V_{DIFF} is the differential input signal swing.
3. LOCK is an open collector output and requires an external pullup resistor.
4. If OEM_TEST is permanently enabled, operating temperature range is limited from 0°C to 60°C inclusive.

TEST LEVELS
1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{EE} = 0V, T_A = 25°C unless otherwise stated, R_{LF} = 1.8k, C_{LF1} = 15nF, C_{LF2} = 3.3pF

PARAMETER	CONDITIONS	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
Serial Data Rate	SDI	-	270 (only)	-	Mb/s		1
Maximum Equalizer Gain (see Figure 3)	@ 135MHz	-	35	-	dB		7
Additive Jitter [Pseudorandom (2^{23} -1)]	270Mb/s, 300m (Belden 8281)	-	300	-	ps p-p	2, 7	3
Intrinsic Jitter [Pseudorandom (2^{23} -1)]	270Mb/s	-	185	-	ps p-p	2, 6	4
Intrinsic Jitter [Pathological (SDI checkfield)]	270Mb/s	-	462	-	ps p-p	2, 6	1
Input Jitter Tolerance	270Mb/s	0.40	0.56	-	UI p-p	3, 6	1
Lock Time - Synchronous Switch	t_{switch} < 0.5µs, 270Mb/s	-	1	-	µs	4	7
	0.5µs< t_{switch} <10ms	-	1	-	ms		
	t_{switch} > 10 ms	-	4	-	ms		
Carrier Loss Time		0.5	1	2	µs	5	7
SDO to SCO Synchronization		-200	0	200	ps		7
SDO, SCO Output Signal Swing	75Ω DC load	600	800	1000	mV p-p		1
SDO, SCO Rise & Fall times	20%-80%	200	300	400	ps		7
SDI/$\overline{SDI}$ Input Resistance		-	10	-	kΩ	7	6
SDI/$\overline{SDI}$ Input Capacitance		-	1.0	-	pF	7	6
SDI/$\overline{SDI}$ Input Return Loss	at 270MHz	15	20	-	dB	7	6

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{EE} = 0V, T_A = 25°C unless otherwise stated, R_{LF} = 1.8k, C_{LF1} = 15nF, C_{LF2} = 3.3pF

PARAMETER	CONDITIONS	MIN	TYPICAL[1]	MAX	UNITS	NOTES	TEST LEVEL
Carrier Detect Response Time	Carrier Applied, C_L<50pF, R_L=open cct.	-	3	-	µs	7	6
	Carrier Removed, C_L<50pF, R_L=open cct.	-	30	-			

NOTES
1. TYPICAL - measured on characterization board.
2. Characterized 6 sigma rms.
3. IJT measured with sinusoidal modulation beyond Loop Bandwidth (at 6.5MHz).
4. Synchronous switching refers to switching the input data from one source to another source which is at the same data rate (ie. line 10 switching for component NTSC).
5. Carrier Loss Time refers to the response of the SDO output from valid re-clocked input data to mute mode when the input signal is removed.
6. Using the DDI input, A/$\overline{D}$=0.
7. Using the SDI input, A/$\overline{D}$=1.

TEST LEVELS
1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
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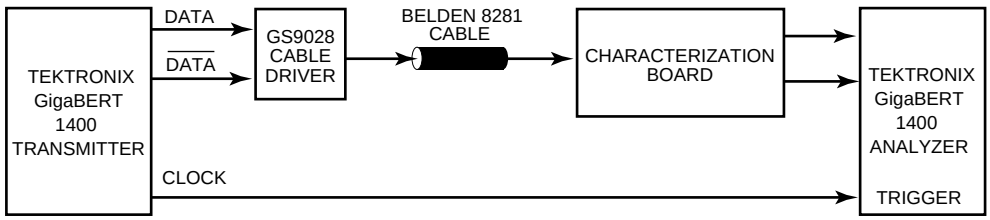
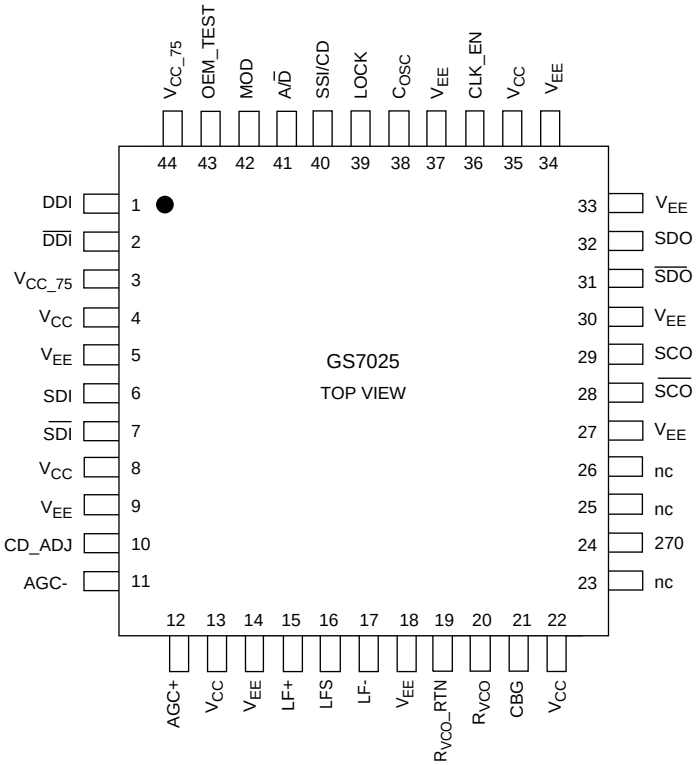


Fig. 1 Test Setup for Figures 5 and 6

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1, 2	DDI/$\overline{\text{DDI}}$	I	Digital data inputs (Differential ECL/PECL).
3, 44	V_{CC}_75	I	Power supply connection for internal 75Ω pullup resistors connected to DDI/$\overline{\text{DDI}}$.
4, 8, 13, 22, 35	V_{CC}	I	Most positive power supply connection.
5, 9, 14, 18, 27, 30, 33, 34, 37	V_{EE}	I	Most negative power supply connection.
6, 7	SDI/$\overline{\text{SDI}}$	I	Differential analog data inputs.
10	CD_ADJ	I	Carrier detect threshold adjust.
11, 12	AGC-, AGC+	I	External AGC capacitor.
15, 16, 17	LF+, LFS, LF-	I	Loop filter component connection.
19	R_{VCO}_RTN	I	R_{VCO} Return.
20	R_{VCO}	I	Frequency setting resistor.
21	CBG	I	Internal bandgap voltage filter capacitor.
23, 25, 26	nc	-	No connect - Do not connect to power or ground. Leave floating.
24	270	I	270Mb/s Data Rate Select - Always set high.
28, 29	$\overline{\text{SCO}}$/SCO	O	Serial clock output. $\overline{\text{SCO}}$/SCO are differential current mode outputs and require external 75Ω pullup resistors.
31, 32	$\overline{\text{SDO}}$/SDO	O	Equalized and reclocked serial digital data outputs. $\overline{\text{SDO}}$/SDO are differential current mode outputs and require external 75Ω pullup resistors.

PIN DESCRIPTIONS (continued)

NUMBER	SYMBOL	TYPE	DESCRIPTION
36	CLK_EN	I	Clock enable. When HIGH, the serial clock outputs are enabled.
38	C_{OSC}	I	Timing control capacitor for internal system clock.
39	LOCK	O	Lock indication. When HIGH, the GS7025 is locked. LOCK is an open collector output and requires an external 10kΩ pullup resistor.
40	SSI/CD	O	Signal strength indicator/Carrier detect.
41	$A/\overline{D}$	I	Analog/Digital select.
42	MOD	I	270 Mb/s modulus select - Always set high.
43	OEM_TEST	O	Output 'Eye' monitor test. Single-ended current mode output that requires an external 50Ω pullup resistor. This feature is recommended for debugging purposes only. If enabled during normal operation, the maximum operating temperature is rated to 60°C.

TYPICAL PERFORMANCE CURVES (V_S = 5V, T_A = 25°C unless otherwise shown)

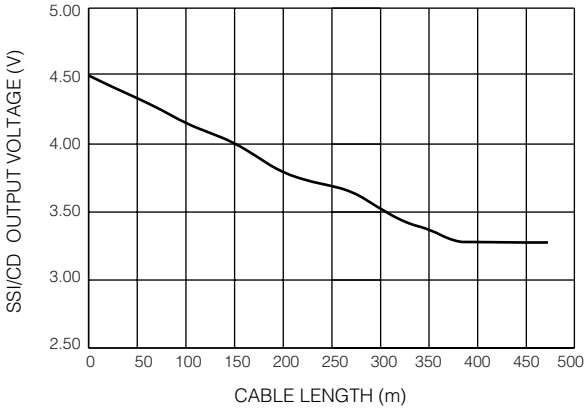


Fig. 2 SSI/CD Voltage vs. Cable Length (Belden 8281) (CD_ADJ = 0V)

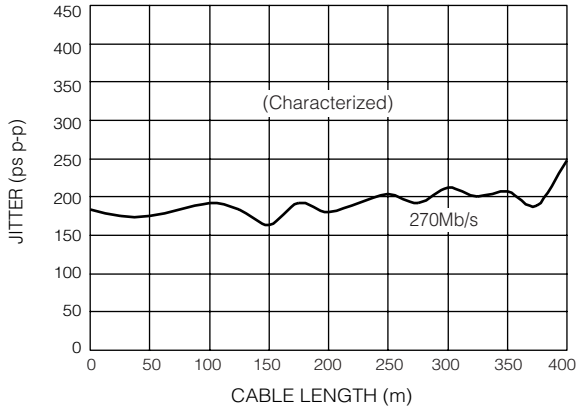


Fig. 5 Typical Additive Jitter vs. Input Cable Length (Belden 8281) Pseudorandom (2^{23}-1)

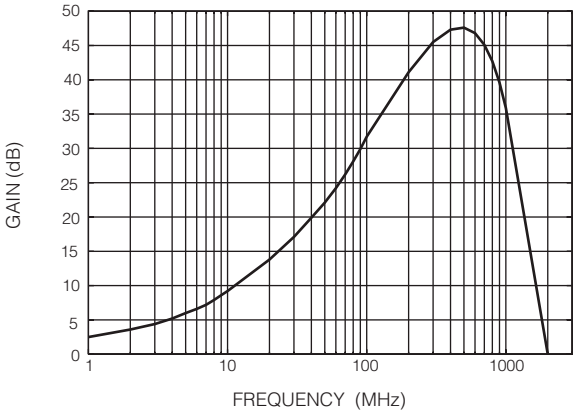


Fig. 3 Equalizer Gain vs. Frequency

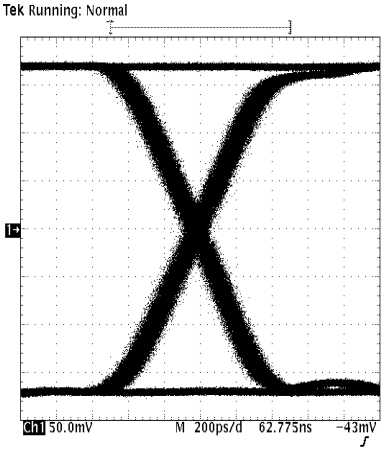


Fig. 6 Intrinsic Jitter (2^{23} - 1 Pattern) 270Mb/s

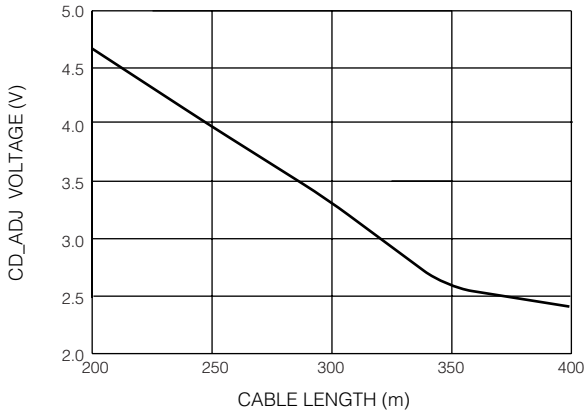


Fig. 4 Carrier Detect Adjust Voltage Threshold Characteristics

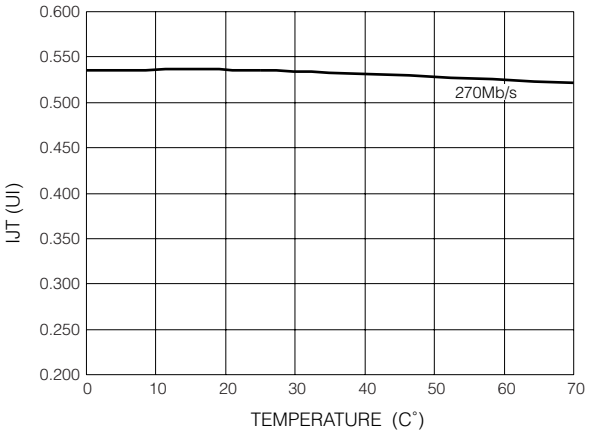


Fig. 7 Typical IJT vs. Temperature (V_{CC} = 5.0V) (Characterized)

DETAILED DESCRIPTION

The GS7025 Serial Digital Receiver is a bipolar integrated circuit containing a built-in cable equalizer and reclocker.

Serial digital signals are applied to either the analog SDI/$\overline{\text{SDI}}$ or digital DDI/$\overline{\text{DDI}}$ inputs. Signals applied to the SDI/$\overline{\text{SDI}}$ inputs are equalized and then passed to a multiplexer. Signals applied to the DDI/$\overline{\text{DDI}}$ inputs bypass the equalizer and go directly to the multiplexer. The analog/digital select pin (A/$\overline{\text{D}}$) determines which signal is then passed to the reclocker.

Packaged in a 44 pin MQFP, the receiver operates from a single 5V supply at a data rate of 270Mb/s.

1. CABLE EQUALIZER

The automatic cable equalizer is designed to equalize a serial digital data rate of 270Mb/s.

The serial data signal is connected to the input pins (SDI/$\overline{\text{SDI}}$) either differentially or single-endedly. The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length. The gain stage provides up to 35dB of gain at 135MHz which typically results in equalization of greater than 350m of Belden 8281 cable at 270Mb/s.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by an external differential AGC filter capacitor (AGC+/AGC-) providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter.

The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its corrective level irrespective of shifts due to AC coupling.

1-1. Signal Strength Indication/Carrier Detect

The GS7025 incorporates an analog signal strength indicator/carrier detect (SSI/CD) output indicating both the presence of a carrier and the amount of equalization applied to the signal. The voltage output of this pin versus cable length (signal strength) is shown in Figure 2 and Figure 8.

With 0m of cable (800mV input signal levels), the SSI/CD output voltage is approximately 4.5V. As the cable length increases, the SSI/CD voltage decreases linearly providing accurate correlation between the SSI/CD voltage and cable length.

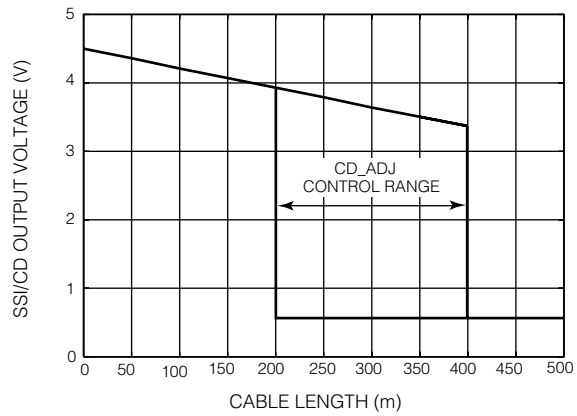


Fig. 8 SSI/CD Voltage vs. Cable Length

When the signal strength decreases to the level set at the "Carrier Detect Threshold Adjust" pin, the SSI/CD voltage goes to a logic "0" state (0.8 V) and can be used to drive other TTL/CMOS compatible logic inputs. In addition, when loss of carrier is detected, the SDO/$\overline{\text{SDO}}$ outputs are muted (set to a known static state).

1-2. Carrier Detect Threshold Adjust

This feature has been designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on chip reference. To alleviate this problem, the GS7025 provides a user adjustable threshold to meet the unique conditions that exist in each user's application. Override and internal default settings have also been provided to give the user total flexibility.

The threshold level at which loss of carrier is detected is adjustable via external resistors at the CD_ADJ pin (*see Figure 4*). The control voltage at the CD_ADJ pin is set by a simple resistor divider circuit (*see Typical Application Circuit*). The threshold level is adjustable from 200m to 350m. By default (no external resistors), the threshold is typically 320m. In noisy environments, it is not recommended to leave this pin floating. Connecting this pin to V_{EE} disables the SDO/$\overline{\text{SDO}}$ muting function and allows for maximum possible cable length equalization.

1-3. Output Eye Monitor Test

The GS7025 also provides an 'Output Eye Monitor Test' (OEM_TEST) which allows the verification of signal integrity after equalization, prior to reslicing. The OEM_TEST pin is an open collector current output that requires an external 50Ω pullup resistor. When the pullup resistor is not used, the OEM_TEST block is disabled and the internal OEM_TEST circuit is powered down. The OEM_TEST

provides a 100mVp-p signal when driving a 50Ω oscilloscope input. Due to additional power consumed by this diagnostic circuit, it is not recommended for continuous operation.

2. RECLOCKER

The reclocker receives a differential serial data stream from the internal multiplexer. It locks an internal clock to the incoming data. It outputs the differential PECL retimed data signal on SDO/$\overline{\text{SDO}}$. It outputs the recovered clock on SCO/$\overline{\text{SCO}}$. The timing between the output and clock signals is shown in Figure 9.

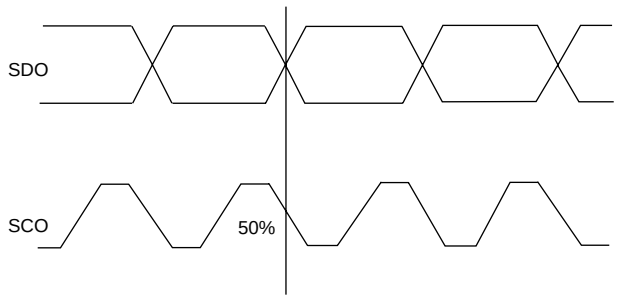


Fig. 9 Output and Clock Signal Timing

The reclocker contains three main functional blocks: the Phase Locked Loop, Frequency Acquisition, and Logic Circuit.

2-1. Phase Locked Loop (PLL)

The Phase Locked Loop locks the internal PLL clock to the incoming data rate. A simplified block diagram of the PLL is shown below. The main components are the VCO, the phase detector, the charge pump, and the loop filter.

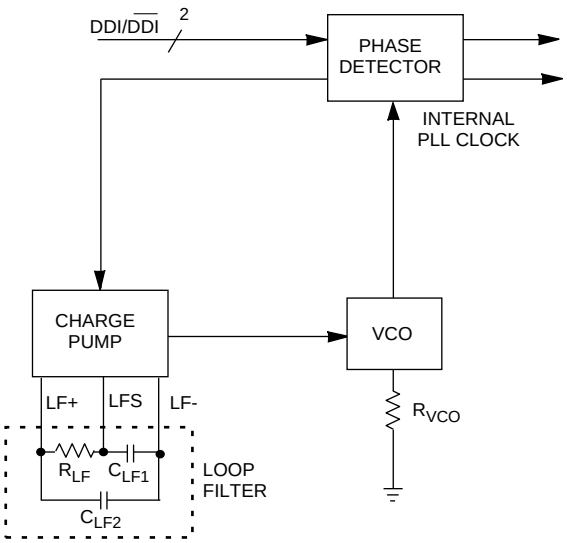


Fig. 10 Simplified Block Diagram of the PLL

2-2. VCO

The VCO is a differential low phase noise, factory trimmed oscillator that provides increased immunity to PCB noise and precise control of the VCO centre frequency. The VCO has a pull range of ±15% about the centre frequency. A single low impedance external resistor, R_{VCO}, sets the VCO centre frequency. The low impedance R_{VCO} minimizes thermal noise and reduces the PLL's sensitivity to PCB noise.

The recommended R_{VCO} value for SMPTE 259M-C applications is 365Ω.

When the input data stream is removed for an excessive period of time *(see AC electrical characteristics table),* the VCO frequency can drift from the 270Mb/s centre frequency to the limits shown in Table1.

TABLE 1: Frequency Drift Range

FREQUENCY	MIN (%)	MAX(%)
270Mb/s lock	-13	28

2-3. Phase Detector

The phase detector compares the phase of the PLL clock with the phase of the incoming data signal and generates error correcting timing pulses. The phase detector design provides a linear transfer function which maximizes the input jitter tolerance of the PLL.

2-4. Charge Pump

The charge pump takes the phase detector output timing pulses and creates a charge packet that is proportional to the system phase error. A unique differential charge pump design insures that the output phase does not drift when data transitions are sparse. This makes the GS7025 ideal for SMPTE 259M-C applications where pathological signals have data transition densities of 0.05.

2-5. Loop Filter

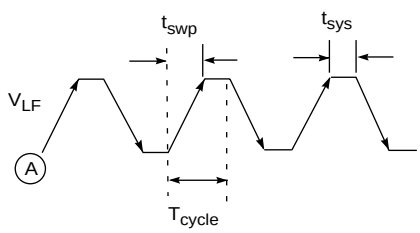
The loop filter integrates the charge pump packets and produces a VCO control voltage. The loop filter is comprised of three external components which are connected to pins LF+, LFS, and LF-. The loop filter design is fully differential giving the GS7025 increased immunity to PCB board noise.

The loop filter components are critical in determining the loop bandwidth and damping of the PLL. Choosing these component values is discussed in detail in the PLL DESIGN GUIDELINES section. Recommended values for SMPTE 259M-C applications are shown in the Typical Application Circuit. No further changes from the recommended GS7025 loop filter components are necessary.

3. FREQUENCY ACQUISITION

The core PLL is able to lock if the incoming data rate and the PLL clock frequency are within the PLL capture range (which is slightly larger than the loop bandwidth). To assist the PLL to lock, the GS7025 uses a frequency acquisition circuit.

The frequency acquisition circuit sweeps the VCO control voltage so that the VCO frequency changes from -10% to +10% of the centre frequency. Figure 11 shows a typical sweep waveform.



$T_{cycle} = t_{swp} + t_{sys}$

Fig. 11 Typical Sweep Waveform

The VCO frequency starts at point A and sweeps up attempting to lock. If lock is not established during the up sweep, the VCO is then swept down. The system is designed such that the probability of locking within one cycle period is greater than 0.999. If the system does not lock within one cycle period, it will attempt to lock in the subsequent cycle.

The average sweep time, t_{swp}, is determined by the loop filter component, C_{LF1}, and the charge pump current, I_{CP}:

$$t_{SWP} = \frac{4C_{LF1}}{3I_{CP}}$$

The nominal sweep time is approximately 121µs when C_{LF1} = 15nF and I_{CP} = 165µA (R_{VCO} = 365Ω).

An internal system clock determines t_{sys} *(see section 3-1, Logic Circuit).*

3-1. Logic Circuit

The GS7025 is controlled by a finite state logic circuit which is clocked by an asynchronous system clock. That is, the system clock is completely independent of the incoming data rate. The system clock runs at low frequencies, relative to the incoming data rate, and thus reduces interference to the PLL.The period of the system clock is set by the C_{OSC} capacitor and is:

$$t_{sys} = 9.6 \times 10^4 \times C_{OSC}[\text{seconds}]$$

The recommended value for t_{sys} is 450µs (C_{OSC} = 4.7nF)

4. LOCKING

The GS7025 indicates valid lock when the following three conditions are satisfied:

1. Input data is detected.
2. The incoming data signal and the PLL clock are phase locked.
3. The system is not locked to an integer-multiple harmonic of a 270Mb/s SMPTE 259M-C signal.

The GS7025 defines the presence of input data when at least one data transition occurs every 1µs.

The GS7025 assumes that it is NOT locked to a harmonic if the pattern '101' or '010' (in the reclocked data stream) occurs at least once every $t_{sys}/3$ seconds. Using the recommended component values, this corresponds to approximately 150µs. In a harmonically locked system, all bit cells are double clocked and the above patterns become '110011' and '001100', respectively.

4-1. Lock Time

Synchronous switching refers to the case where the input data is changed from one source to another source which is at the same data rate (but different phase).

When input data to the GS7025 is removed, the GS7025 latches the current state. Therefore, when data is reapplied, the GS7025 begins the lock procedure at the previous locked data rate. As a result, in synchronous switching applications, the GS7025 locks very quickly. The nominal lock time depends on the switching time and is summarized in the Table 3.

TABLE 3.

SWITCHING TIME	LOCK TIME
<0.5µs	10µs
0.5µs - 10ms	$2t_{sys}$
>10ms	$2T_{cycle} + 2t_{sys}$

To acquire lock, the frequency acquisition circuit may have to sweep over an entire cycle depending on initial conditions. Maximum lock time is $2T_{cycle} + 2t_{sys}$.

The nominal value of T_{cycle} for the GS7025 operating in a typical SMPTE 259M-C application is approximately 1.3ms.

The GS7025 has a dedicated LOCK output (pin 39) indicating when the device is locked. It should be noted that in synchronous switching applications where the switching time is less than 0.5µs, the LOCK output will NOT be de-asserted and the data outputs will NOT be muted.

5. OUTPUT DATA MUTING

The GS7025 internally mutes the SDO and $\overline{SDO}$ outputs when the device is not locked. When muted, SDO/$\overline{SDO}$ are latched providing a logic state to the subsequent circuit and avoiding a condition where noise could be amplified and appear as data.

The output data muting timing is shown in Figure 12.

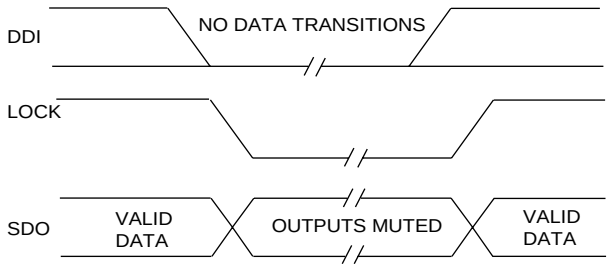


Fig. 12 Output Data Muting Timing

6. CLOCK ENABLE

When CLK_EN is high, the GS7025 SCO/$\overline{SCO}$ outputs are enabled. When CLK_EN is low, the SCO/$\overline{SCO}$ outputs are placed in a high Z state and float to V_{CC}. Disabling the clock outputs results in a power savings of 10%. It is recommended that the CLK_EN input be hard wired to the desired state. For applications which do not require the clock output, connect CLK_EN to Ground and connect the SCO/$\overline{SCO}$ outputs to V_{CC}.

7. STRESSFULL DATA PATTERNS

All PLL's are susceptible to stressful data patterns which can introduce bit errors in the data stream. PLL's are most sensitive to patterns which have long run lengths of 0's or 1's (low data transition densities for a long period of time). The GS7025 is designed to operate with low data transition densities such as the SMPTE 259M-C pathological signal (data transition density = 0.05).

8. I/O DESCRIPTION

8-1. High Speed Analog Inputs (SDI/$\overline{SDI}$)

SDI/$\overline{SDI}$ are high impedance inputs which accept differential or single-ended input drive.

Figure 13 shows the recommended interface when a single-ended serial digital signal is used.

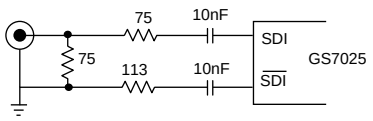


Fig. 13

8-2. High Speed Digital Inputs (DDI/$\overline{DDI}$)

DDI/$\overline{DDI}$ are high impedance inputs which accept differential or single-ended input drive. Two conditions must be observed when interfacing to these inputs:

1. Input signal amplitudes are between 200 and 2000mV.
2. The common mode input voltage range is as specified in the DC Characteristics table.

Commonly used interface examples are shown in Figures 14 to 16.

Figure 14 illustrates the simplest interface to the GS7025 digital inputs. In this example, the driving device generates the PECL level signals (800mV amplitudes) having a common mode input range between 0.4 and 4.6V. This scheme is recommended when the trace lengths are less than 1in. The value of the resistors depends on the output driver circuitry.

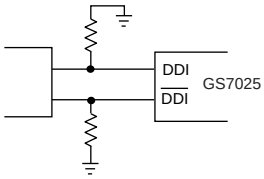


Fig. 14

When trace lengths become greater than 1in, controlled impedance traces should be used. The recommended interface is shown in Figure 15. In this case, a parallel resistor (R_{LOAD}) is placed near the GS7025 inputs to terminate the controlled impedance trace. The value of R_{LOAD} should be twice the value of the characteristic impedance of the trace. In addition, place series resistors (R_{SOURCE}) near the driving chip to serve as source terminations. They should be equal to the value of the trace impedance. Assuming 800mV output swings at the driver, R_{LOAD} = 100Ω, R_{SOURCE} = 50Ω and Z_O = 50Ω.

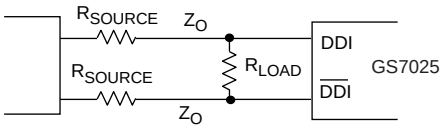


Fig. 15

Figure 16 shows the recommended interface when the GS7025 digital inputs are driven single-endedly. In this case, the input must be AC-coupled and a matching resistor (Zo) must be used.

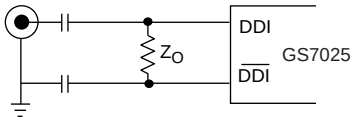


Fig. 16

When the DDI and the $\overline{DDI}$ inputs are not used, saturate one input of the differential amplifier for improved noise immunity. To saturate, connect either pins 44 and 1 or pins 2 and 3 to V_{CC}. Leave the other pair floating.

8-3. High Speed Outputs (SDO/$\overline{SDO}$ and SCO/$\overline{SCO}$)

SDO/$\overline{SDO}$ and SCO/$\overline{SCO}$ are current mode outputs that require external pullups (*see Figure 17*). The output signal swings are 800mV when 75Ω resistors are used. To shift the signal levels down by approximately 0.7 volts, place a diode between V_{CC} and the pullups. When the output traces are longer than 1in, use controlled impedance traces. Place the pullup resistors at the end of the output traces as they terminate the trace in its characteristic impedance (75Ω).

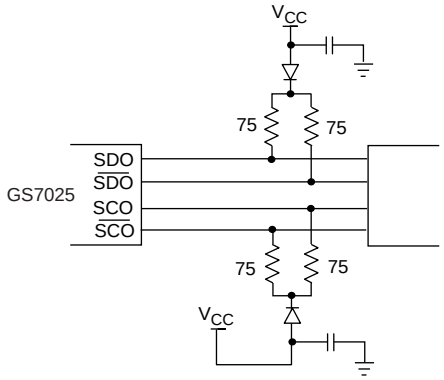
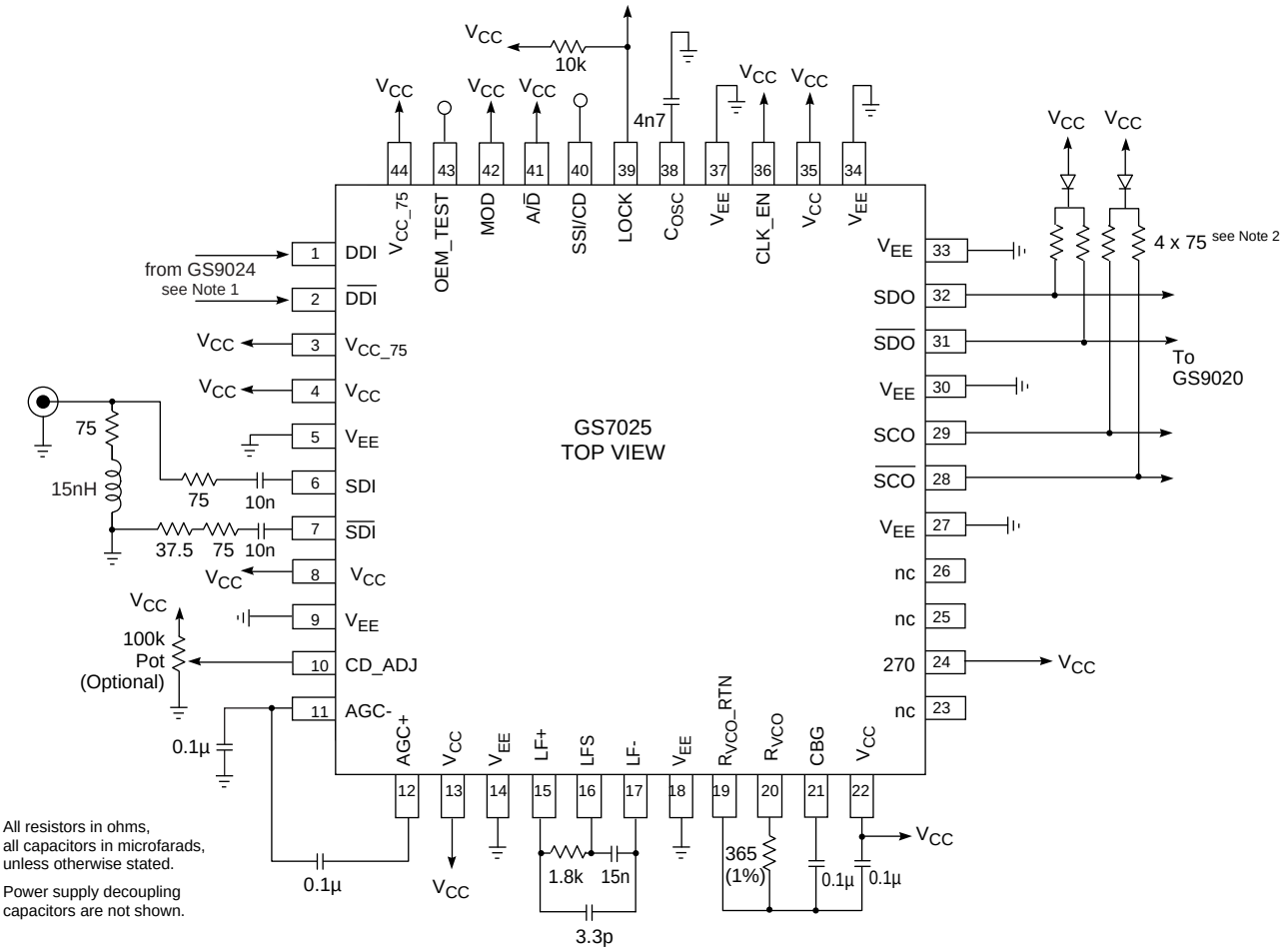


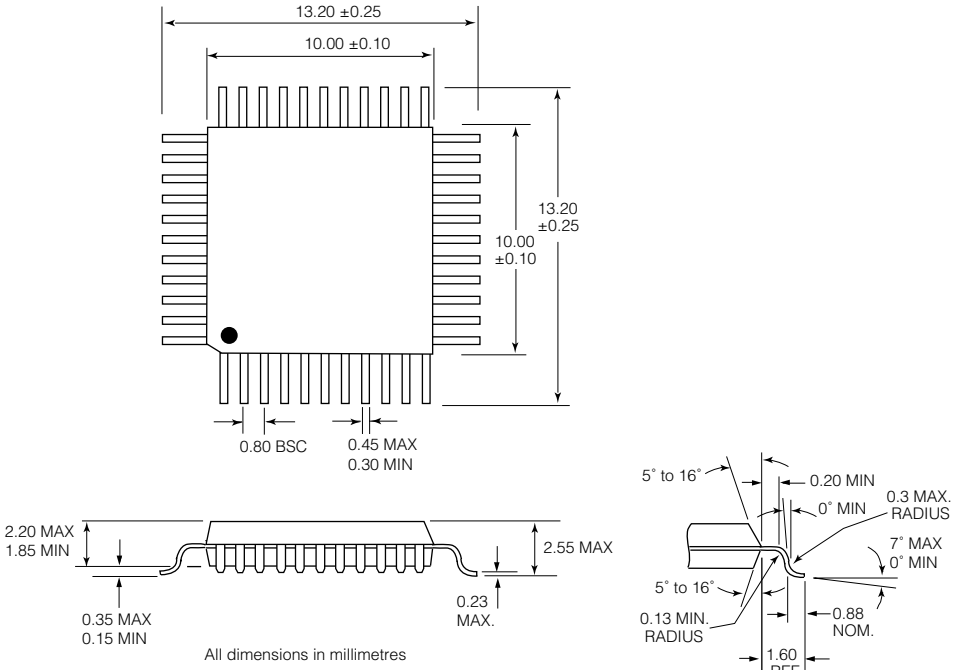
Fig. 17

TYPICAL APPLICATION CIRCUIT



NOTES
1. It is recommended that the DDI/$\overline{DDI}$ inpute are not driven when the SDI/$\overline{SDI}$ inputs are being used. This minimizes crosstalk between the DDI/$\overline{DDI}$ and SDI/$\overline{SDI}$ inputs and maximizes performance.
2. These resistors are not needed if the internal pull-up resistors on the GS9020 are used.

PACKAGE DIMENSIONS



All dimensions in millimetres

44 pin MQFP

CAUTION

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DOCUMENT IDENTIFICATION

PRELIMINARY DATA SHEET
The product is in a preproduction phase and specifications are subject to change.

REVISION NOTES:

New document.

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