MOTOROLA MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Quad 2-Input Multiplexer/ Latch

The MC10H173 is a quad 2-input multiplexer with latch. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Data Propagation Delay, 1.5 ns Typical •
- Power Dissipation, 275 mW Typical
- Voltage Compensated
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- MECL 10K–Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to V _{EE}	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	Т _А	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

154	STR.	0 °		25°		75 °		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE	_	73	_	66	_	73	mA
Inp <mark>ut Current</mark> High Pins 3–7 & 10–13 Pin 9	l _{inH}		510 475		320 300		320 300	μΑ
Input Current Low	linL	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V _{OL}	-1.95	-1.63	-1.95	-1.63	-1.9 <mark>5</mark>	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	<u>-0.81</u>	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

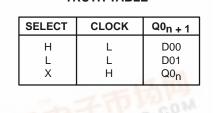
Propagation Delay Data Clock Select	^t pd	0.7 1.0 1.0	2.3 3.7 3.6	0.7 1.0 1.0	2.3 3.7 3.6	0.7 1.0 1.0	2.3 3.7 3.6	ns
Set–up Time Data Select	^t set	0.7 1.0	_	0.7 1.0	_	0.7 1.0	_	ns
Hold Time Data Select	^t hold	0.7 1.0		0.7 1.0	1	0.7 1.0	E.	ns
Rise Time	t _r	0.7	2.4	0.7	2.4	0.7	2.4	ns
Fall Time	t _f	0.7	2.4	0.7	2.4	0.7	2.4	ns

NOTE:

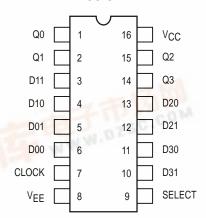
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.



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DIP **PIN ASSIGNMENT**



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).

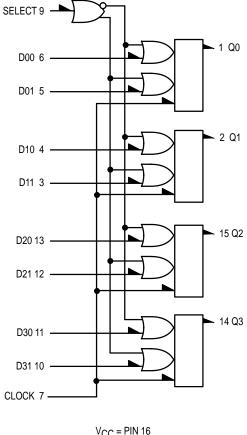




APPLICATION INFORMATION

The MC10173 is a quad two-channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input

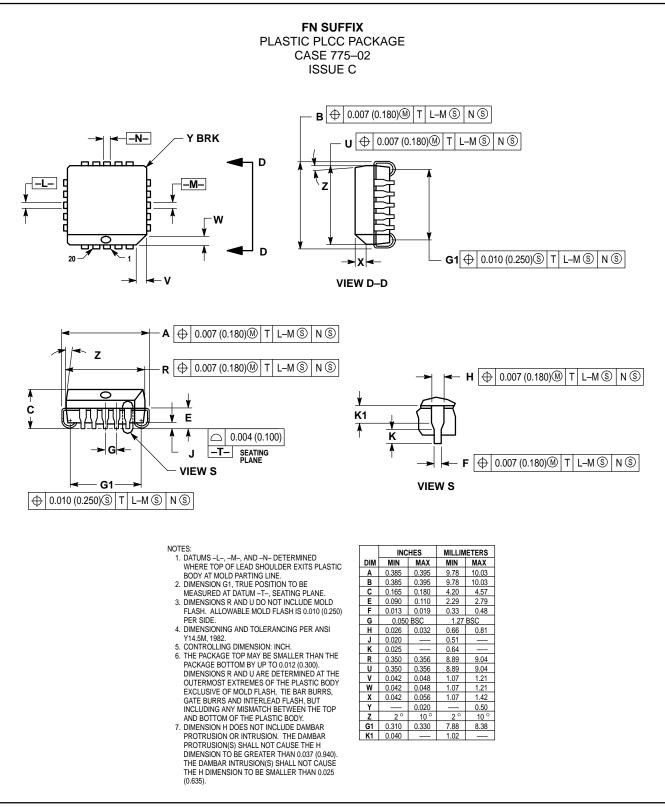
will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.



LOGIC DIAGRAM

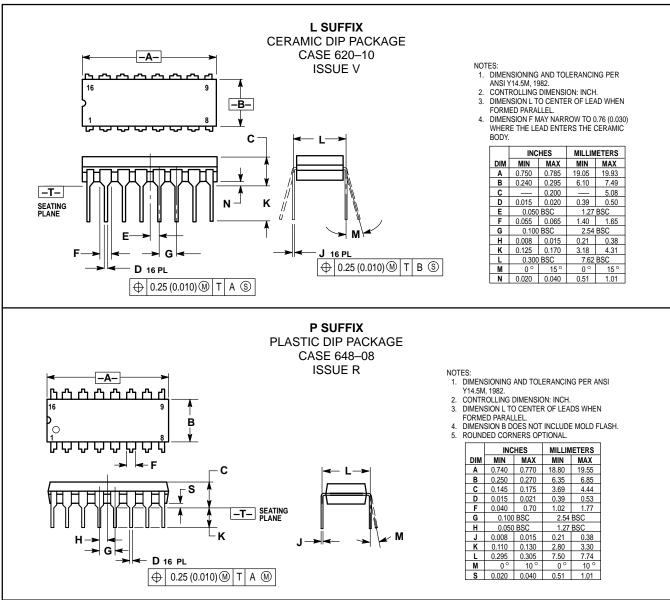
V_{CC} = PIN 16 V_{EE} = PIN 8

OUTLINE DIMENSIONS



MC10H173

OUTLINE DIMENSIONS



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