

INTEGRATED CIRCUITS

DATA SHEET

74LVC32245A; 74LVCH32245A 32-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Product specification
File under Integrated Circuits, IC24

1999 Sep 01

32-bit bus transceiver with direction pin; 5 V tolerant; 3-state

74LVC32245A; 74LVCH32245A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range of 1.2 to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-trough standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on data inputs (74LVCH32245A only)
- Typical output ground bounce voltage:
 $V_{OLP} < 0.8 \text{ V}$ at $V_{CC} = 3.3 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$
- Typical output V_{OH} undershoot voltage:
 $V_{OHV} > 2 \text{ V}$ at $V_{CC} = 3.3 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$
- Power-off disabled outputs, permitting live insertion
- Plastic fine-pitch ball grid array package.

DESCRIPTION

The 74LVC(H)32245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 and 5 V environment.

The 74LVC(H)32245A is a 32-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The 74LVC(H)32245A features two output enable (\overline{nOE}) inputs for easy cascading and two send or receive (\overline{nDIR}) inputs for direction control. \overline{nOE} controls the outputs so that the buses are effectively isolated.

To ensure the high-impedance state during power-up or power-down, input \overline{nOE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The 74LVCH32245A bus hold data inputs eliminates the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level (see Fig.2).

QUICK REFERENCE DATA

Ground = 0 V; $T_{amb} = 25 \text{ }^\circ\text{C}$; $t_r = t_f \leq 2.5 \text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA_n to nB_n ; nB_n to nA_n	$C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$	3.0	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	$V_I = \text{GND to } V_{CC}$; note 1	30	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

FUNCTION TABLE

See note 1.

INPUT		OUTPUT	
n \overline{OE}	nDIR	nA _n	nB _n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

Note

- H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC32245AEC	-40 to +85 °C	96	LFBGA96	plastic	SOT536-1
74LVCH32245AEC		96	LFBGA96	plastic	SOT536-1

PINNING

SYMBOL	DESCRIPTION
nDIR	direction control
n \overline{OE}	output enable input (active LOW)
nA _n	data inputs/outputs
nB _n	data inputs/outputs
GND	ground (0 V)
V _{CC}	DC supply voltage

32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

MNA475

6	1A ₁	1A ₃	1A ₅	1A ₇	2A ₁	2A ₃	2A ₅	2A ₆	3A ₁	3A ₃	3A ₅	3A ₇	4A ₁	4A ₃	4A ₅	4A ₆
5	1A ₀	1A ₂	1A ₄	1A ₆	2A ₀	2A ₂	2A ₄	2A ₇	3A ₀	3A ₂	3A ₄	3A ₆	4A ₀	4A ₂	4A ₄	4A ₇
4	1O $\overline{\text{E}}$	GND	V _{CC}	GND	GND	V _{CC}	GND	2O $\overline{\text{E}}$	3O $\overline{\text{E}}$	GND	V _{CC}	GND	GND	V _{CC}	GND	4O $\overline{\text{E}}$
3	1DIR	GND	V _{CC}	GND	GND	V _{CC}	GND	2DIR	3DIR	GND	V _{CC}	GND	GND	V _{CC}	GND	4DIR
2	1B ₀	1B ₂	1B ₄	1B ₆	2B ₀	2B ₂	2B ₄	2B ₇	3B ₀	3B ₂	3B ₄	3B ₆	4B ₀	4B ₂	4B ₄	4B ₇
1	1B ₁	1B ₃	1B ₅	1B ₇	2B ₁	2B ₃	2B ₅	2B ₆	3B ₁	3B ₃	3B ₅	3B ₇	4B ₁	4B ₃	4B ₅	4B ₆
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

Fig.1 Pin configuration.

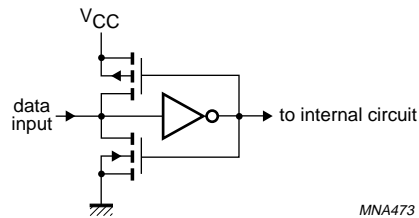


Fig.2 Bus hold circuit.

32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

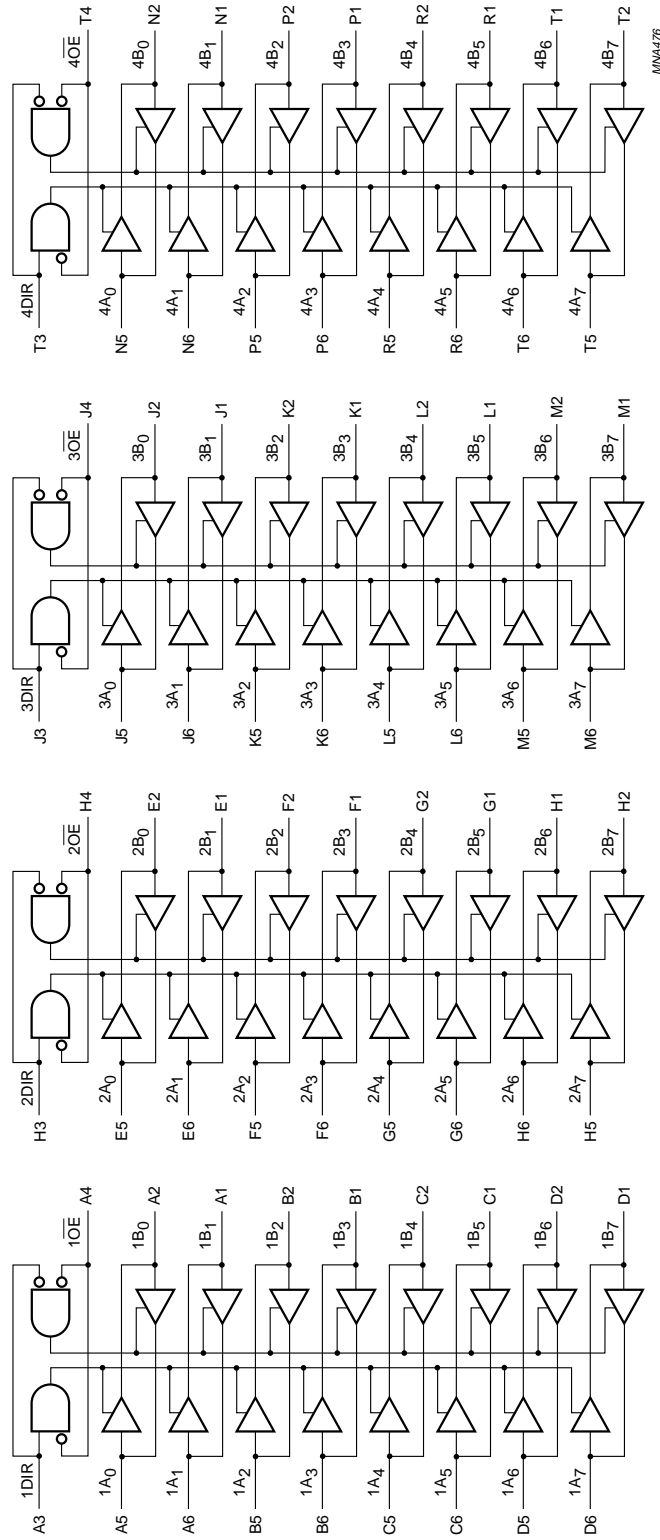


Fig.3 Logic symbol.

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74LVC32245A;
74LVCH32245A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V _{CC}	DC supply voltage	for max. speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V _I	DC input voltage		0	5.5	V
V _O	DC output voltage	output HIGH or LOW state	0	V _{CC}	V
		3-state	0	5.5	V
T _{amb}	operating ambient temperature	see DC and AC characteristics per device	-40	+85	°C
t _r , t _f (Δt/Δf)	input rise and fall times ratio	V _{CC} = 1.2 to 2.7 V	0	20	ns/V
		V _{CC} = 2.7 to 3.6 V	0	10	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	DC supply voltage		-0.5	+6.5	V
V _I	DC input voltage	note 1	-0.5	+6.5	V
I _{IK}	DC input diode current	V _I < 0	-	-50	mA
I _{OK}	DC output diode current	V _O > V _{CC} or V _O < 0; note 1	-	±50	mA
V _O	DC output voltage	output HIGH or LOW state; note 1	-0.5	V _{CC} + 0.5	V
		output 3-state; note 1	-0.5	+6.5	V
I _O	DC output source or sink current	V _O = 0 to V _{CC}	-	±50	mA
I _{CC} , I _{GND}	DC V _{CC} or GND current		-	±100	mA
T _{stg}	storage temperature		-65	+150	°C
P _D	power dissipation per package	temperature range: -40 to +85 °C; note 2	-	1000	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 70 °C the value of P_D derates linearly with 1.8 mW/K.

32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

DC CHARACTERISTICS

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)			UNIT
		OTHER	V _{CC} (V)	-40 to +85			
				MIN.	TYP. ⁽¹⁾	MAX.	
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	
V _{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –12 mA I _O = –100 μA I _O = –18 mA I _O = –24 mA	2.7	V _{CC} – 0.5	–	–	V
			3.0	V _{CC} – 0.2	V _{CC}	–	
			3.0	V _{CC} – 0.6	–	–	
			3.0	V _{CC} – 0.8	–	–	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 12 mA I _O = 100 μA I _O = 24 mA	2.7	–	–	0.40	V
			3.0	–	–	0.20	
			3.0	–	–	0.55	
I _I	input leakage current	V _I = 5.5 V or GND; note 2	3.6	–	±0.1	±5	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND	3.6	–	0.1	±5	μA
I _{off}	power off leakage supply current	V _I or V _O = 5.5 V	0.0	–	0.1	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	–	0.1	40	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} – 0.6 V; I _O = 0	2.7 to 3.6	–	5	500	μA
I _{BHL}	bus hold LOW sustaining current	V _I = 0.8 V; notes 3, 4 and 5	3.0	75	–	–	μA
I _{BHH}	bus hold HIGH sustaining current	V _I = 2.0 V; notes 3, 4 and 5	3.0	–75	–	–	μA
I _{BHLO}	bus hold LOW overdrive current	notes 3, 4 and 6	3.6	500	–	–	μA
I _{BHHO}	bus hold HIGH overdrive current	notes 3, 4 and 6	3.6	–500	–	–	μA

Notes

1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For bus hold parts the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5 V on the input terminal.
3. Valid for data inputs of bus hold parts only (LVCH32xxx-A).
4. For data inputs only. Control inputs do not have a bus hold circuit.
5. The specified sustaining current at the data input holds the input below the specified V_I level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input level.

32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

AC CHARACTERISTICS

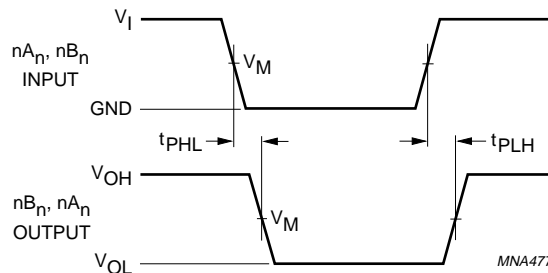
Ground = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500 \Omega$.

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb} = -40$ to $+85$ °C			UNIT
		WAVEFORMS	V_{CC} (V)	MIN.	TYP. ⁽¹⁾	MAX.	
t_{PHL}/t_{PLH}	propagation delay nA_n to nB_n ; nB_n to nA_n	see Figs 4 and 6	2.7	1.5	–	5.5	ns
			3.0 to 3.6	1.5	3.0	4.5	
t_{PZH}/t_{PZL}	3-state output enable time nOE to nA_n ; nOE to nB_n	see Figs 5 and 6	2.7	1.5	–	7.1	ns
			3.0 to 3.6	1.5	4.0	6.1	
t_{PHZ}/t_{PLZ}	3-state output disable time nOE to nA_n ; nOE to nB_n	see Figs 5 and 6	2.7	1.5	–	6.6	ns
			3.0 to 3.6	1.5	4.0	5.6	

Note

1. All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

AC WAVEFORMS

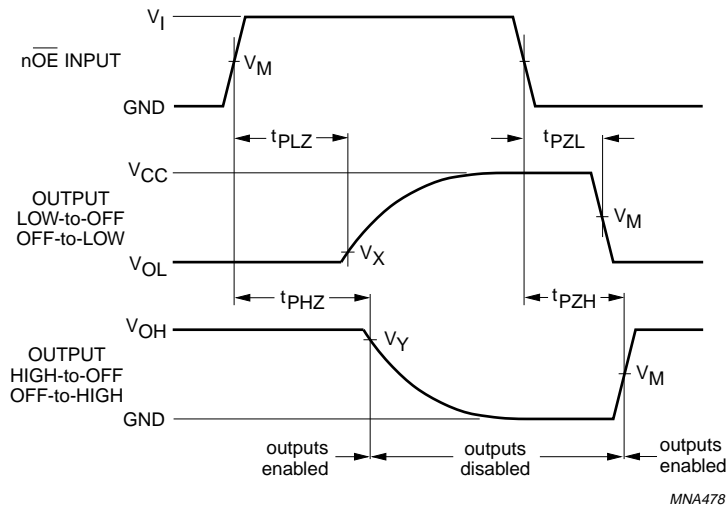


$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V or
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V.
 V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.4 Input nA_n , nB_n to output nB_n , nA_n propagation delay times.

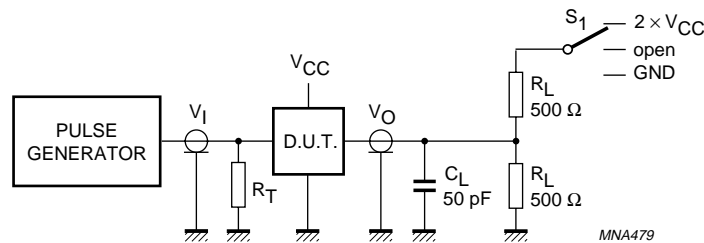
32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A



$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$ or
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$;
 $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$ or
 $V_X = V_{OL} + 0.1 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$;
 $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$ or
 $V_Y = V_{OH} - 0.1 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$;
 V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 3-state enable and disable times.



TEST	S ₁
t _{PLH} /t _{PHL}	open
t _{PLZ} /t _{PZL}	2 × V _{CC}
t _{PHZ} /t _{PZH}	GND

V _{CC}	V _I
< 2.7 V	V _{CC}
2.7 to 3.6 V	2.7 V

Definitions for test circuit:
 R_L = load resistor.
 C_L = load capacitance including jig and probe capacitance.
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

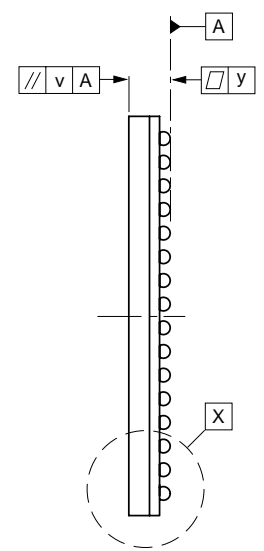
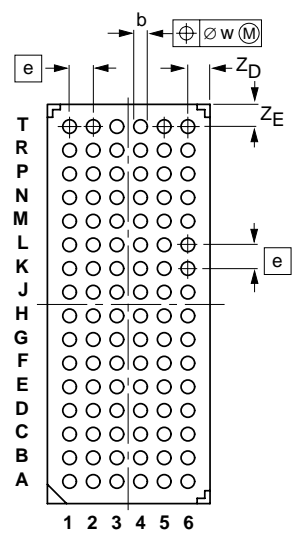
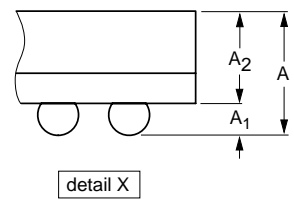
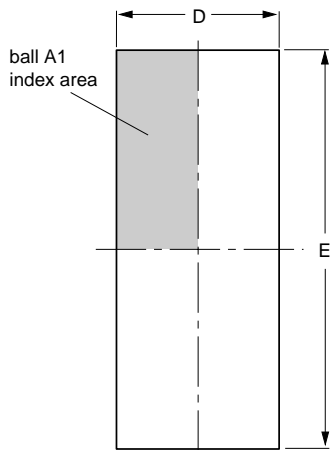
Fig.6 Load circuitry for switching times.

32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

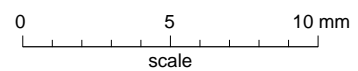
PACKAGE OUTLINE

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	b	D	E	e	v	w	y	Z _D	Z _E
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	0.2	0.15	0.1	0.93 0.58	0.93 0.58



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT536-1						-98-11-25- 99-06-03

32-bit bus transceiver with direction pin; 5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

NOTES

32-bit bus transceiver with direction pin;
5 V tolerant; 3-state

74LVC32245A;
74LVCH32245A

NOTES

32-bit bus transceiver with direction pin;
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74LVC32245A;
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