Quad CMOS to PECL* Translator

The MC10H352 is a quad translator for interfacing data between a CMOS logic section and the PECL section of digital systems when only a +5.0~Vdc power supply is available. The MC10H352 has CMOS compatible inputs and PECL complementary open—emitter outputs that allow use as an inverting/non—inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state ($\approx +3.2~\text{V}$) and all inverting outputs to the PECL high logic state ($\approx +4.1~\text{V}$).

The MC10H352 can also be used with the MC10H350 to transmit and receive CMOS information differentially via balanced twisted pair lines.

- Single +5.0 V Power Supply
- All V_{CC} Pins Isolated On Chip
- · Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical

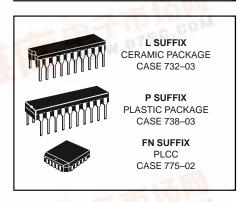
MAXIMUM RATINGS

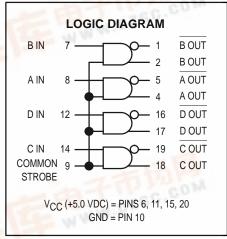
Characteristic	Symbol	Rating	Unit
Power Supply	Vcc	0 to +7.0	Vdc
Input Voltage (V _{CC} = 5.0 V)	VI	0 to V _{CC}	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	TA	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC1} = V_{CC2} = 5.0 V ± 5.0%)

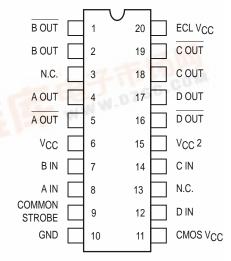
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply	ECL		50		45	1	50	mA
Current	TTL		20		15	1	20	mA
Reverse Current Pins 7, 8, 12, 14 Pin 9	I _R		25 100		20 80		25 100	μА
Forward Current Pins 7, 8, 12, 14 Pin 9	lF	-	-0.8 -3.2	_	-0.6 -2.4	=(-0.8 -3.2	mA
Input Voltage Breakdown	V _{(BR)in}	5.5	44	5.5	COM	5.5	1 m	Vdc
Input Clamp Voltage (I _{in} = -18 mA)	VI	WW	-1.5	120.	-1.5	_	-1.5	Vdc
High Output Voltage (1)	Vон	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
Low Output Voltage (1)	V _{OL}	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
High Input Voltage	VIH	3.15		3.15		3.15	_	Vdc
Low input Voltage	V _{IL}	_	1.5		1.5	_	1.5	Vdc

MC10H352





DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion
Tables on page 6–36 of the Motorola MECL Data
Book (DL122/D).

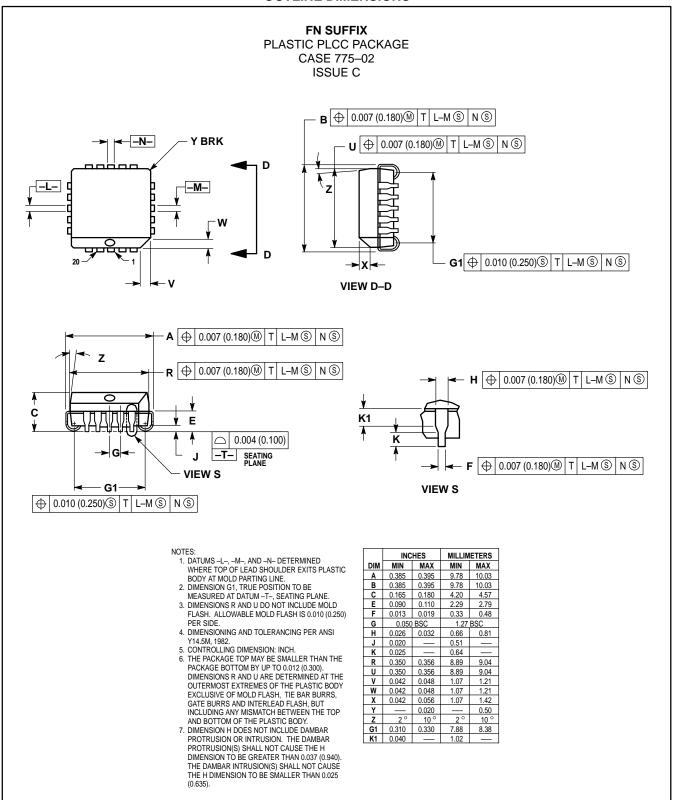
AC PARAMETERS

		0 °		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Propagation Delay (1)	t _{pd}	0.4	1.9	0.4	2.0	0.4	2.1	ns
Rise Time (20% to 80%)	t _r	0.4	1.9	0.4	2.0	0.4	2.1	ns
Fall Time (80% to 20%)	t _f	0.4	1.9	0.4	2.0	0.4	2.1	ns
Maximum Operating Frequency	f _{max}	150	_	150	_	150	_	MHz

⁽¹⁾ Propagation delay is measured on this circuit from $V_{CC}/2$ on the input waveform to the 50% point on the output waveform. **NOTE:**

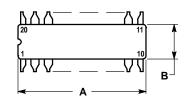
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to V_{CC} – 2.0 Vdc.

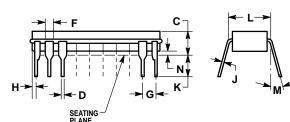
OUTLINE DIMENSIONS



OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 732-03 ISSUE E

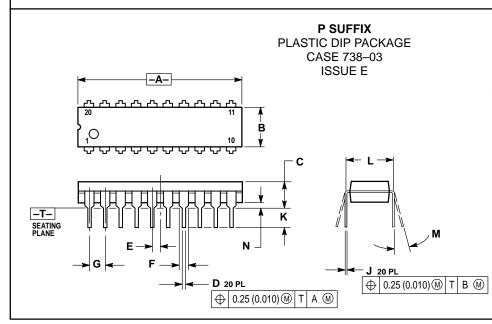




NOTES:

- 1. LEADS WITHIN 0.010 DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
- 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL. 3. DIMENSIONS A AND B INCLUDE MENISCUS.

	INCHES					
DIM	MIN MAX					
Α	0.940	0.990				
В	0.260	0.295				
С	0.150	0.200				
D	0.015	0.022				
F	0.055	0.065				
G	0.100	BSC				
Н	0.020	0.050				
J	0.008	0.012				
K	0.125	0.160				
L	0.300 BSC					
M	0°	15°				
N	0.010	0.040				



- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN
- FORMED PARALLEL.

 4. DIMENSION B DOES NOT INCLUDE MOLD

	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	1.010	1.070	25.66	27.17		
В	0.240	0.260	6.10	6.60		
С	0.150	0.180	3.81	4.57		
D	0.015	0.022	0.39	0.55		
Е	0.050 BSC		1.27 BSC			
F	0.050	0.070	1.27	1.77		
G	0.100	0.100 BSC		2.54 BSC		
J	0.008	0.015	0.21	0.38		
K	0.110	0.140	2.80	3.55		
L	0.300 BSC		7.62 BSC			
М	0°	15°	0°	15°		
N	0.020	0.040	0.51	1.01		

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