**Data Sheet**    *July 1999*    *File Number*  **3134.2**

## Quad SPST, CMOS RF/Video Switch

The IH5352 is a quad SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high OFF isolation while maintaining good frequency response in the ON condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically $t_{ON}$ = 150ns and $t_{OFF}$ = 80ns. "Break-Before-Make" switching is guaranteed.
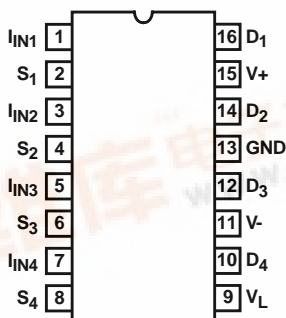
Switch ON resistance is typically 40Ω - 50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies.
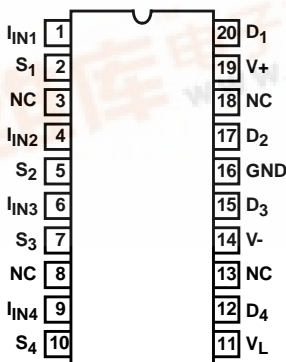
## Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| IH5352CPE | 0 to 70 | 16 Ld PDIP | E16.3 |
| IH5352CBP | 0 to 70 | 20 Ld SOIC | M20.3 |

## Pinouts

**IH5352 (PDIP) TOP VIEW**

```
I_IN1  1        16  D_1
S_1    2        15  V+
I_IN2  3        14  D_2
S_2    4        13  GND
I_IN3  5        12  D_3
S_3    6        11  V-
I_IN4  7        10  D_4
S_4    8         9  V_L
```

**IH5352 (SOIC) TOP VIEW**

```
I_IN1  1        20  D_1
S_1    2        19  V+
NC     3        18  NC
I_IN2  4        17  D_2
S_2    5        16  GND
I_IN3  6        15  D_3
S_3    7        14  V-
NC     8        13  NC
I_IN4  9        12  D_4
S_4   10        11  V_L
```

## Features

- $r_{DS(ON)}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 75Ω
- Switch Attenuation Varies Less Than 3dB From DC to 100MHz
- OFF Isolation at 10MHz . . . . . . . . . . . . . . . . . . . . >70dB
- Crosstalk Isolation at 10MHz . . . . . . . . . . . . . . . . >60dB
- Compatible With TTL, CMOS Logic
- Wide Operating Power Supply Range
- Power Supply Current . . . . . . . . . . . . . . . . . . . . . . . <1µA
- "Break-Before-Make" Switching
- Fast Switching (Typ) . . . . . . . . . . . . . . . . . . . . 80ns/150ns

## Applications

- Video Switch
- Communications Equipment
- Disk Drives
- Instrumentation
- CATV

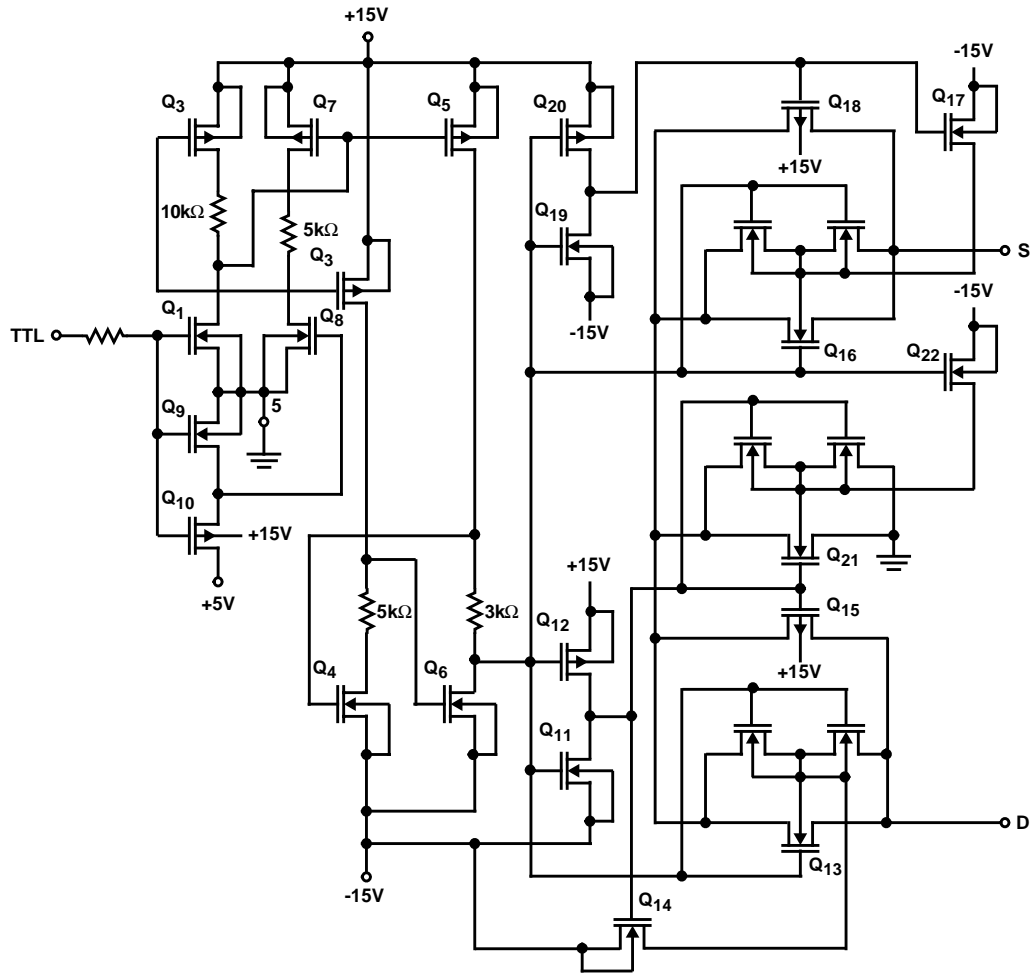## Functional Diagram

**SWITCH STATE SHOWN FOR LOGIC "0" INPUT**
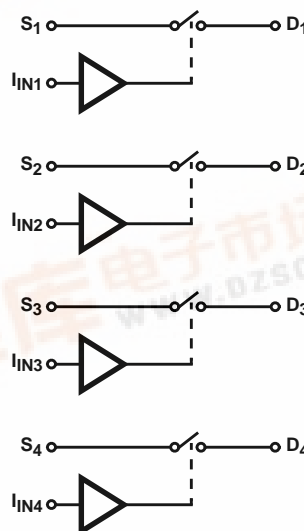


**TRUTH TABLE**

| LOGIC | SWITCHES |
|---|---|
| 0 | Off |
| 1 | On |

1

## Schematic Diagram

$^1/_4$ **IH5352**

## IH5352

### Absolute Maximum Ratings

V+ to Ground . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +18V
V- to Ground. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -18V
$V_L$ to Ground . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . V+ to V-
Logic Control Voltage. . . . . . . . . . . . . . . . . . . . . . . . . . . . . V+ to V-
Analog Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . V+ to V-
Current (Any Terminal). . . . . . . . . . . . . . . . . . . . . . . . . . . . 50mA

### Operating Conditions

Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . . . . $0^oC$ to $70^oC$
Supply Voltage Range
  V+, $V_L$. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5V to 15V
  V- . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -5V to -15V

### Thermal Information

Thermal Resistance (Typical, Note 1)         $\theta_{JA}$ ($^oC$/W)
  SOIC Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . .    90
  PDIP Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . .    90
Maximum Junction Temperature (Plastic Packages) . . . . . . .$150^oC$
Maximum Storage Temperature Range . . . . . . . . . . -$65^oC$ to $150^oC$
Maximum Lead Temperature (Soldering, 10s). . . . . . . . . . . $300^oC$
  (SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

### Electrical Specifications    V+ = +15V, $V_L$ = +5V, V- = -15V, Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | (NOTE 2) TYP $25^oC$ | (NOTE 4) $0^oC$ | (NOTE 4) $25^oC$ | (NOTE 4) $70^oC$ | UNITS |
|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn ON Time, $t_{ON}$ | Figure 1 | 150 | - | - | - | ns |
| Turn OFF Time, $t_{OFF}$ | | 80 | - | - | - | ns |
| OFF Isolation, OIRR | Figure 2 | 70 | - | - | - | dB |
| Crosstalk, CCRR | Figure 3 | -60 | - | - | - | dB |
| Switch Attenuation 3dB Frequency, $f_{3dB}$ | Figure 4 | 100 | - | - | - | MHz |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Logic "1" Input Voltage, $V_{IH}$ | | >2.4 | - | - | - | V |
| Logic "0" Input Voltage, $V_{IL}$ | | <0.8 | - | - | - | V |
| Input Logic Current, $I_{IN}$ | $V_{IN}$ > 2.4V or < 0V | 0.1 | ±1 | ±1 | 10 | μA |
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Drain-Source ON Resistance, $r_{DS(ON)}$ | $V_D = \pm5V$, $I_S = 10mA$, $V_{IN} \geq 2.4V$ | 50 | 75 | 75 | 100 | Ω |
| | $V_D = \pm10V$, $I_S = 10mA$, $V_{IN} \geq 2.4V$ | 100 | 150 | 150 | 175 | Ω |
| | V+ = $V_L$ = +5V, $V_{IN}$ = 3V, V- = -5V, $V_D = \pm3V$, $I_S = 10mA$ | 175 | 300 | 300 | 350 | Ω |
| On Resistance Match Between Channels, $\Delta r_{DS(ON)}$ | $I_S = 10mA$, $V_D = \pm5V$ | 5 | - | - | - | Ω |
| Switch OFF Leakage Current, $I_{D(OFF)}$ or $I_{S(OFF)}$ | $V_{S/D} = \pm5V$ or $\pm14V$, $V_{IN} \leq 0.8V$ (Note 3) | - | - | ±2 | 100 | nA |
| Switch ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$ | $V_{S/D} = \pm5V$ or $\pm14V$, $V_{IN} \geq 2.4V$ | - | - | ±2 | 100 | nA |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Positive Supply Quiescent Current, I+ | $V_{IN}$ = 0V or +5V | 0.1 | 1 | 1 | 10 | μA |
| Negative Supply Quiescent Current, I- | | 0.1 | 1 | 1 | 10 | μA |
| Logic Supply Quiescent Current, $I_L$ | | 0.1 | 1 | 1 | 10 | μA |

NOTES:

2. Typical values are not tested in production. They are given as a design aid only.

3. Positive and negative voltages applied to opposite sides of switch, in both directions successively.

4. Min or Max value, unless otherwise specified.

## Test Circuits and Waveforms
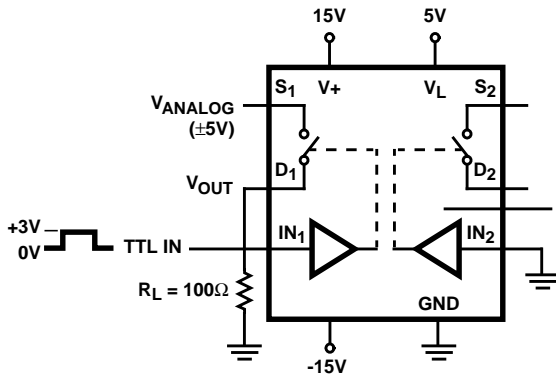


NOTE: Only one channel shown. Others act identically.
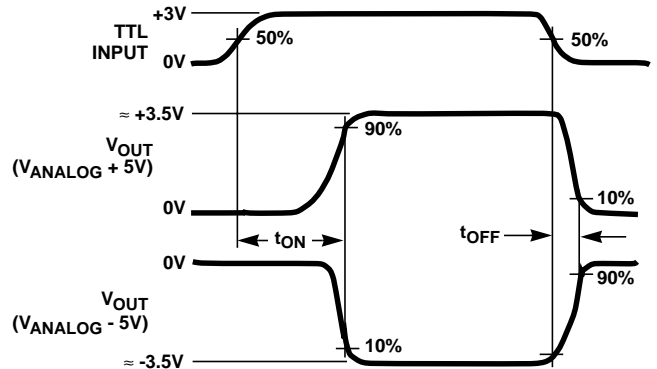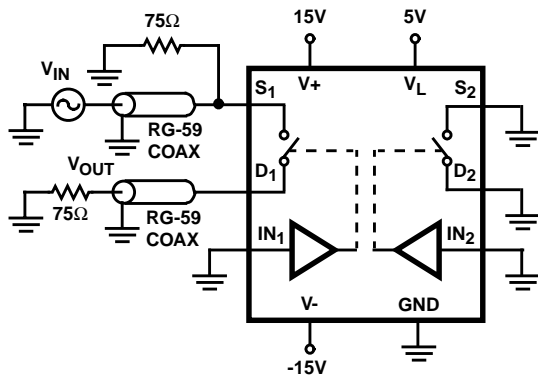
**FIGURE 1A.  TEST CIRCUIT**



**FIGURE 1B.  MEASUREMENT POINTS**

**FIGURE 1.  $t_{ON}$ AND $t_{OFF}$**


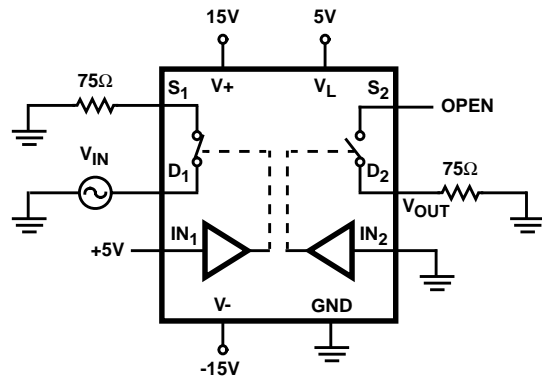
$V_{IN} = \pm 5V(10V_{P-P})$ at $f = 10MHz$

$$OIRR = 20Log \frac{V_{IN}}{V_{OUT}}$$

NOTE:   Only one channel shown. Others act identically.
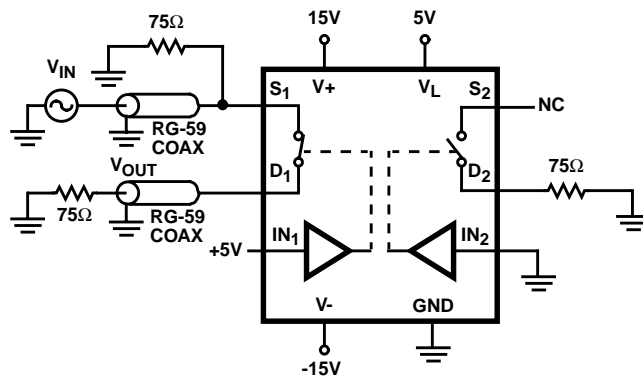
**FIGURE 2. OFF ISOLATION TEST CIRCUIT**



$V_{IN} = 225mV_{RMS}$ at $f = 10MHz$

$$CCRR = 20Log \frac{V_{OUT}}{V_{IN}}$$

**FIGURE 3.  CROSSTALK TEST CIRCUIT**



$$ATTN: = 20Log \frac{R_L}{r_{DS(ON)} + R_L}$$

Nominally, at DC, ATTN equals -4dB. When the attenuation reaches -1dB, the frequency at which this occurs is $f_{3dB}$.

NOTE:  Only one channel shown. Others act identically.

**FIGURE 4.  SWITCH ATTENUATION TEST CIRCUIT**

## Detailed Description

Figure 5 shows the internal circuit of one channel of the IH5352. Here, a shunt switch is closed, and the two series switches are open when the video switch channel is open or off. This provides much better isolation between the input and output terminals than a simple series switch does, especially at high frequencies. The result is excellent off-isolation in the Video and RF frequency ranges when compared to conventional analog switches.

The control input level shifting circuitry is very similar to that of the IH5140 series of Analog Switches, and gives very high speed, guaranteed "Break-Before-Make" action, low static power consumption and TTL compatibility.
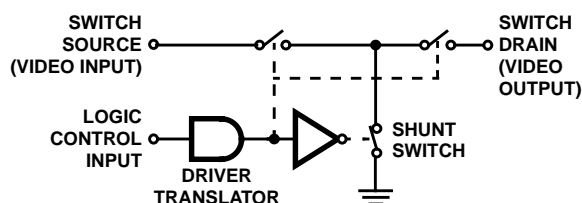


NOTE: 1 channel of 4 shown.

**FIGURE 5. INTERNAL SWITCH CONFIGURATION**

## Typical Applications

### Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5352 has a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV on a 1000pF capacitor), at $V_{S-D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 6 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1kΩ potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the -5V to +5V range.

Since individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 7. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to -5V as shown in the figure. The choice of -5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.
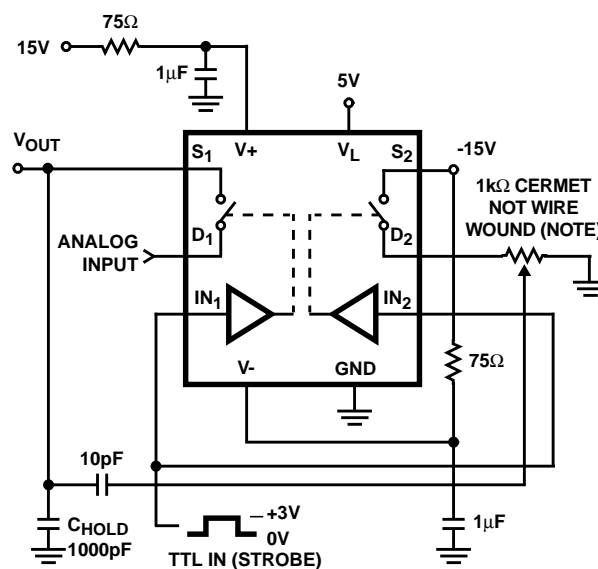


NOTE: Adjust pot for 0mV$_{P-P}$ step at V$_{OUT}$ with no analog (AC) signal present.
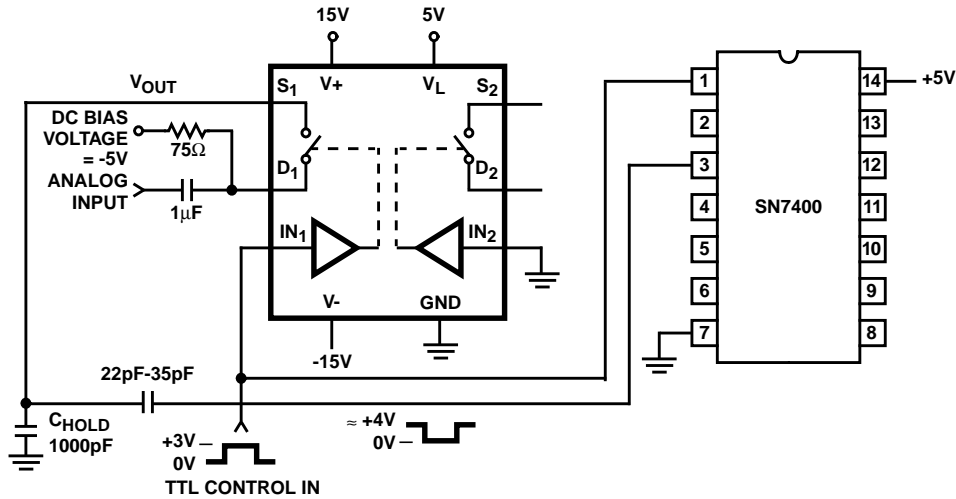
**FIGURE 6. CHARGE INJECTION COMPENSATION**

**FIGURE 7. ALTERNATIVE COMPENSATION CIRCUIT**

### *Overvoltage Protection*

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5352. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5352.

The same method of protection will provide over ±25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 8.
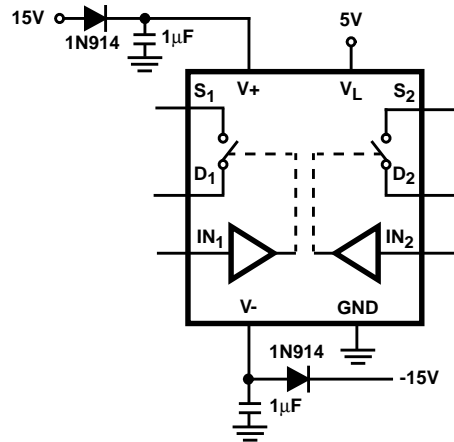


**FIGURE 8. OVERVOLTAGE PROTECTION**

## *Typical Performance Curves*
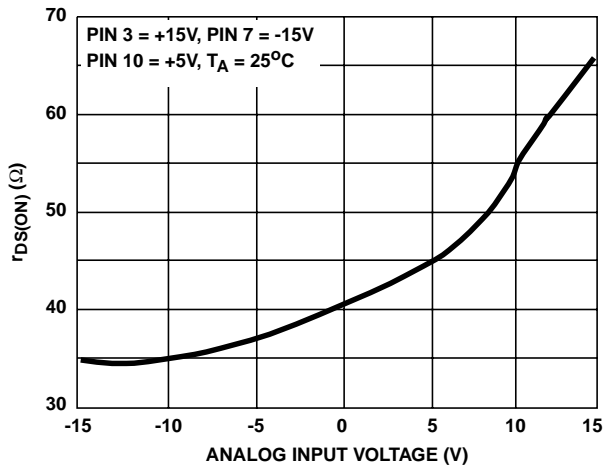


FIGURE 9. r$_{DS(ON)}$ vs ANALOG INPUT VOLTAGE WITH ±15V POWER SUPPLIES
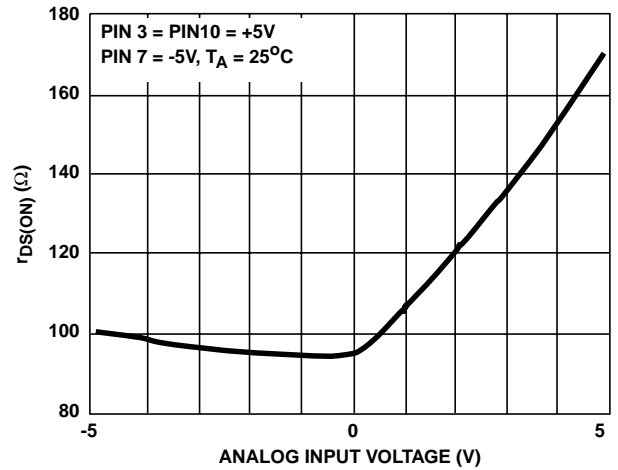


FIGURE 10. r$_{DS(ON)}$ vs ANALOG INPUT LEVEL WITH ±5V POWER SUPPLIES
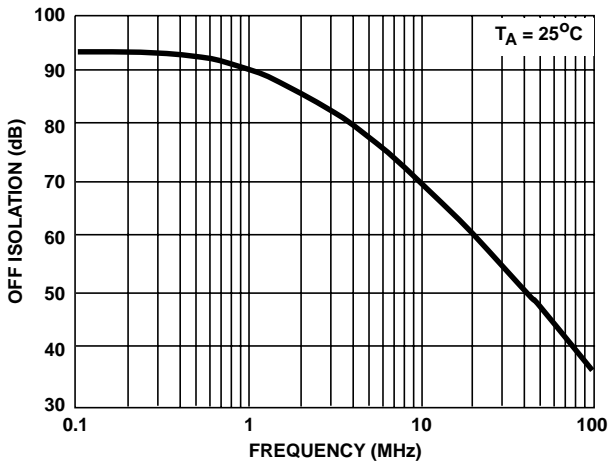


FIGURE 11. OFF ISOLATION vs FREQUENCY (SEE FIGURE 2)
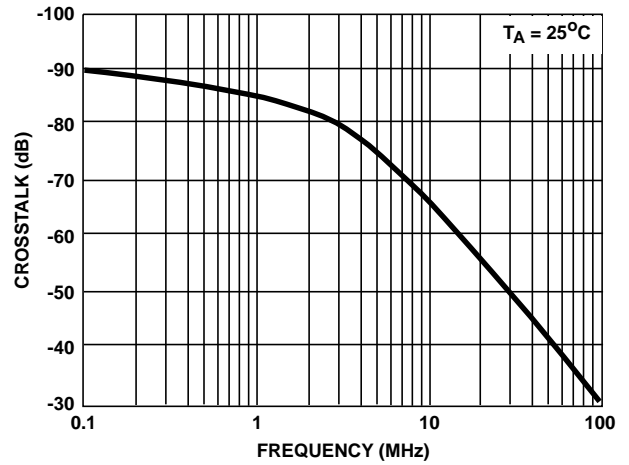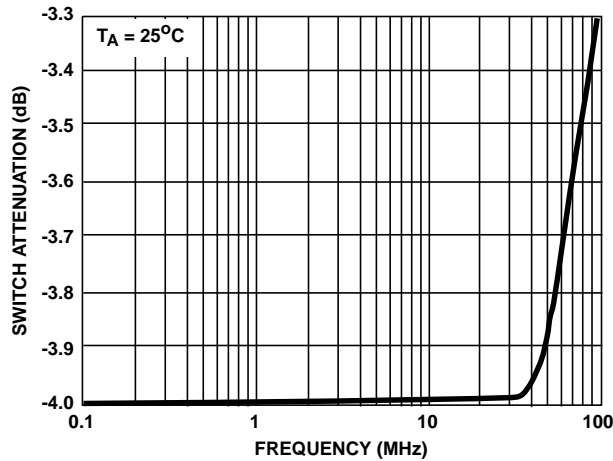


FIGURE 12. CROSSTALK vs FREQUENCY (SEE FIGURE 3)



FIGURE 13. SWITCH ATTENUATION vs FREQUENCY (R$_L$ = 75$\Omega$, SEE FIGURE 4)

## Die Characteristics

**DIE DIMENSIONS:**

2617μm x 5233μm

**METALLIZATION:**

Type: Al
Thickness: 10kÅ ±1kÅ

**PASSIVATION:**

Type: PSG/Nitride
PSG Thickness: 7kÅ ±1.4kÅ
Nitride Thickness: 8kÅ ±1.2kÅ

**WORST CASE CURRENT DENSITY:**

9.1 x $10^4$ A/cm$^2$

## Metallization Mask Layout

**IH5352**

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**