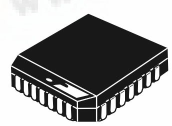
PECL/TTL-TTL 1:8 Clock Distribution Chip

MC10H646
MC100H646

PENTIUM MICROPROCESSOR PECL/TTL–TTL CLOCK DRIVER



FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

The MC10H/100H646 is a single supply, low skew translating 1:8 clock driver. Devices in the Motorola H600 translator series utilize the 28–lead PLCC for optimal power pinning, signal flow through and electrical performance. The single supply H646 is similar to the H643, which is a dual supply 1:8 version of the same function.

- PECL/TTL–TTL Version of Popular ECLinPS™ E111
- Low Skew
- Guaranteed Skew Spec
- Tri–State Enable
- Differential Internal Design
- V_{BB} Output
- Single Supply
- Extra TTL and ECL Power/Ground Pins
- Matched High and Low Output Impedance
- Meets Specifications Required to Drive the Pentium™ Microprocessor

The H646 was designed specifically to drive series terminated transmission lines. Special techniques were used to match the HIGH and LOW output impedances to about 7ohms. This simplifies the choice of the termination resistor for series terminated applications. To match the HIGH and LOW output impedances, it was necessary to remove the standard I_{OS} limiting resistor. As a result, the user should take care in preventing an output short to ground as the part will be permanently damaged.

The H646 device meets all of the requirements for driving the 60 and 66MHz Pentium Microprocessor. The device has no PLL components, which greatly simplifies its implementation into a digital design. The eight copies of the clock allows for point–to–point clock distribution to simplify board layout and optimize signal integrity.

The H646 provides differential PECL inputs for picking up LOW skew PECL clocks from the backplane and distributing it to TTL loads on a daughter board. When used in conjunction with the MC10/100E111, very low skew, very wide clock trees can be designed. In addition, a TTL level clock input is provided for flexibility. Note that only one of the inputs can be used on a single chip. For correct operation, the unused input pins should be left open.

The Output Enable pin forces the outputs into a high impedance state when a logic 0 is applied.

The output buffers of the H646 can drive two series terminated, 50Ω transmission lines each. This capability allows the H646 to drive up to 16 different point–to–point clock loads. Refer to the Applications section for a more detailed discussion in this area.

The 10H version is compatible with MECL 10H™ ECL logic levels. The 100H version is compatible with 100K levels.

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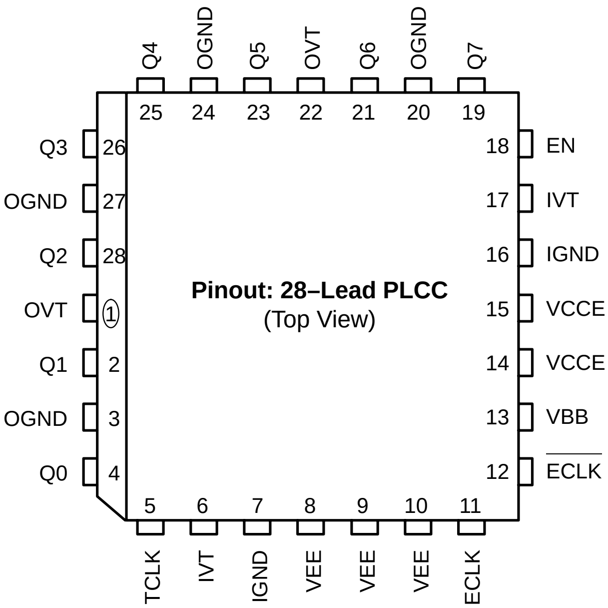
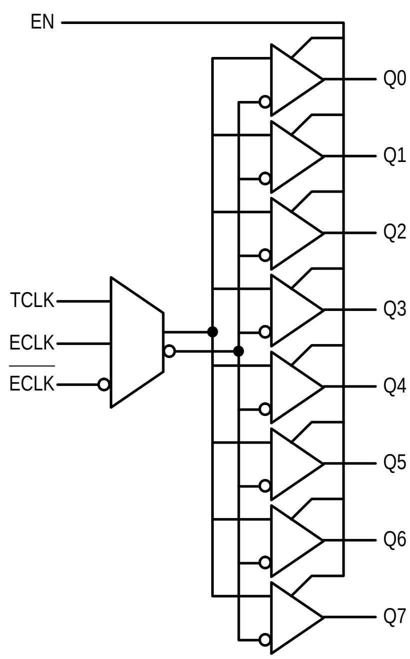


Pinout: 28–Lead PLCC
(Top View)

PIN NAMES

PIN	FUNCTION
OGND	TTL Output Ground (0V)
OVT	TTL Output V_{CC} (+5.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL V_{CC} (+5.0V)
V_{EE}	ECL V_{EE} (0V)
V_{CCE}	ECL Ground (5.0V)
ECLK, $\overline{ECLK}$	Differential Signal Input (PECL)
V_{BB}	V_{BB} Reference Output
Q0–Q7	Signal Outputs (TTL)
EN	Tri–State Enable Input (TTL)

LOGIC DIAGRAM



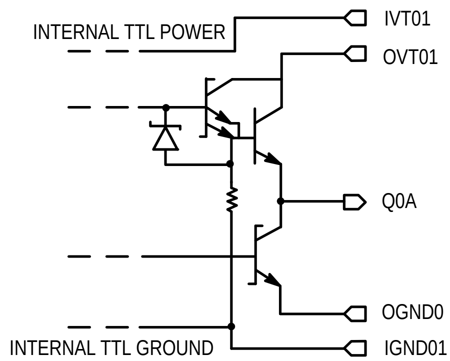


Figure 1. Output Structure

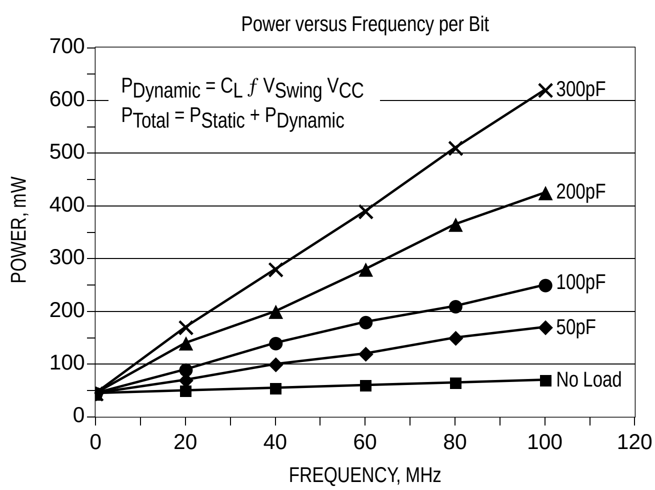


Figure 2. Power versus Frequency (Typical)

TRUTH TABLE

TCLK	ECLK	$\overline{ECLK}$	EN	Q
GND	L	H	H	L
GND	H	L	H	H
H	GND	GND	H	H
L	GND	GND	H	L
X	X	X	L	Z

L = Low Voltage Level; H = High Voltage Level; Z = Tristate

DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.6	– –	2.6	– –	2.6	– –	V	I_{OH} = 24mA
V_{OL}	Output LOW Voltage	–	0.5	–	0.5	–	0.5	V	I_{OL} = 48mA
IOS	Output Short Circuit Current	–	–	–	–	–	–	mA	See Note **1**

1. The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting IOS resistor.

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

10H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			175			175	µA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA	
V_{IH}	Input HIGH Voltage	3.83		4.16	3.87		4.19	3.94		4.28	V	IVT = IVO = VCCE = 5.0V (**1**)
V_{IL}	Input LOW Voltage	3.05		3.52	3.05		3.52	3.05		3.555	V	IVT = IVO = VCCE = 5.0V (**1**)
V_{BB}	Output Reference Voltage	3.62		3.73	3.65		3.75	3.69		3.81	V	IVT = IVO = VCCE = 5.0V (**1**)

100H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			175			175	µA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA	
V_{IH}	Input HIGH Voltage	3.835		4.12	3.835		4.12	3.835		3.835	V	IVT = IVO = VCCE = 5.0V (**1**)
V_{IL}	Input LOW Voltage	3.19		3.525	3.19		3.525	3.19		3.525	V	IVT = IVO = VCCE = 5.0V (**1**)
V_{BB}	Output Reference Voltage	3.62		3.74	3.62		3.74	3.62		3.74	V	IVT = IVO = VCCE = 5.0V (**1**)

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to VCCE and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = VCCE = 5.0V

DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
I_{CCL}	Power Supply Current		185		166	185		185	mA	Total all OVT, IVT, and VCCE pins
I_{CCH}			175		154	175		175	mA	
I_{CCZ}			210			210		210		

AC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	ECLK to Q TCLK to Q	4.8 5.1	5.8 6.4	5.0 5.3	6.0 6.4	5.6 5.7	6.6 7.0	ns	
t_{PHL}	Propagation Delay	ECLK to Q TCLK to Q	4.4 4.7	5.4 6.0	4.4 4.8	5.4 5.9	4.8 5.2	5.8 6.5	ns	
$t_{SK(O)}$	Output Skew	Q0, Q3, Q4, Q7 Q1, Q2, Q5 Q0–Q7		350 350 500		350 350 500		350 350 500	ps	Note 1, 6
$t_{SK(PR)}$	Process Skew	ECLK to Q TCLK to Q		1.0 1.3		1.0 1.1		1.0 1.3	ns	Note 2, 6
$t_{SK(P)}$	Pulse Skew	$\Delta t_{PLH} - t_{PHL}$		1.0		1.0		1.0	ns	
t_r, t_f	Rise/Fall Time		0.3	1.5	0.3	1.5	0.3	1.5	ns	
t_{PW}	Output Pulse Width	66MHz @ 2.0V 66MHz @ 0.8V 60MHz @ 2.0V 60MHz @ 0.8V	5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		ns	Note 3, 6
$t_{Stability}$	Clock Stability			±75		±75		±75	ps	Note 4, 6
F_{MAX}	Maximum Input Frequency			80		80		80	MHz	Note 5, 6

1. Output skew defined for identical output transitions.
2. Process skew is valid for V_{CC} = 5.0V ±5%.
3. Parameters guaranteed by $t_{SK(P)}$ and t_r, t_f specification limits.
4. Clock stability is the period variation between two successive rising edges.
5. For series terminated lines. See Applications section for F_{MAX} enhancement techniques.
6. All AC specifications tested driving 50Ω series terminated transmission lines at 80MHz.

OUTLINE DIMENSIONS

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PLASTIC PLCC PACKAGE
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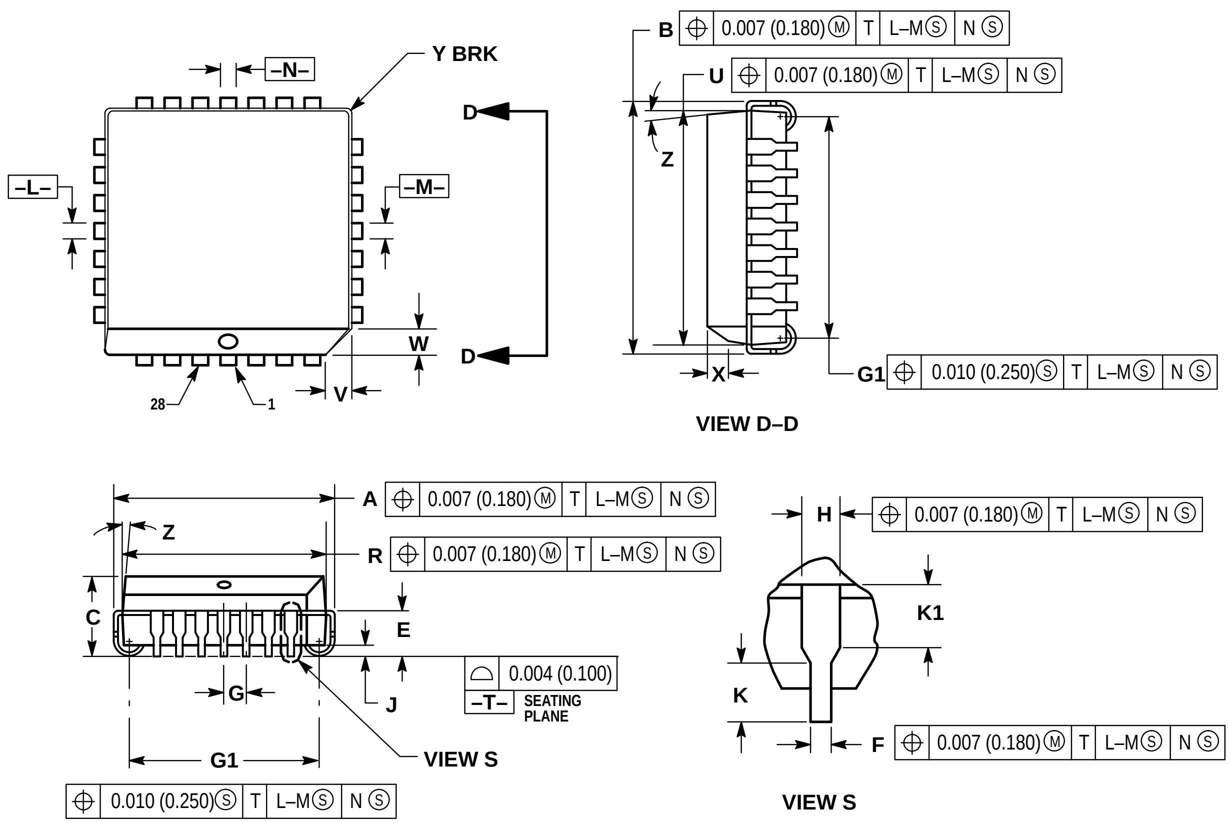
ISSUE D



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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INTERNET: http://www.mot.com/sps/

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center,
3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

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