## PECL／TTL－TTL 1：8 Clock Distribution Chip

The MC10H／100H646 is a single supply，low skew translating 1：8 clock driver．Devices in the Motorola H600 translator series utilize the 28－lead PLCC for optimal power pinning，signal flow through and electrical performance．The single supply H646 is similar to the H643，which is a dual supply $1: 8$ version of the same function．
－PECL／TTL－TTL Version of Popular ECLinPSTM E111
－Low Skew
－Guaranteed Skew Spec
－Tri－State Enable
－Differential Internal Design
－VBB Output
－Single Supply
－Extra TTL and ECL Power／Ground Pins
－Matched High and Low Output Impedance
－Meets Specifications Required to Drive the Pentium ${ }^{\text {TM }}$ Microprocessor

The H646 was designed specifically to drive series terminated transmission lines．Special techniques were used to match the HIGH and LOW output impedances to about 7ohms．This simplifies the choice of the termination resistor for series terminated applications．To match the HIGH and LOW output impedances，it was necessary to remove the standard IOS limiting resistor．As a result，the user should take care in preventing an output short to ground as the part will be permanently damaged．

The H646 device meets all of the requirements for driving the 60 and 66 MHz Pentium Microprocessor．The device has no PLL components，which greatly simplifies its implementation into a digital design．The eight copies of the clock allows for point－to－point clock distribution to simplify board layout and optimize signal integrity．

The H646 provides differential PECL inputs for picking up LOW skew PECL clocks from the backplane and distributing it to TTL loads on a daughter board．When used in conjunction with the MC10／100E111，very low skew，very wide clock trees can be designed．In addition，a TTL level clock input is provided for flexibility．Note that only one of the inputs can be used on a single chip．For correct operation，the unused input pins should be left open．

The Output Enable pin forces the outputs into a high impedance state when a logic 0 is applied．
The output buffers of the H646 can drive two series terminated， $50 \Omega$ transmission lines each．This capability allows the H 646 to drive up to 16 different point－to－point clock loads．Refer to the Applications section for a more detailed discussion in this area．

The 10 H version is compatible with MECL $10 \mathrm{H}^{\mathrm{TM}}$ ECL logic levels．The 100 H version is compatible with 100 K levels．

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PIN NAMES

| PIN | FUNCTION |
| :---: | :---: |
| OGND | TTL Output Ground (0V) |
| OVT | TTL Output $\mathrm{V}_{\mathrm{CC}}(+5.0 \mathrm{~V})$ |
| IGND | Internal TTL GND (0V) |
| IVT | Internal TTL $\mathrm{V}_{\text {CC }}(+5.0 \mathrm{~V})$ |
| $V_{\text {EE }}$ | ECL $\mathrm{V}_{\mathrm{EE}}(0 \mathrm{~V})$ |
| $V_{\text {CCE }}$ | ECL Ground (5.0V) |
| ECLK, ECLK | Differential Signal Input (PECL) |
| $\mathrm{V}_{\mathrm{BB}}$ | $\mathrm{V}_{\text {BB }}$ Reference Output |
| Q0-Q7 | Signal Outputs (TTL) |
| EN | Tri-State Enable Input (TTL) |



Figure 1. Output Structure


Figure 2. Power versus Frequency (Typical)

TRUTH TABLE

| TCLK | ECLK | ECLK | EN | Q |
| :---: | :---: | :---: | :---: | :---: |
| GND | L | H | H | L |
| GND | H | L | H | H |
| H | GND | GND | H | H |
| L | GND | GND | H | L |
| X | X | X | L | Z |

L = Low Voltage Level; H = High Voltage Level; Z = Tristate

DC CHARACTERISTICS (IVT $=$ OVT $=$ VCCE $=5.0 \mathrm{~V} \pm 5 \%$ )

| Symbol | Characteristic | $0^{\circ} \mathrm{C}$ |  | $25^{\circ} \mathrm{C}$ |  | $85^{\circ} \mathrm{C}$ |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max | Min | Max |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage | 2.6 | - | 2.6 | - | 2.6 | - | V | $\mathrm{IOH}=24 \mathrm{~mA}$ |
| VOL | Output LOW Voltage | - | 0.5 | - | 0.5 | - | 0.5 | V | $\mathrm{IOL}=48 \mathrm{~mA}$ |
| IOS | Output Short Circuit Current | - | - | - | - | - | - | mA | See Note 1 |

1. The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting IOS resistor.

TTL DC CHARACTERISTICS (VT = VE = 5.0 V $\pm 5 \%$ )

| Symbol | Characteristic | $0^{\circ} \mathrm{C}$ |  | $25^{\circ} \mathrm{C}$ |  | $85^{\circ} \mathrm{C}$ |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max | Min | Max |  |  |
| $\begin{aligned} & \hline \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | Input HIGH Voltage Input LOW Voltage | 2.0 | 0.8 | 2.0 | 0.8 | 2.0 | 0.8 | V |  |
| IIH | Input HIGH Current |  | $\begin{gathered} 20 \\ 100 \end{gathered}$ |  | $\begin{gathered} 20 \\ 100 \end{gathered}$ |  | $\begin{gathered} 20 \\ 100 \end{gathered}$ | $\mu \mathrm{A}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=2.7 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IN}}=7.0 \mathrm{~V} \end{aligned}$ |
| IIL | Input LOW Current |  | -0.6 |  | -0.6 |  | -0.6 | mA | $\mathrm{V}_{\mathrm{IN}}=0.5 \mathrm{~V}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage | $\begin{aligned} & 2.5 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 2.5 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 2.5 \\ & 2.0 \end{aligned}$ |  | V | $\begin{aligned} & \mathrm{IOH}=-3.0 \mathrm{~mA} \\ & \mathrm{IOH}=-24 \mathrm{~mA} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Output LOW Voltage |  | 0.5 |  | 0.5 |  | 0.5 | V | $\mathrm{l} \mathrm{OL}=24 \mathrm{~mA}$ |
| $\mathrm{V}_{\text {IK }}$ | Input Clamp Voltage |  | -1.2 |  | -1.2 |  | -1.2 | V | $\mathrm{I}_{\mathrm{N}}=-18 \mathrm{~mA}$ |
| los | Output Short Circuit Current | -100 | -225 | -100 | -225 | -100 | -225 | mA | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ |

10H PECL DC CHARACTERISTICS (IVT = OVT $=$ VCCE $=5.0 \mathrm{~V} \pm 5 \%$ )

| Symbol | Characteristic | $0^{\circ} \mathrm{C}$ |  |  | $25^{\circ} \mathrm{C}$ |  |  | $85^{\circ} \mathrm{C}$ |  |  | Unit | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |  |
| $\mathrm{I}_{\mathrm{IH}}$ | Input HIGH Current |  |  | 225 |  |  | 175 |  |  | 175 | $\mu \mathrm{A}$ |  |
| IIL | Input LOW Current | 0.5 |  |  | 0.5 |  |  | 0.5 |  |  | $\mu \mathrm{A}$ |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Input HIGH Voltage | 3.83 |  | 4.16 | 3.87 |  | 4.19 | 3.94 |  | 4.28 | V | $\begin{aligned} & \text { IVT }=\mathrm{IVO}= \\ & \mathrm{VCCE}=5.0 \mathrm{~V} \end{aligned}$ |
| VIL | Input LOW Voltage | 3.05 |  | 3.52 | 3.05 |  | 3.52 | 3.05 |  | 3.555 | V | $\begin{aligned} & \mathrm{IVT}=\mathrm{IVO}= \\ & \mathrm{VCCE}=5.0 \mathrm{~V}(\mathbf{1}) \end{aligned}$ |
| $\mathrm{V}_{\mathrm{BB}}$ | Output Reference Voltage | 3.62 |  | 3.73 | 3.65 |  | 3.75 | 3.69 |  | 3.81 | V | $\begin{aligned} & \text { IVT }=\mathrm{IVO}= \\ & \mathrm{VCCE}=5.0 \mathrm{~V} \end{aligned}$ |

100H PECL DC CHARACTERISTICS (IVT = OVT = VCCE $=5.0 \mathrm{~V} \pm 5 \%$ )

| Symbol | Characteristic | $0^{\circ} \mathrm{C}$ |  |  | $25^{\circ} \mathrm{C}$ |  |  | $85^{\circ} \mathrm{C}$ |  |  | Unit | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |  |
| $\mathrm{l}_{\mathrm{IH}}$ | Input HIGH Current |  |  | 225 |  |  | 175 |  |  | 175 | $\mu \mathrm{A}$ |  |
| $\mathrm{I}_{\text {IL }}$ | Input LOW Current | 0.5 |  |  | 0.5 |  |  | 0.5 |  |  | $\mu \mathrm{A}$ |  |
| $\mathrm{V}_{\text {IH }}$ | Input HIGH Voltage | 3.835 |  | 4.12 | 3.835 |  | 4.12 | 3.835 |  | 3.835 | V | $\begin{aligned} & \mathrm{IVT}=\mathrm{IVO}= \\ & \mathrm{VCCE}=5.0 \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\text {IL }}$ | Input LOW Voltage | 3.19 |  | 3.525 | 3.19 |  | 3.525 | 3.19 |  | 3.525 | V | $\begin{aligned} & \mathrm{IVT}=\mathrm{IVO}= \\ & \mathrm{VCCE}=5.0 \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\text {BB }}$ | Output Reference Voltage | 3.62 |  | 3.74 | 3.62 |  | 3.74 | 3.62 |  | 3.74 | V | $\begin{aligned} & \mathrm{IVT}=\mathrm{IVO}= \\ & \mathrm{VCCE}=5.0 \mathrm{~V}(1) \end{aligned}$ |

[^0]DC CHARACTERISTICS (IVT $=$ OVT $=$ VCCE $=5.0 \mathrm{~V} \pm 5 \%$ )

| Symbol | Characteristic | $0^{\circ} \mathrm{C}$ |  | $25^{\circ} \mathrm{C}$ |  |  | $85^{\circ} \mathrm{C}$ |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Typ | Max | Min | Max |  |  |
| ${ }^{\text {I CCL }}$ | Power Supply Current |  | 185 |  | 166 | 185 |  | 185 | mA | Total all OVT, IVT, and VCCE pins |
| ${ }^{\text {ICCH }}$ |  |  | 175 |  | 154 | 175 |  | 175 | mA |  |
| ${ }^{\text {I CCZ }}$ |  |  | 210 |  |  | 210 |  | 210 |  |  |

AC CHARACTERISTICS (IVT $=$ OVT $=$ VCCE $=5.0 \mathrm{~V} \pm 5 \%$ )

| Symbol | Characteristic |  | $0^{\circ} \mathrm{C}$ |  | $25^{\circ} \mathrm{C}$ |  | $85^{\circ} \mathrm{C}$ |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max | Min | Max | Min | Max |  |  |
| tPLH | Propagation Delay | ECLK to Q TCLK to Q | $\begin{aligned} & \hline 4.8 \\ & 5.1 \end{aligned}$ | $\begin{aligned} & \hline 5.8 \\ & 6.4 \end{aligned}$ | $\begin{aligned} & \hline 5.0 \\ & 5.3 \end{aligned}$ | $\begin{aligned} & \hline 6.0 \\ & 6 . \end{aligned}$ | $\begin{aligned} & 5.6 \\ & 5.7 \end{aligned}$ | $\begin{aligned} & 6.6 \\ & 7.0 \end{aligned}$ | ns |  |
| tPHL | Propagation Delay | ECLK to Q TCLK to Q | $\begin{aligned} & 4.4 \\ & 47 \end{aligned}$ | $\begin{aligned} & 5.4 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 4.4 \\ & 4.8 \end{aligned}$ | $\begin{aligned} & 5.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 4.8 \\ & 5.2 \end{aligned}$ | $\begin{aligned} & 5.8 \\ & 6.5 \end{aligned}$ | ns |  |
| tSK(0) | Output Skew | $\begin{array}{r} \text { Q0, Q3, Q4, Q7 } \\ \text { Q1, Q2, Q5 } \\ \text { Q0-Q7 } \end{array}$ |  | $\begin{aligned} & 350 \\ & 350 \\ & 500 \end{aligned}$ |  | $\begin{aligned} & 350 \\ & 350 \\ & 500 \end{aligned}$ |  | $\begin{aligned} & 350 \\ & 350 \\ & 500 \end{aligned}$ | ps | Note 1, 6 |
| tsk(PR) | Process Skew | ECLK to Q TCLK to Q |  | $\begin{aligned} & 1.0 \\ & 1.3 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 1.1 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 1.3 \end{aligned}$ | ns | Note 2, 6 |
| tSK(P) | Pulse Skew | $\Delta$ tPLH - tphL |  | 1.0 |  | 1.0 |  | 1.0 | ns |  |
| $\mathrm{t}_{\mathrm{r}, \mathrm{t}} \mathrm{t}_{\mathrm{f}}$ | Rise/Fall Time |  | 0.3 | 1.5 | 0.3 | 1.5 | 0.3 | 1.5 | ns |  |
| tPW | Output Pulse Width | $\begin{aligned} & 66 \mathrm{MHz} @ 2.0 \mathrm{~V} \\ & 66 \mathrm{MHz} @ 0.8 \mathrm{~V} \\ & 60 \mathrm{MHz} @ 2.0 \mathrm{~V} \\ & 60 \mathrm{MHz} @ 0.8 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 5.5 \\ & 5.5 \\ & 6.0 \\ & 6.0 \end{aligned}$ |  | $\begin{aligned} & \hline 5.5 \\ & 5.5 \\ & 6.0 \\ & 6.0 \end{aligned}$ |  | $\begin{aligned} & 5.5 \\ & 5.5 \\ & 6.0 \\ & 6.0 \end{aligned}$ |  | ns | Note 3, 6 |
| ${ }^{\text {tstability }}$ | Clock Stability |  |  | $\pm 75$ |  | $\pm 75$ |  | $\pm 75$ | ps | Note 4, 6 |
| $\mathrm{F}_{\text {MAX }}$ | Maximum Input Freq |  |  | 80 |  | 80 |  | 80 | MHz | Note 5, 6 |

1. Output skew defined for identical output transitions.
2. Process skew is valid for $\mathrm{V}_{\mathrm{C}}=5.0 \mathrm{~V} \pm 5 \%$.
3. Parameters guaranteed by $\mathrm{t}_{\mathrm{SK}}(\mathrm{P})$ and $\mathrm{t}_{\mathrm{r}}$, $\mathrm{t}_{\mathrm{f}}$ specification limits.
4. Clock stability is the period variation between two successive rising edges.
5. For series terminated lines. See Applications section for FMAX enhancement techniques.
6. All AC specifications tested driving $50 \Omega$ series terminated transmission lines at 80 MHz .

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE D


VIEW D-D


| $\theta$ | $0.010(0.250)(\mathrm{S}$ | T | L-M (S) | N (S) |
| :--- | :--- | :--- | :--- | :--- |



VIEW S

NOTES:

1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR
PROTRUSION(S) SHALL NOT CAUSE THE H PROTRUSION(S) SHALL NOT CAUSE THE H
DIMENSION TO BE GREATER THAN 0.037 DIMENSION TO BE GREATER THAN 0.037
(0.940). THE DAMBAR INTRUSION(S) SHALL ( 0.940 ). THE DAMBAR INTRUSION(S) SH
NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 ( 0.635 ).

|  | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | 1.27 BSC |  |  |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | - | 0.51 | - |
| K | 0.025 | - | 0.64 | - |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | - | 0.020 | - | 0.50 |
| Z | $2^{\circ}$ | $10^{\circ}$ | $2^{\circ}$ | $10^{\circ}$ |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | - | 1.02 | - |


#### Abstract

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[^0]:    1. $E C L V_{I H}, V_{I L}$ and $V_{B B}$ are referenced to VCCE and will vary $1: 1$ with the power supply. The levels shown are for $\operatorname{IVT}=\mathrm{IVO}=\mathrm{VCCE}=5.0 \mathrm{~V}$
