intersil

HA2546/883

Wideband Two Quadrant Analog Multiplier (Voltage Output)

July 1994

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Speed Voltage Output. . . . . 300V/µs (Min)
- Low Multiplication Error . . . . . .3.0% (Max)
  1.6% (Typ)
- Input Bias Currents . . . . . 5µA (Max)
  1.2µA (Typ)
- Signal Input Feedthrough . . . . . .-52dB (Typ)
- Wide Signal Bandwidth . . . . . 30MHz (Typ)
- Wide Control Bandwidth . . . . . 17MHz (Typ)
- Gain Flatness to 5MHz. . . . . .0.10dB (Typ)

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Description

The HA-2546/883 is a monolithic, high speed, two quadrant, analog multiplier constructed in the Intersil Dielectrically Isolated High Frequency Process. The HA-2546/883 has a voltage output with a 30MHz signal bandwidth, 300V/µs slew rate and a 17MHz control input bandwidth. High bandwidth and slew rate make this part an ideal component for use in video systems. The suitability for precision video applications is demonstrated further by the 0.1dB gain flatness at 5MHz, 1.6% multiplication error, -52dB feedthrough and differential inputs with 1.2µA bias currents. The HA-2546/883 also has low differential gain (0.1% typ.) and phase (0.1^{o} typ.) errors.

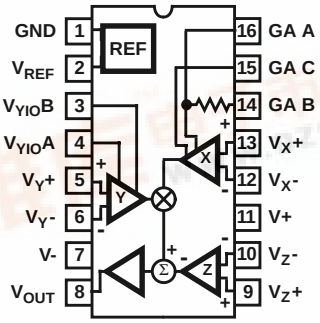
The HA-2546/883 is well suited for AGC circuits as well as mixer applications for sonar, radar, and medical imaging equipment. The voltage output of the HA-2546/883 simplifies many designs by eliminating the current-to-voltage conversion stage required for current output multipliers.

Ordering Information

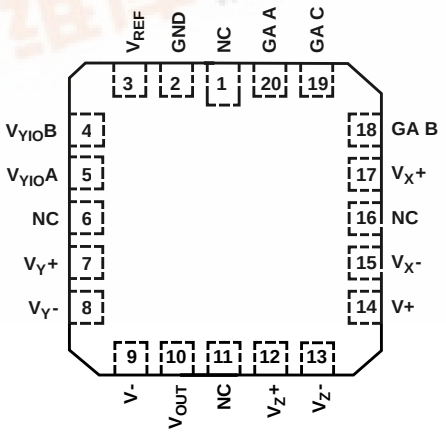
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-2546/883	-55^{o}C to +125^{o}C	16 Lead CerDIP
HA4-2546/883	-55^{o}C to +125^{o}C	20 Lead Ceramic LCC

Pinouts

HA-2546/883
(CERDIP)
TOP VIEW



HA-2546/883
(CLCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- 35V
Differential Input Voltage 6V
Output Current 60mA
Junction Temperature . . . . . +175^{o}C
Storage Temperature Range . . . . . -65^{o}C ≤ T_A ≤ +150^{o}C
ESD Rating . . . . . <2000V
Lead Temperature (Soldering 10s) . . . . . +300^{o}C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	80^{o}C/W	25^{o}C/W
Ceramic LCC	61^{o}C/W	12^{o}C/W

Maximum Package Power Dissipation
CerDIP Package at +75^{o}C 1.25W
Ceramic LCC Package at +75^{o}C 1.64W
Package Power Dissipation Derating Factor above +75^{o}C
CerDIP Package . . . . . 12mW/^{o}C
Ceramic LCC Package . . . . . 16mW/^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -55^{o}C to +125^{o}C
Operating Supply Voltage . . . . . ±8V to ±15V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±15V, R_{LOAD} = 1kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Multiplication Error	ME	V_Y = ±5V	1	+25^{o}C	-3	3	%FS
			2, 3	+125^{o}C, -55^{o}C	-5	5	%FS
Scale Factor Error	SF		1	+25^{o}C	-5	5	%
			2, 3	+125^{o}C, -55^{o}C	-5	5	%
Common Mode Range	+CMR		1	+25^{o}C	5	-	V
			2, 3	+125^{o}C, -55^{o}C	5	-	V
	-CMR		1	+25^{o}C	-	-5	V
			2, 3	+125^{o}C, -55^{o}C	-	-5	V
Input Offset Voltage (V_Y)	$V_{IO}(V_Y)$	V_{CM} = 0V	1	+25^{o}C	-10	10	mV
			2, 3	+125^{o}C, -55^{o}C	-15	15	mV
Input Bias Current (V_Y)	$I_B(V_Y)$	V_{CM} = 0V	1	+25^{o}C	-15	15	µA
			2, 3	+125^{o}C, -55^{o}C	-20	20	µA
Input Offset Current (V_Y)	$I_{IO}(V_Y)$	V_{CM} = 0V	1	+25^{o}C	-2	2	µA
			2, 3	+125^{o}C, -55^{o}C	-3	3	µA
Common Mode (V_Y) Rejection Ratio	+CMRR(V_Y)	V_Y = 0 to +5V, V_X = +2V	1	+25^{o}C	60	-	dB
			2, 3	+125^{o}C, -55^{o}C	60	-	dB
	-CMRR(V_Y)	V_Y = 0 to -5V, V_X = +2V	1	+25^{o}C	60	-	dB
			2, 3	+125^{o}C, -55^{o}C	60	-	dB
Input Offset Voltage (V_X)	$V_{IO}(V_X)$	V_{CM} = 0V	1	+25^{o}C	-2	2	mV
			2, 3	+125^{o}C, -55^{o}C	-15	15	mV
Input Bias Current (V_X)	$I_B(V_X)$	V_{CM} = 0V	1	+25^{o}C	-2	2	µA
			2, 3	+125^{o}C, -55^{o}C	-5	5	µA
Input Offset Current (V_X)	$I_{IO}(V_X)$	V_{CM} = 0V	1	+25^{o}C	-2	2	µA
			2, 3	+125^{o}C, -55^{o}C	-3	3	µA
Input Offset Voltage (V_Z)	$V_{IO}(V_Z)$	V_X = 0V, V_Y = 0V	1	+25^{o}C	-15	15	mV
			2, 3	+125^{o}C, -55^{o}C	-15	15	mV
Output Voltage Swing	$+V_{OUT}$	V_Y = +5V, V_X = +2.5V	1	+25^{o}C	5	-	V
			2, 3	+125^{o}C, -55^{o}C	5	-	V
	$-V_{OUT}$	V_Y = -5V, V_X = +2.5V	1	+25^{o}C	-	-5	V
			2, 3	+125^{o}C, -55^{o}C	-	-5	V
Output Current	$+I_{OUT}$	V_Y = +5V, V_X = +2.5V	1	+25^{o}C	20	-	mA
			2, 3	+125^{o}C, -55^{o}C	20	-	mA
	$-I_{OUT}$	V_Y = -5V, V_X = +2.5V	1	+25^{o}C	-	-20	mA
			2, 3	+125^{o}C, -55^{o}C	-	-20	mA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{SUPPLY} = ±15V, R_{LOAD} = 1kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Power Supply Rejection Ratio	+PSRR	ΔV_S = 3V, V+ = +15V, V- = -15V, V+ = +12V, V- = -15V	1	+25°C	58	-	dB
			2, 3	+125°C, -55°C	58	-	dB
	-PSRR	ΔV_S = 3V, V+ = +15V, V- = -15V, V+ = +15V, V- = -12V	1	+25°C	58	-	dB
			2, 3	+125°C, -55°C	58	-	dB
Quiescent Power Supply Current	$+I_{CC}$	$V_X = V_Y$ = 0V, I_{OUT} = 0mA	1	+25°C	29	-	mA
			2, 3	+125°C, -55°C	29	-	mA
	$-I_{CC}$	$V_X = V_Y$ = 0V, I_{OUT} = 0mA	1	+25°C	-	-29	mA
			2, 3	+125°C, -55°C	-	-29	mA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See AC Specifications in Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±15V, R_{LOAD} = 1kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -5V to +5V, $V_X = 2V_{DC}$	1	+25°C	300	-	V/µs
			1	+125°C, -55°C	300	-	V/µs
	-SR	V_{OUT} = +5V to -5V, $V_X = 2V_{DC}$	1	+25°C	300	-	V/µs
			1	+125°C, -55°C	300	-	V/µs
Rise and Fall Time	TR	V_{OUT} = -100mV to +100mV $V_X = 2V_{DC}$	1, 3	+25°C	-	15	ns
			1, 3	+125°C, -55°C	-	17	ns
	TF	V_{OUT} = +100mV to -100mV $V_X = 2V_{DC}$	1, 3	+25°C	-	15	ns
			1, 3	+125°C, -55°C	-	17	ns
Overshoot	+OS	V_{OUT} = -100mV to +100mV $V_X = 2V_{DC}$	1	+25°C	-	30	%
			1	+125°C, -55°C	-	30	%
	-OS	V_{OUT} = +100mV to -100mV $V_X = 2V_{DC}$	1	+25°C	-	30	%
			1	+125°C, -55°C	-	30	%
Full Power Bandwidth	FPBW	V_{PEAK} = 5V, $V_X = 2V_{DC}$	1, 2	+25°C	9.5	-	MHz
			1, 2	+125°C, -55°C	9.5	-	MHz

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Measured between 10% and 90% points.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1(Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
79.9mils x 119.7mils x 19mils ± 1mils

METALLIZATION:
Type: Al, 1%Cu
Thickness: 16kÅ ± 2kÅ

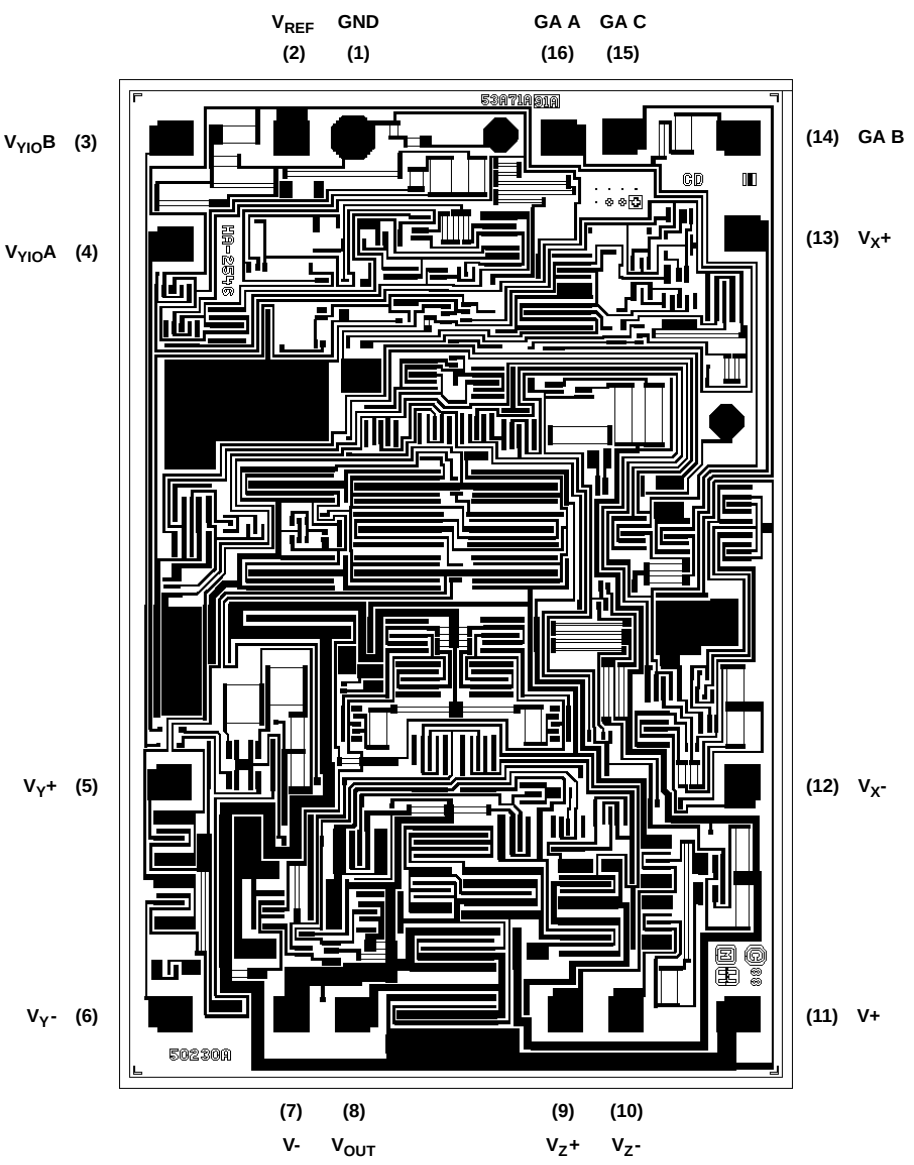
GLASSIVATION:
Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ± 1.5kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:
0.72×10^5 A/cm^2

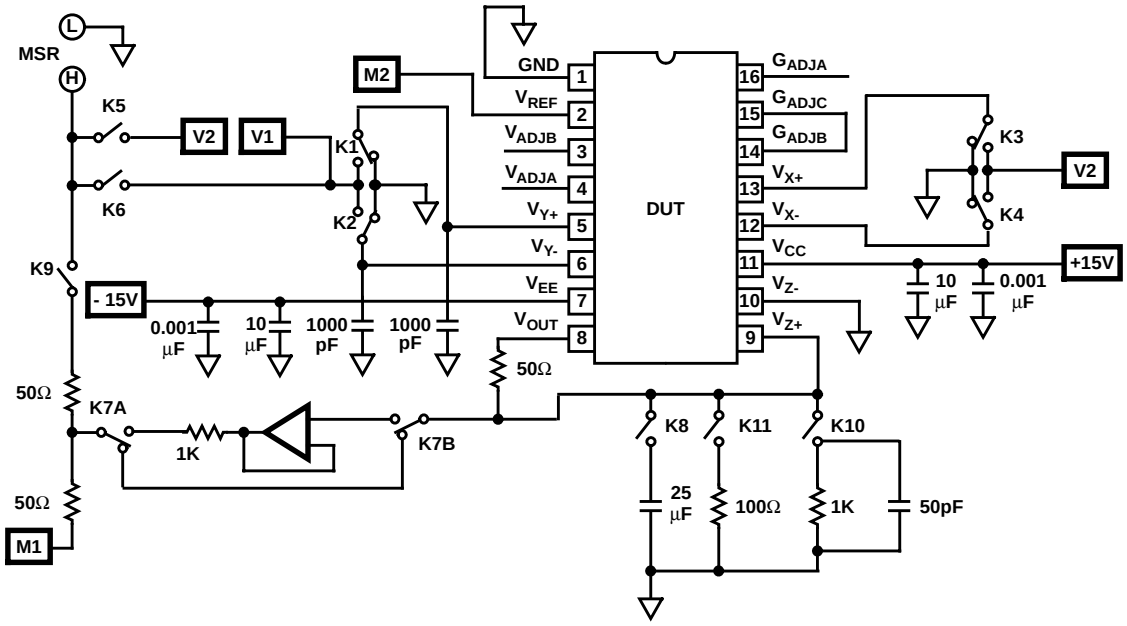
TRANSISTOR COUNT: 87

Metallization Mask Layout

HA-2546/883



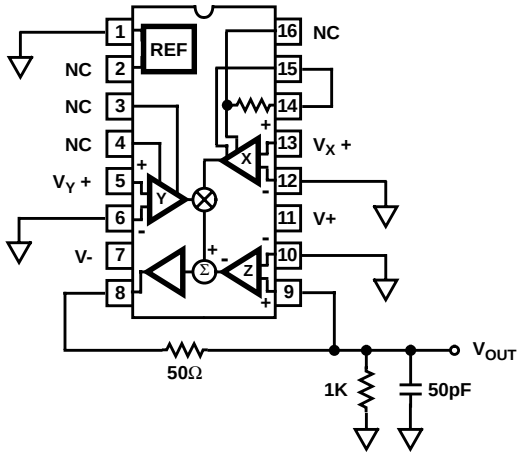
Test Circuit



For Detailed Information, Refer to HA-2546/883 Test Tech Brief

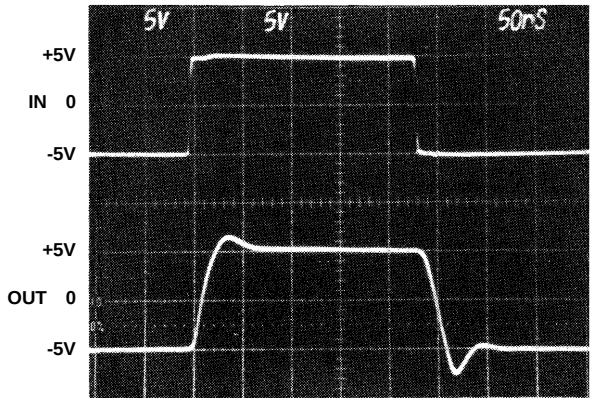
Test Waveforms

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

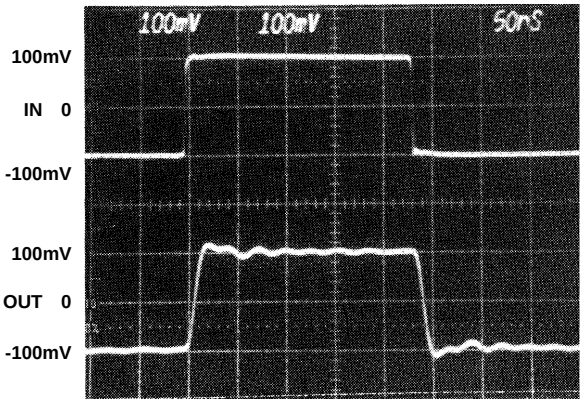


Test Waveforms (Continued)

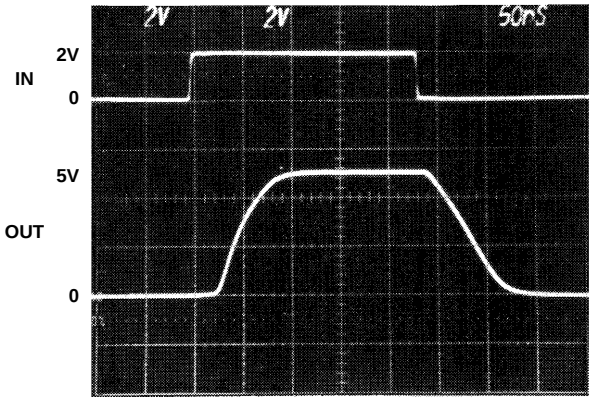
V_Y LARGE SIGNAL RESPONSE
Vertical Scale: 5V/Div. Horizontal Scale: 50ns/Div.



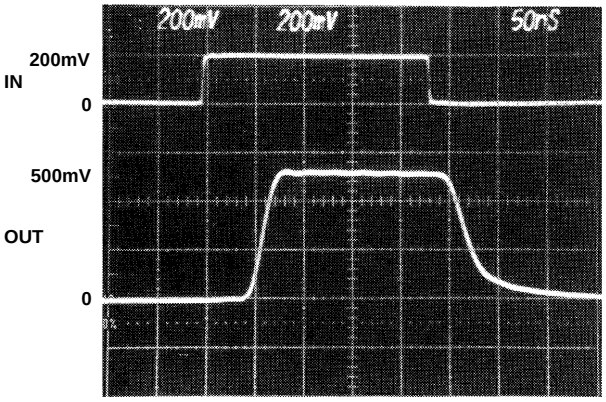
V_Y SMALL SIGNAL RESPONSE
Vertical Scale: 100mV/Div. Horizontal Scale: 50ns/Div.



V_X LARGE SIGNAL RESPONSE
Vertical Scale: 2V/Div. Horizontal Scale: 50ns/Div.

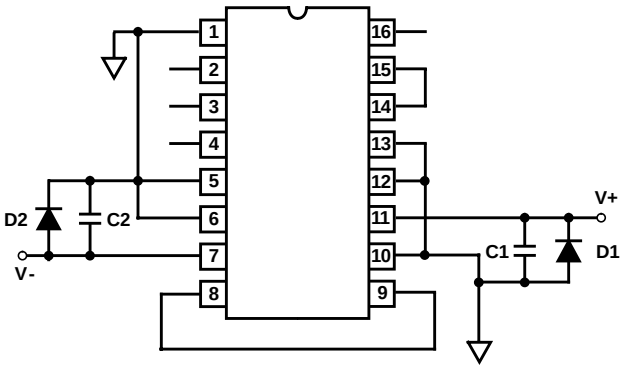


V_X SMALL SIGNAL RESPONSE
Vertical Scale: 200mV/Div. Horizontal Scale: 50ns/Div.



Burn-In Circuits

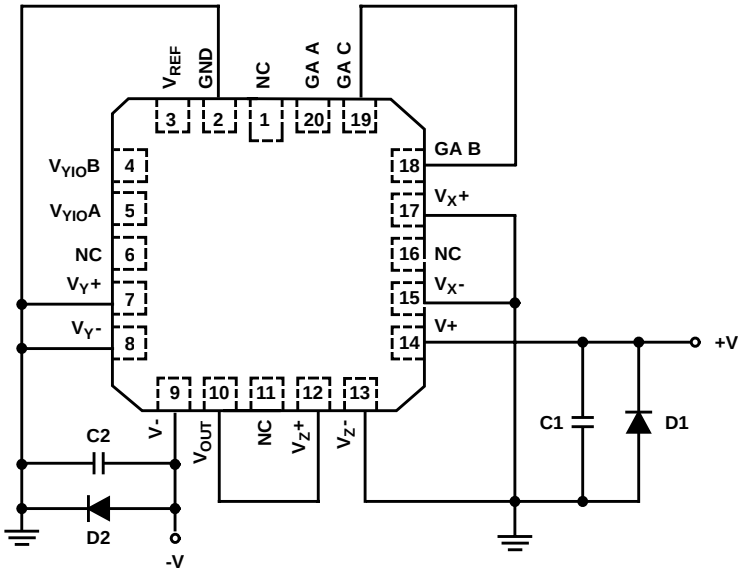
HA-2546/883 CERDIP



NOTES:

C1 = 0.01µF/Socket Min.
C2 = 0.01µF/Socket Min.
D1 = D2 = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 31V \pm 1V$

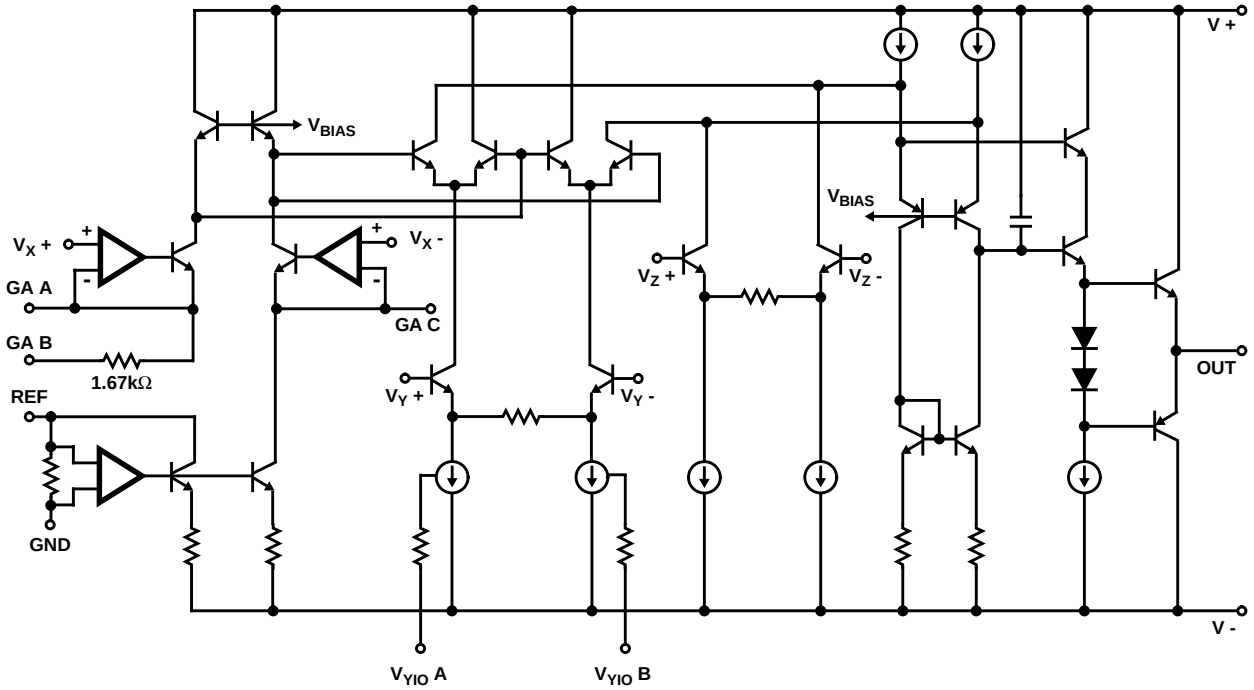
HA-2546/883 CERAMIC LCC



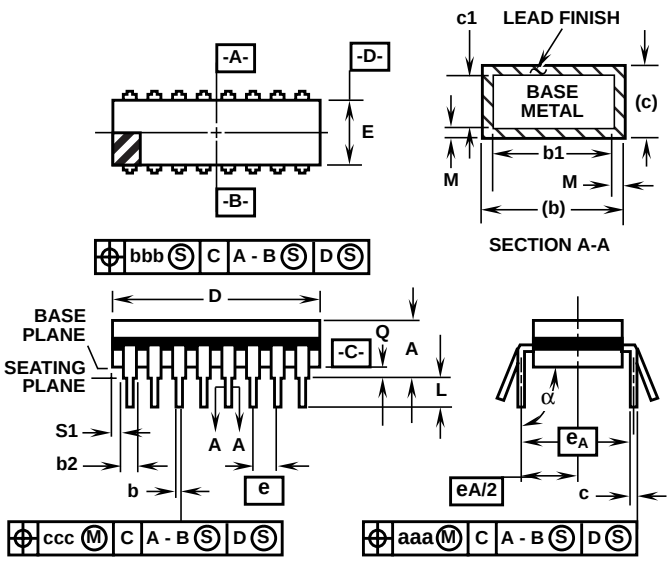
NOTES:

C1 = C2 = 0.01µF/Socket Min.
D1 = D2 = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 31V \pm 1V$

Simplified Schematic



Packaging



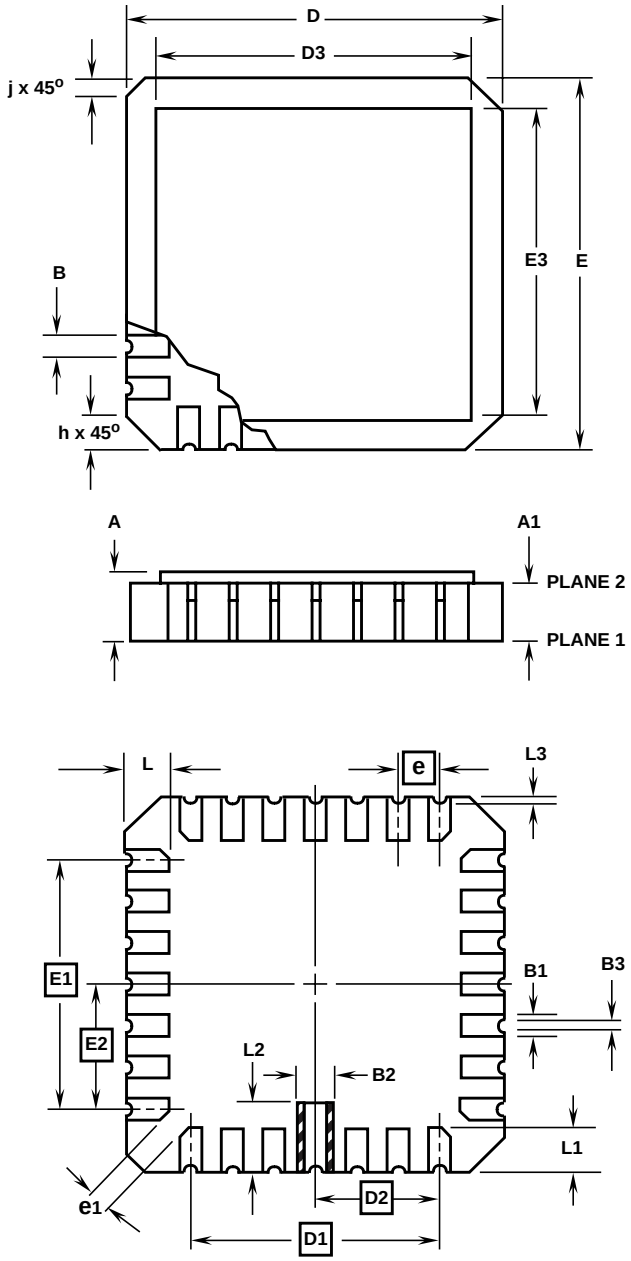
F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch.
11. Materials: Compliant to MIL-I-38535.

Packaging (Continued)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	7
B	-	-	-	-	4
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.
8. Materials: Compliant to MIL-I-38535.

HARRIS Semiconductor

HA2546

DESIGN INFORMATION

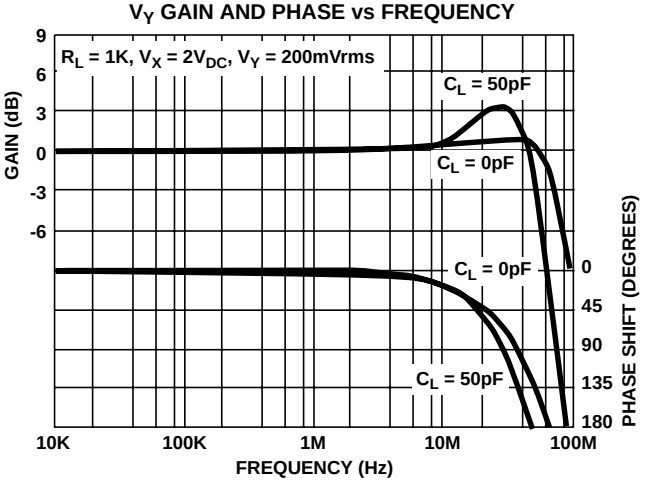
August 1999

Wideband Two Quadrant Analog Multiplier

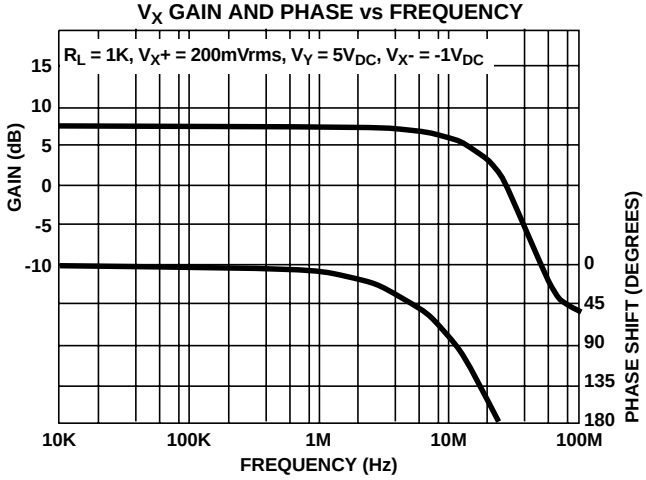
The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $V_S = \pm15V$, $T_A = +25^oC$, See Test Circuit For Multiplier Configuration.

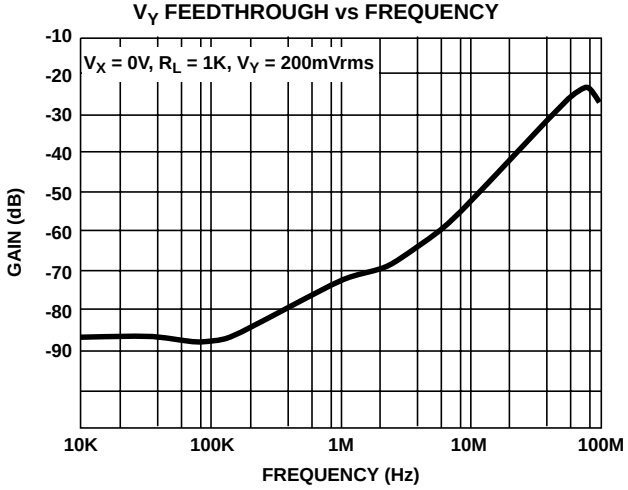
V_Y GAIN AND PHASE vs FREQUENCY



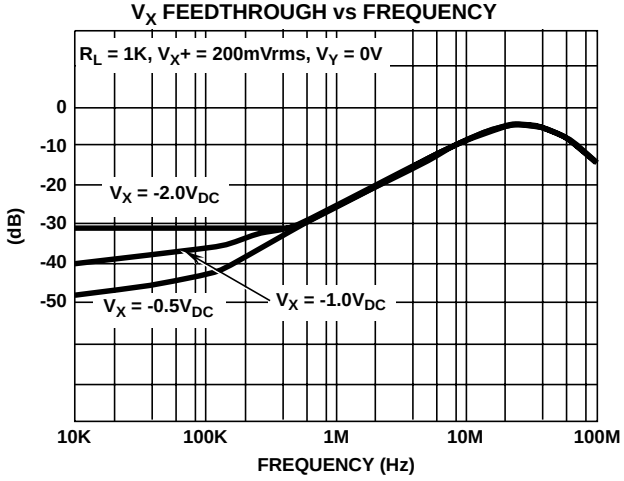
V_X GAIN AND PHASE vs FREQUENCY



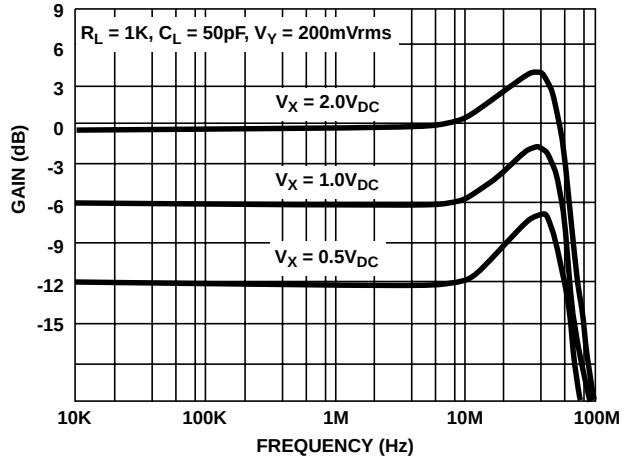
V_Y FEEDTHROUGH vs FREQUENCY



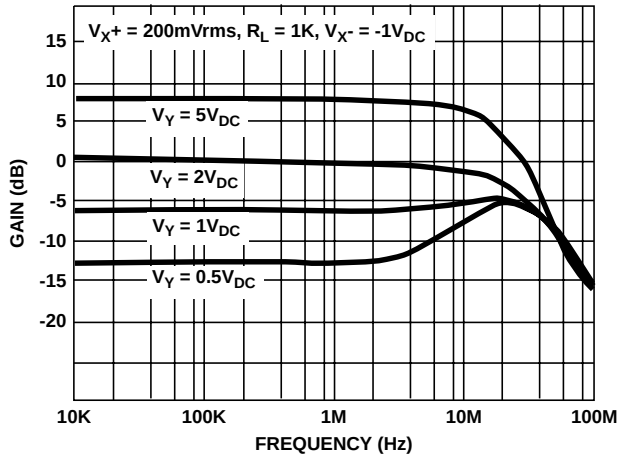
V_X FEEDTHROUGH vs FREQUENCY



VARIOUS V_Y FREQUENCY RESPONSES



VARIOUS V_X FREQUENCY RESPONSES



DESIGN INFORMATION (Continued)

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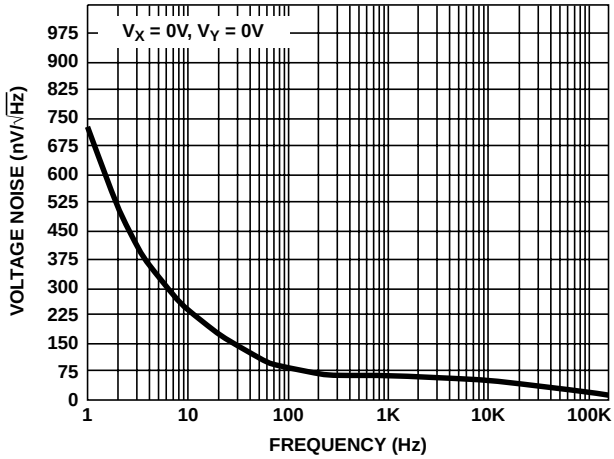
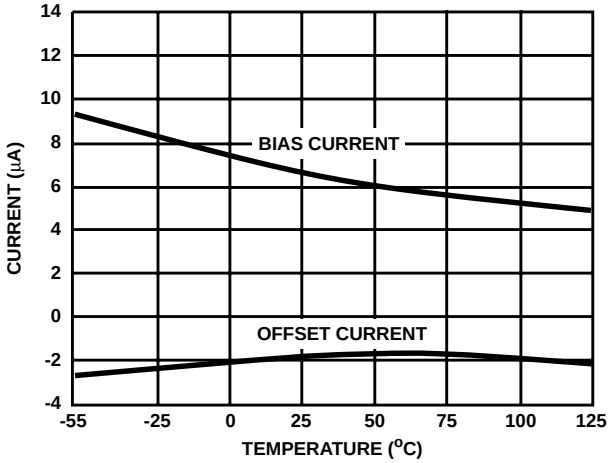
Typical Performance Curves $V_S = \pm15V$, $T_A = +25^oC$, See Test Circuit For Multiplier Configuration. **(Continued)**

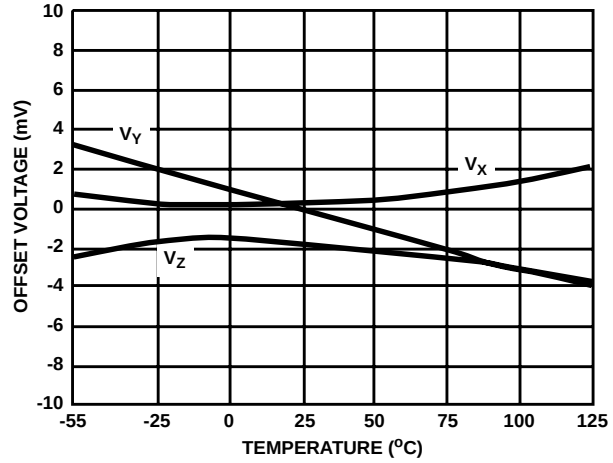
NOISE CHARACTERISTICS



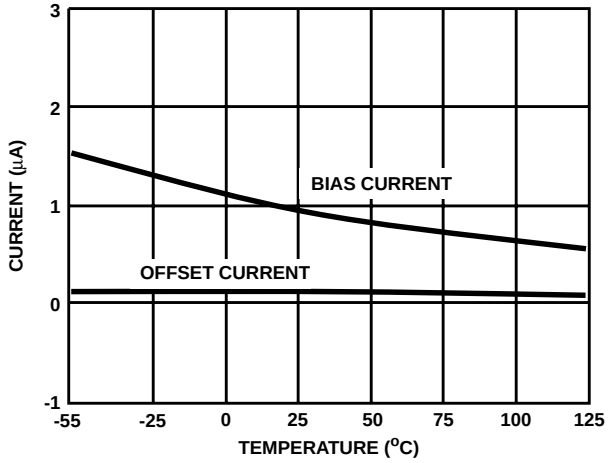
V_Y OFFSET AND BIAS CURRENT vs TEMPERATURE



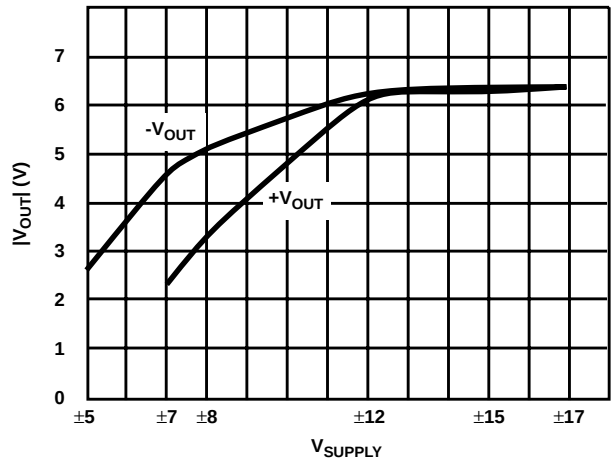
OFFSET VOLTAGE vs TEMPERATURE



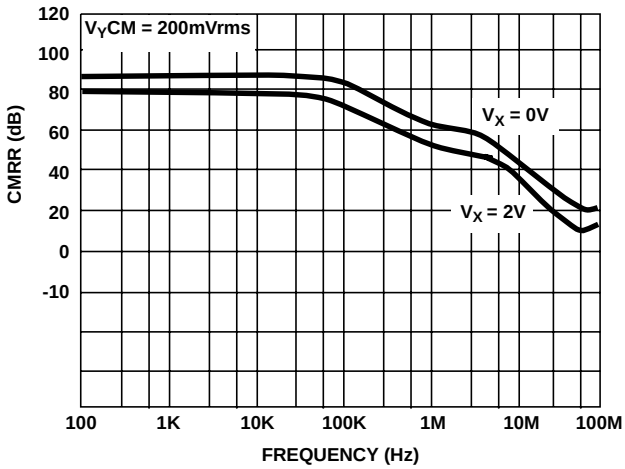
V_X OFFSET AND BIAS CURRENT vs TEMPERATURE



V_{OUT} vs V_{SUPPLY}



V_Y CMRR vs FREQUENCY



DESIGN INFORMATION (Continued)

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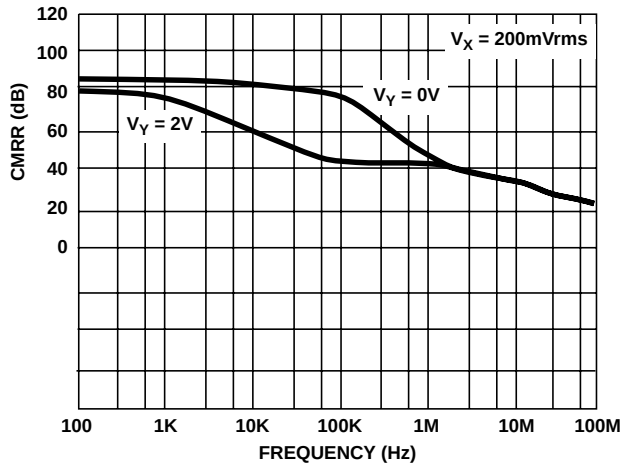
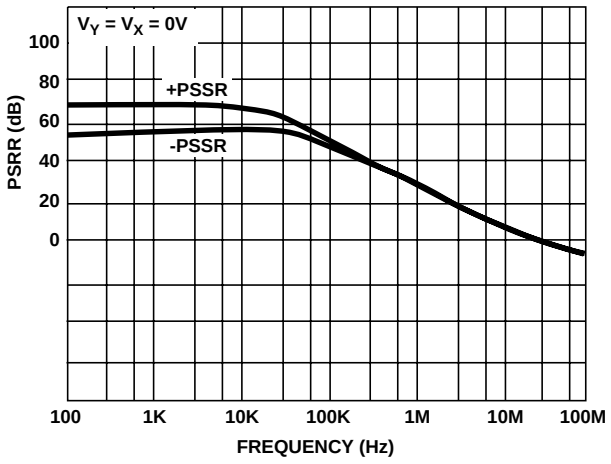
Typical Performance Curves $V_S = \pm15V$, $T_A = +25^oC$, See Test Circuit For Multiplier Configuration. **(Continued)**

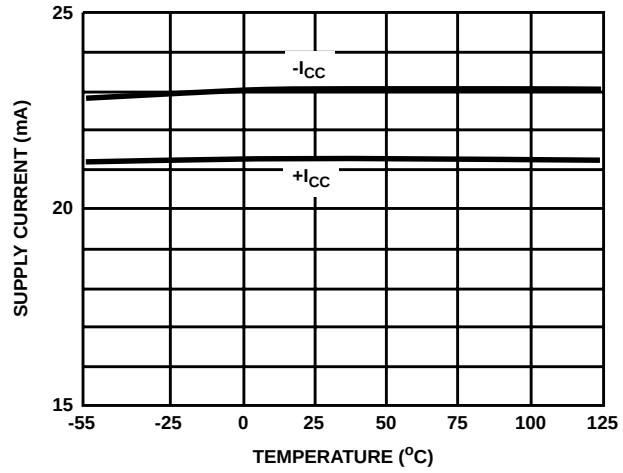
V_X COMMON MODE REJECTION RATIO vs FREQUENCY



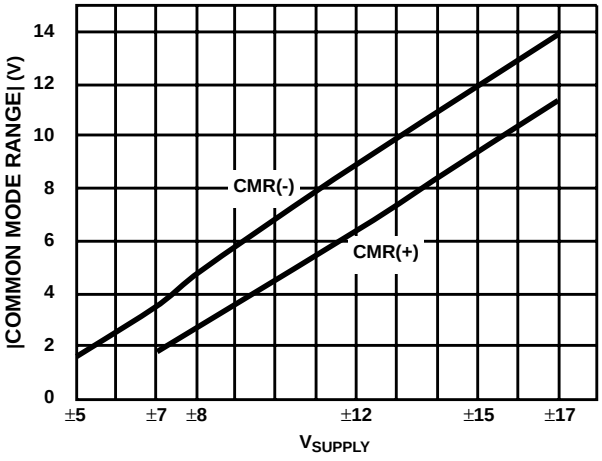
PSRR vs FREQUENCY



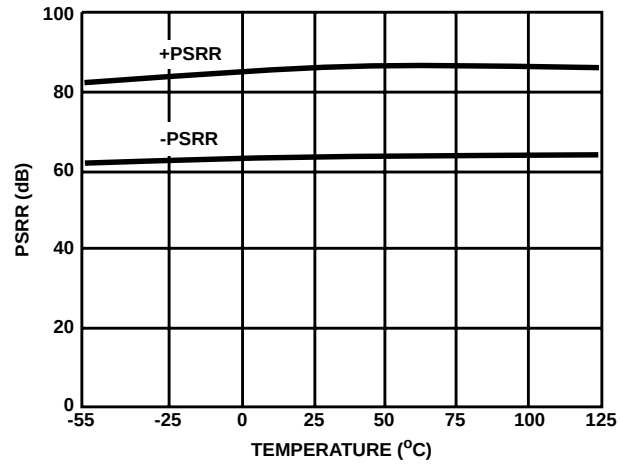
SUPPLY CURRENT vs TEMPERATURE



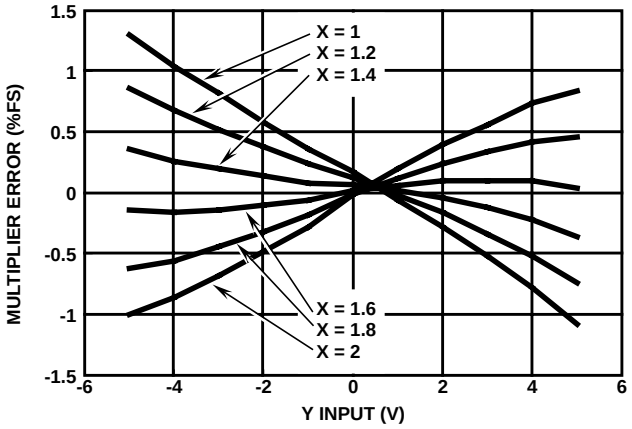
COMMON MODE RANGE vs V_{SUPPLY}



PSRR vs TEMPERATURE



MULTIPLIER ERROR



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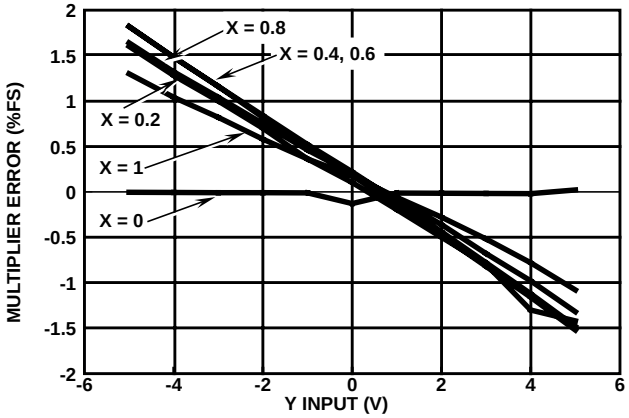
Typical Performance Curves $V_S = \pm15V$, $T_A = +25^oC$, See Test Circuit For Multiplier Configuration. **(Continued)**

MULTIPLIER ERROR



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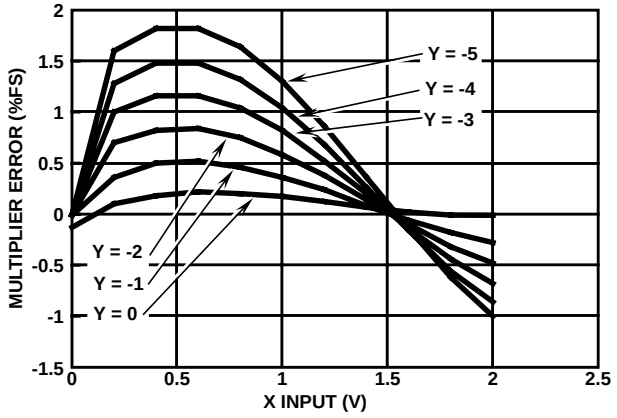
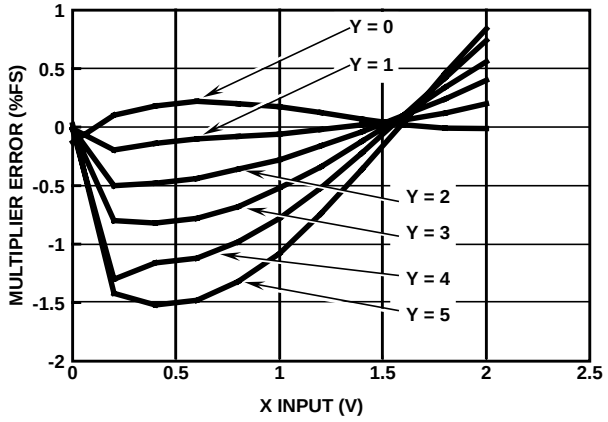
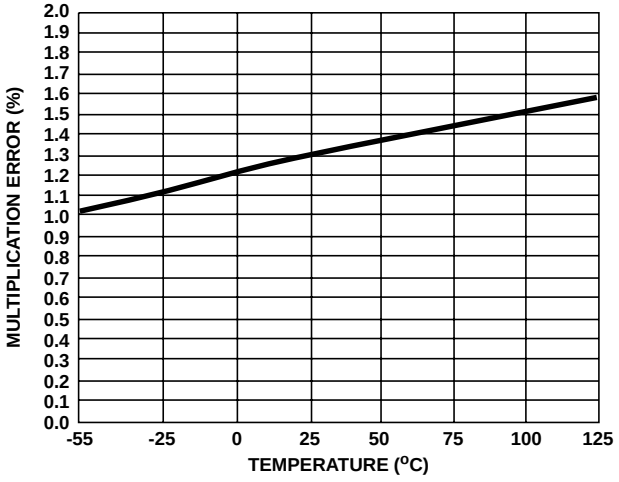


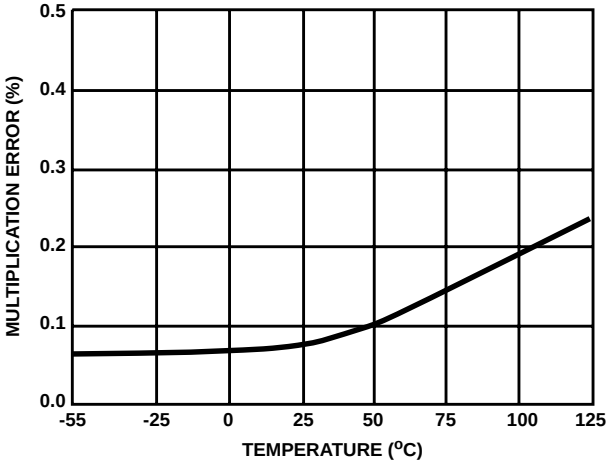
MULTIPLIER ERROR



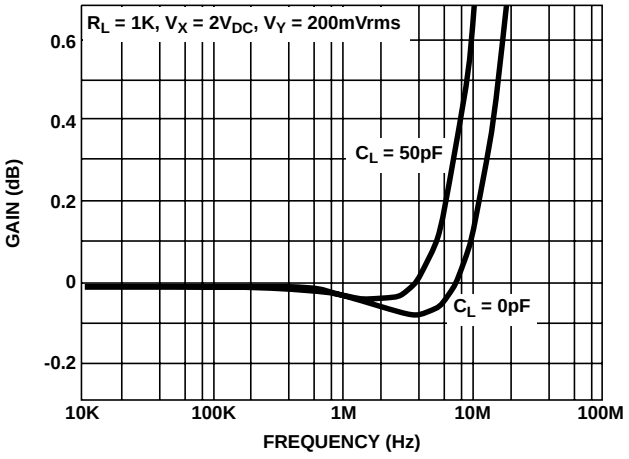
WORST CASE MULTIPLICATION ERROR vs TEMPERATURE



MULTIPLICATION ERROR vs TEMPERATURE



GAIN VARIATION vs FREQUENCY



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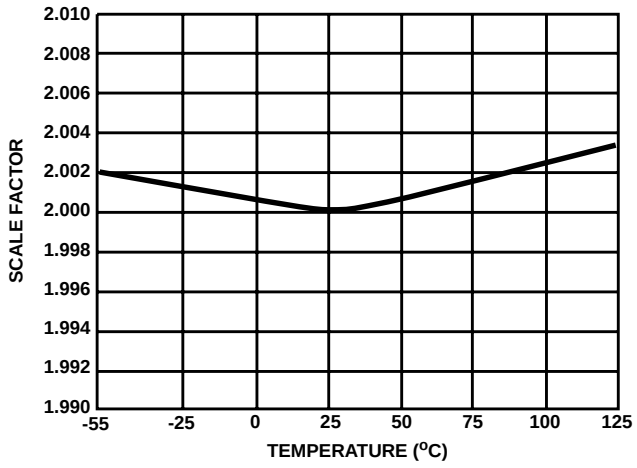
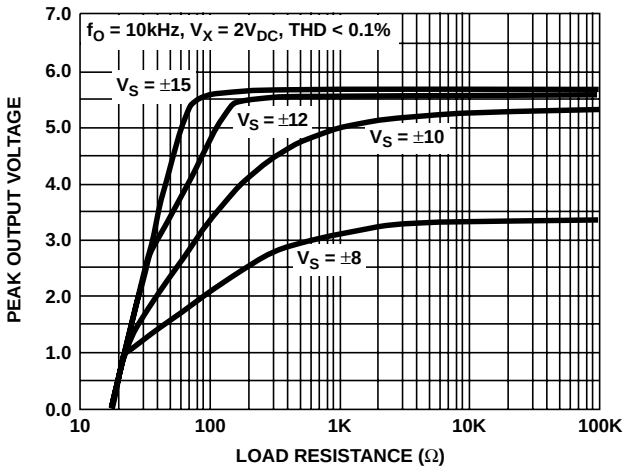
Typical Performance Curves $V_S = \pm15V$, $T_A = +25^oC$, See Test Circuit For Multiplier Configuration. **(Continued)**

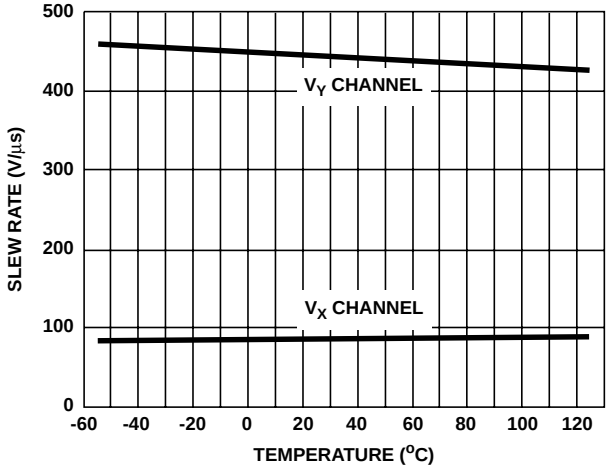
SCALE FACTOR vs TEMPERATURE



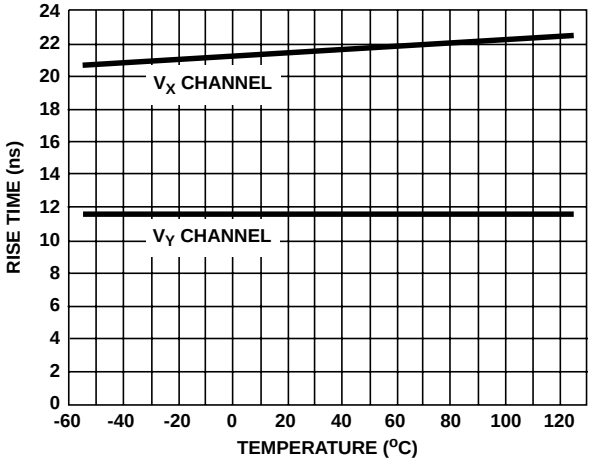
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



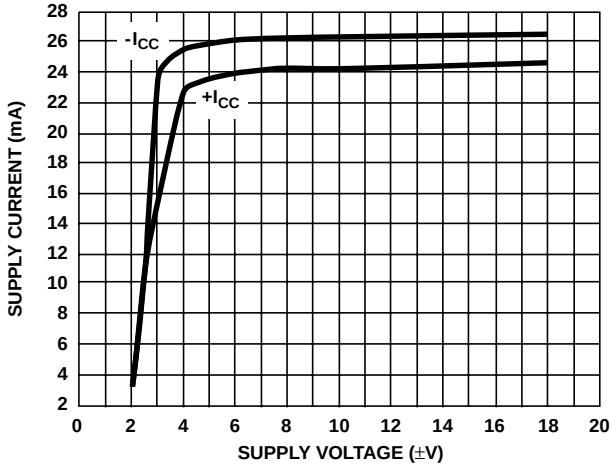
SLEW RATE vs TEMPERATURE



RISE TIME vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE



DESIGN INFORMATION (Continued)

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Application Information

Theory of Operation

The HA-2546 is a two quadrant multiplier with the following three differential inputs; the signal channel, V_Y+ and V_Y-, the control channel, V_X+ and V_X-, and the summed channel, V_Z+ and V_Z-, to complete the feedback of the output amplifier. The differential voltages of channel X and Y are converted to differential currents. These currents are then multiplied in a circuit similar to a Gilbert Cell multiplier, producing a differential current product. The differential voltage of the Z channel is converted into a differential current which then sums with the products currents. The differential "product/sum" currents are converted to a single-ended current and then converted to a voltage output by a transimpedance amplifier.

The open loop transfer equation for the HA-2546 is:

$$V_{OUT} = A \left[\frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{SF} - (V_{Z+} - V_{Z-}) \right]$$

where;

A = Output Amplifier Open Loop Gain

SF = Scale Factor

V_X, V_Y, V_Z = Differential Inputs

The scale factor is used to maintain the output of the multiplier within the normal operating range of ±5V. The scale factor can be defined by the user by way of an optional external resistor, R_{EXT}, and the Gain Adjust pins, Gain Adjust A (GA A), Gain Adjust B (GA B), and Gain Adjust C (GA C). The scale factor is determined as follows:

SF = 2, when GA B is shorted to GA C

SF ≅ 1.2 R_{EXT}, when R_{EXT} is connected between GA A and GA C (R_{EXT} is in kΩ)

SF ≅ 1.2 (R_{EXT} + 1.667kΩ), when R_{EXT} is connected to GA B and GA C (R_{EXT} is in kΩ)

The scale factor can be adjusted from 2 to 5. It should be noted that any adjustments to the scale factor will affect the AC performance of the control channel, V_X. The normal input operating range of V_X is equal to the scale factor voltage.

The typical multiplier configuration is shown in Figure 1. The ideal transfer function for this configuration is:

$$V_{OUT} = \begin{cases} \frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{2} + V_{Z-}, & \text{when } V_X \geq 0V \\ 0, & \text{when } V_X < 0V \end{cases}$$

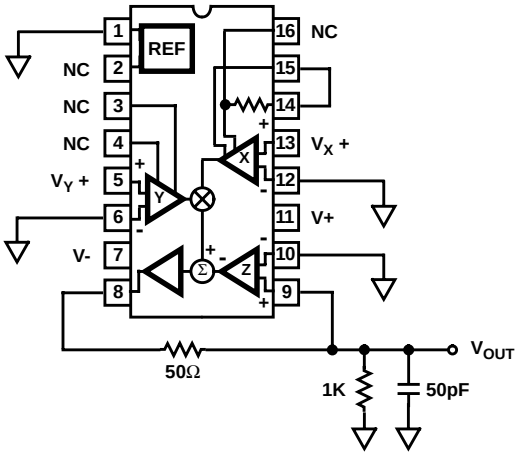

FIGURE 1.

The V_{X-} pin is usually connected to ground so that when V_{X+} is negative there is no signal at the output, i.e. two quadrant operation. If the V_X input is a negative going signal the V_{X+} pin maybe grounded and the V_{X-} pin used as the control input.

The V_{Y-} terminal is usually grounded allowing the V_{Y+} to swing ±5V. The V_{Z+} terminal is usually connected directly to V_{OUT} to complete the feedback loop of the output amplifier while V_{Z-} is grounded. The scale factor is normally set to 2 by connecting GA B to GA C. Therefore the transfer equation simplifies to $V_{OUT} = (V_X V_Y) / 2$.

Offset Adjustment

The signal channel offset voltage may be nulled by using a 20kΩ potentiometer between V_{YIO} Adjust pins A and B and connecting the wiper to -V. Reducing the signal channel offset will reduce V_X AC feedthrough. Output offset voltage can also be nulled by connecting V_{Z-} to the wiper of a 20kΩ potentiometer which is tied between +V and -V.

Capacitive Drive Capability

When driving capacitive loads >20pF, a 50Ω resistor is recommended between V_{OUT} and V_{Z+}, using V_{Z+} as the output (See Figure 1). This will prevent the multiplier from going unstable.

Power Supply Decoupling

Power supply decoupling is essential for high frequency circuits. A 0.01µF high quality ceramic capacitor at each supply pin in parallel with a 1µF tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to the close spacing with which they may be placed to the supply pins minimizing lead inductance.

Adjusting Scale Factor

The HA-2546 two quadrant multiplier may be configured for many uses. Following are examples of a few typical applications.

DESIGN INFORMATION (Continued)

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Adjusting the scale factor will tailor the control signal, V_X, input voltage range to match your needs. Referring to the simplified schematic and looking for the V_X input stage, you will notice the unusual design. The internal reference sets up a 1.2mA current sink for the V_X differential pair. The control signal applied to this input will be forced across the scale factor setting resistor and set the current flowing in the V_{X+} side of the differential pair. When the current through this resistor reaches 1.2mA, all the current available is flowing in the one side and full scale has been reached. Normally the 1.67kΩ internal resistor sets the scale factor to 2V when the Gain Adjust pins B and C are connected together, but you may set this resistor to any convenient value using pins 16 (GA A) and 15 (GA C).

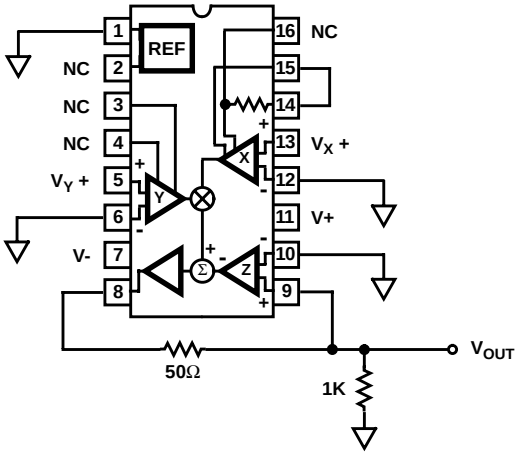

FIGURE 2A. MULTIPLIER, $V_{OUT} = V_X V_Y / 2$, SCALE FACTOR = 2V

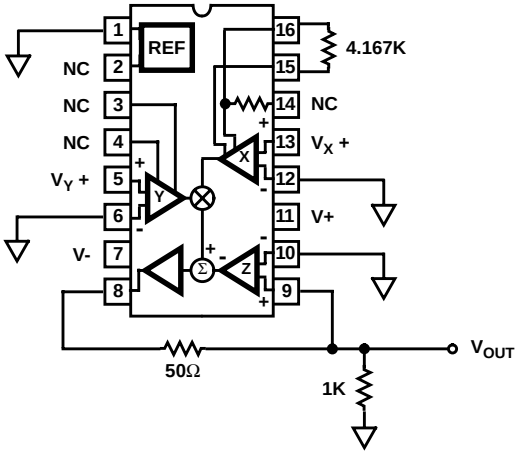

FIGURE 2B. MULTIPLIER, $V_{OUT} = V_X V_Y / 5$, SCALE FACTOR = 5V

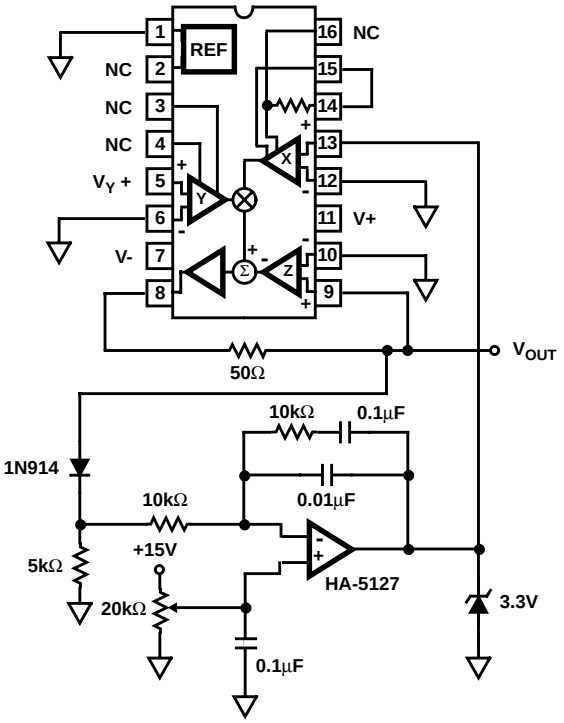

FIGURE 3. AUTOMATIC GAIN CONTROL

In Figure 3, the HA-2546 is configured in a true Automatic Gain Control or AGC application. The HA-5127, low noise op amp, provides the gain control level to the X input. This level will set the peak output voltage of the multiplier to match the reference level. The feedback network around the HA-5127 provides stability and a response time adjustment for the gain control circuit.

DESIGN INFORMATION (Continued)

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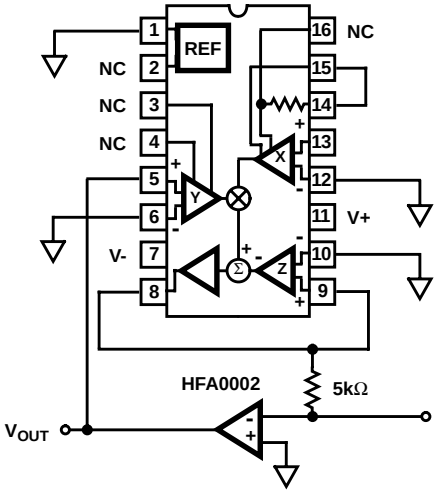


FIGURE 4A. VOLTAGE CONTROLLED AMPLIFIER

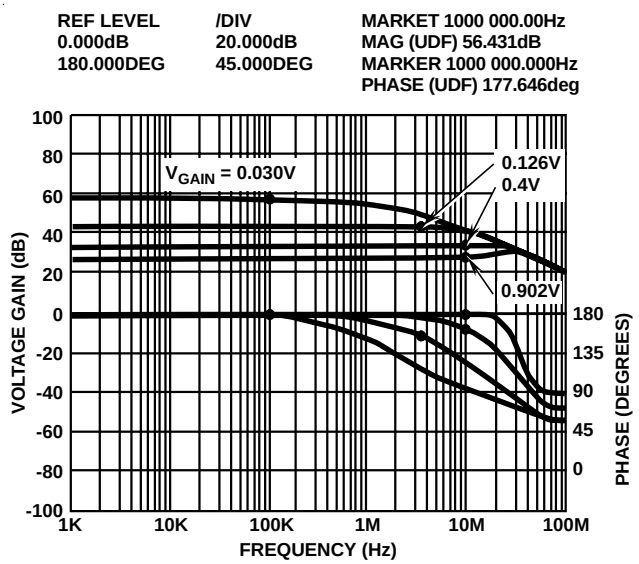


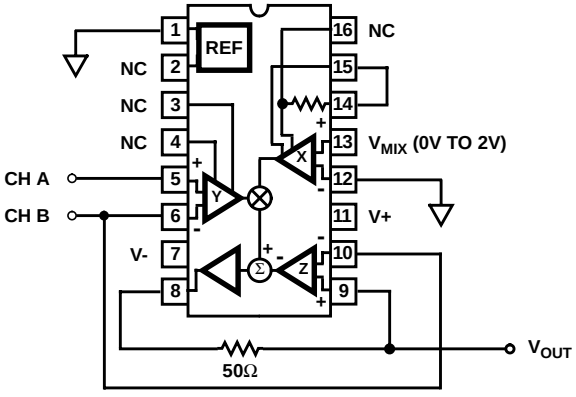
FIGURE 4B. VOLTAGE CONTROLLED AMPLIFIER

This multiplier has the advantage over other AGC circuits, in that the signal bandwidth is not affected by the control signal gain adjustment.

A wide range of gain adjustment is available with the Voltage Controlled Amplifier configuration shown in Figure 4A. and Figure 4B. Here the gain of the HFA0002 is swept from 20V/V at a control voltage of 0.902V to a gain of almost 1000V/V with a control voltage of 0.03V.

The Video Fader circuit provides a unique function as shown in Figure 5. Here Ch B is applied to the minus Z input in addition to the minus Y input. V_{MIX} will control the percentage of Ch A and Ch B that are mixed together to produce a resulting video image or other signal.

Many other applications are possible including division, squaring, square-root, percentage calculations, etc. Please refer to the HA-2556 four quadrant multiplier for additional applications.



V_{OUT} = Ch B + (Ch A - Ch B) V_{MIX} / Scale Factor
Scale Factor = 2
V_{OUT} = All Ch B; if V_{MIX} = 0V
V_{OUT} = All Ch A; if V_{MIX} = 2V (Full Scale)
V_{OUT} = Mix of Ch A and Ch B; if 0V < V_{MIX} < 2V

FIGURE 5. VIDEO FADER

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{LOAD} = 1kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETER		CONDITIONS	TEMP	TYP	UNITS
Multiplication Error Drift			Full	0.002	%/^{o}C
Differential Gain		V_X = 2V, V_Y = 300mV_{P-P}, f_O = 3.58MHz	+25^{o}C	0.1	%
Differential Phase		V_X = 2V, V_Y = 300mV_{P-P}, f_O = 3.58MHz	+25^{o}C	0.1	Degrees
Gain Tolerance	DC to 5MHz	V_X = 2V	+25^{o}C	0.1	dB
	5MHz to 8MHz		+25^{o}C	0.18	dB
1% Amplitude Error			+25^{o}C	6	MHz
1% Vector Error			+25^{o}C	260	kHz
THD+N		f_O = 10kHz, V_Y = 1Vrms, V_X = 2V	+25^{o}C	0.03	%
Voltage Noise	f_O = 10Hz	V_X = 0V, V_Y = 0V	+25^{o}C	400	nV/Hz
	f_O = 100Hz		+25^{o}C	150	nV/Hz
	f_O = 1kHz		+25^{o}C	75	nV/Hz
Common Mode Range			+25^{o}C	±9	V
SIGNAL INPUT, V_Y					
Average Offset Voltage Drift			Full	45	µV/^{o}C
Differential Input Resistance			+25^{o}C	720	KΩ
Small Signal Bandwidth (-3dB)		V_X = 2V	+25^{o}C	40	MHz
Feedthrough		f_O = 5MHz, V_X = 0V, V_Y = 200mVrms	+25^{o}C	-52	dB
V_Y TRANSIENT RESPONSE					
Propagation Delay			+25^{o}C	25	ns
Settling Time		V_Y = ±5V, V_X = 2V	+25^{o}C	200	ns
CONTROL INPUT, V_X					
Average Offset Voltage Drift			Full	10	µV/^{o}C
Differential Input Resistance			+25^{o}C	360	kΩ
Small Signal Bandwidth (-3dB)		V_Y = 5V, V_X = -1V	+25^{o}C	17	MHz
Feedthrough		f_O = 100kHz, V_Y = 0V, V_X = 200mVrms	+25^{o}C	-40	dB
Common Mode Rejection Ratio		V_X = 0V to 2V, V_Y = 5V	+25^{o}C	80	dB
V_X TRANSIENT RESPONSE					
Propagation Delay			+25^{o}C	50	ns
Settling Time		V_X = 0 to 2V, V_Y = 5V	+25^{o}C	200	ns
V_Z CHARACTERISTICS					
Open Loop Gain			+25^{o}C	70	dB
Differential Input Resistance			+25^{o}C	900	kΩ
OUTPUT CHARACTERISTICS					
Output Resistance			+25^{o}C	1	Ω