HA-4741/883

July 1994

Quad Operational Amplifier

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Slew Rate . . . . . 0.9V/μs (Min)**
- **Bandwidth . . . . . 2.5MHz (Min)**
- **Input Offset Voltage. . . . . 3mV (Max)**
- **Input Bias Current . . . . . 200nA (Max)**
- **Input Voltage Noise . . . . . 9nV/√Hz (Typ)**
- **No Crossover Distortion**
- **Standard Quad Pinout**

Applications

- **Universal Active Filters**
- **D3 Communications Filters**
- **Audio Amplifiers**
- **Battery-Powered Equipment**

Description

The Intersil HA-4741/883, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741/883 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

The HA-4741/883 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (3mV max), input bias current (200nA max) and input voltage noise (9nV/√Hz typ at 1kHz). The 2.5MHz bandwidth, coupled with high open loop gain, allow the HA-4741/883 to be used in designs requiring amplifiers of wideband signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741/883's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741/883 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (66dB at 10kHz).

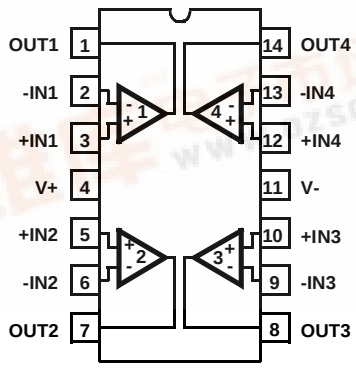
A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741/883, making it compatible with almost any system including battery-powered equipment.

Ordering Information

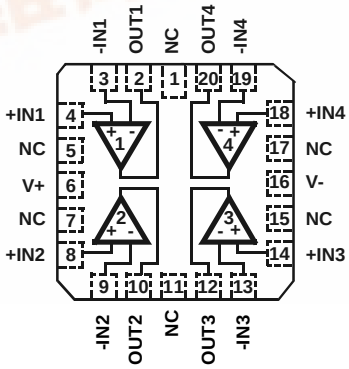
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-4741/883	-55°C to +125°C	14 Lead CerDIP
HA4-4741/883	-55°C to +125°C	20 Lead Ceramic LCC

Pinouts

HA-4741/883
(CERDIP)
TOP VIEW



HA-4741/883
(CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 15V
Voltage at Either Input Terminal . . . . . V+ to V-
Output Current . . . . . Indefinite (One Amplifier Shorted to GND)
Junction Temperature (T_J) . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
ESD Rating . . . . . <2000V
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	75°C/W	20°C/W
Ceramic LCC Package	65°C/W	15°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq +175°C$
CerDIP Package 1.33W
Ceramic LCC Package 1.54W
Package Power Dissipation Derating Factor Above +75°C
CerDIP Package . . . . . 13.3mW/°C
Ceramic LCC Package . . . . . 15.4mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage . . . . . ±5V to ±15V
$V_{INCM} \leq 1/2\ (V+ - V-)$
$R_L \geq 2k\Omega$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_{SUPPLY} = \pm15V$, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-5	5	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$, $+R_S = 10k\Omega$, $-R_S = 100\Omega$	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
	$-I_B$	$V_{CM} = 0V$, $+R_S = 100\Omega$, $-R_S = 10k\Omega$	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$, $+R_S = 10k\Omega$, $-R_S = 10k\Omega$	1	+25°C	-30	30	nA
			2, 3	+125°C, -55°C	-75	75	nA
Common Mode Range	+CMR	V+ = 3V, V- = -27V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-CMR	V+ = 27V, V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	$V_{OUT} = 0V$ and +10V, $R_L = 2k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
	$-A_{VOL}$	$V_{OUT} = 0V$ and -10V, $R_L = 2k\Omega$	4	+25°C	50	-	kV/V
			5, 6	+125°C, -55°C	25	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = -10V$, V+ = +5V, V- = -25V, $V_{OUT} = -10V$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	74	-	dB
	-CMRR	$\Delta V_{CM} = +10V$, V+ = +25V, V- = -5V, $V_{OUT} = +10V$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	74	-	dB

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	$+V_{OUT1}$	R_L = 10kΩ	4	+25°C	12	-	V
			5, 6	+125°C, -55°C	12	-	V
	$-V_{OUT1}$	R_L = 10kΩ	4	+25°C	-	-12	V
			5, 6	+125°C, -55°C	-	-12	V
	$+V_{OUT2}$	R_L = 2kΩ	4	+25°C	10	-	V
			5, 6	+125°C, -55°C	10	-	V
	$-V_{OUT2}$	R_L = 2kΩ	4	+25°C	-	-10	V
			5, 6	+125°C, -55°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	5	-	mA
			5, 6	+125°C, -55°C	5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-5	mA
			5, 6	+125°C, -55°C	-	-5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	5	mA
			2, 3	+125°C, -55°C	-	7	mA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-5	-	mA
			2, 3	+125°C, -55°C	-7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = +5V, V+ = +10V, V- = -15V, V+ = +20V, V- = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	ΔV_{SUP} = -5V, V+ = +15V, V- = -10V, V+ = +15V, V- = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	V_{OUT} = -5V to +5V	7	+25°C	0.9	-	V/µs
	-SR	V_{OUT} = +5V to -5V	7	+25°C	0.9	-	V/µs
Rise and Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	140	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	140	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%
Gain Bandwidth Product (Small Signal)	GBWP	V_{OUT} = 50mV	7	+25°C	2.5	-	MHz

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V_{SUPPLY} = ±15V, R_{LOAD} = 5kΩ, C_{LOAD} = 50pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	260	-	kΩ
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	14	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	350	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	180	mW
Channel Separation	CS	f = 10kHz, R_S = 1kΩ Referred to Input A_V = 100V/V, V_{IN} = 100mV_{PEAK}	1	+25°C	-66	-	dB

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/(2πV_{PEAK}).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
87 x 75 x 19 mils ± 1 mils
2210 x 1910 x 483µm ± 25.4µm

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

WORST CASE CURRENT DENSITY:
1.68×10^5 A/cm^2

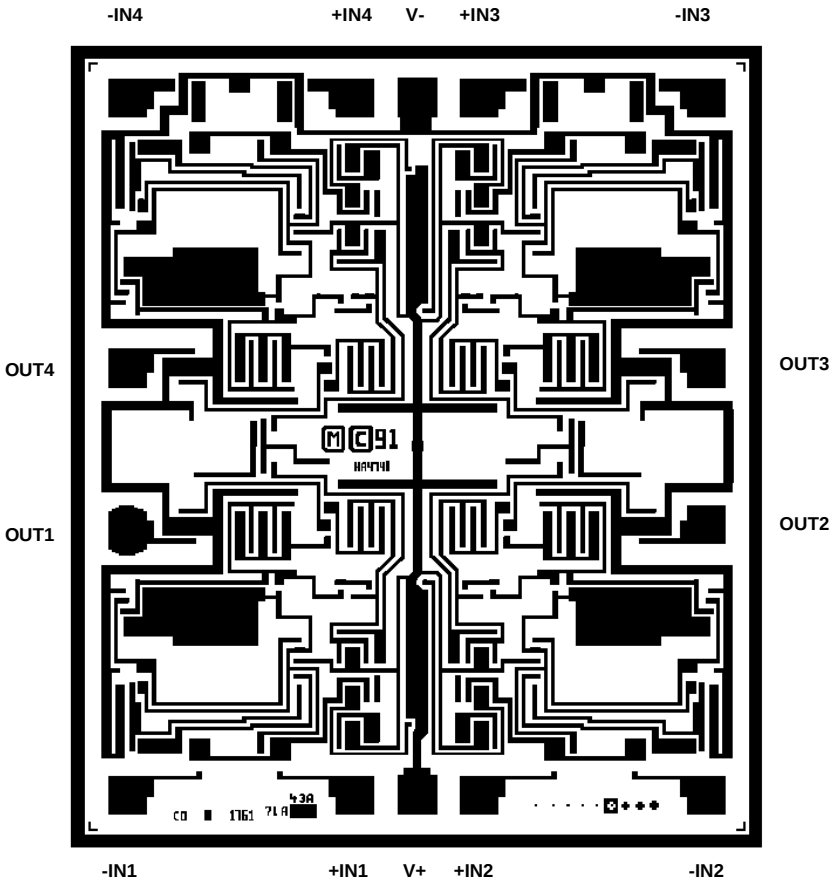
SUBSTRATE POTENTIAL (Powered Up): V-

TRANSISTOR COUNT: 72

PROCESS: Junction Isolated Bipolar/JFET

Metallization Mask Layout

HA-4741/883



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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality