34 W × 4-Channel BTL Power IC

HITACHI

ADE-207-263A (Z)

2nd Edition Jul. 1999

Description

The HA13158A is four-channel BTL amplifier IC designed for car audio, featuring high output and low distortion, and applicable to digital audio equipment. It provides 34 W output per channel, with a 13.7 V power supply and at Max distortion. DZSC.COM

Functions

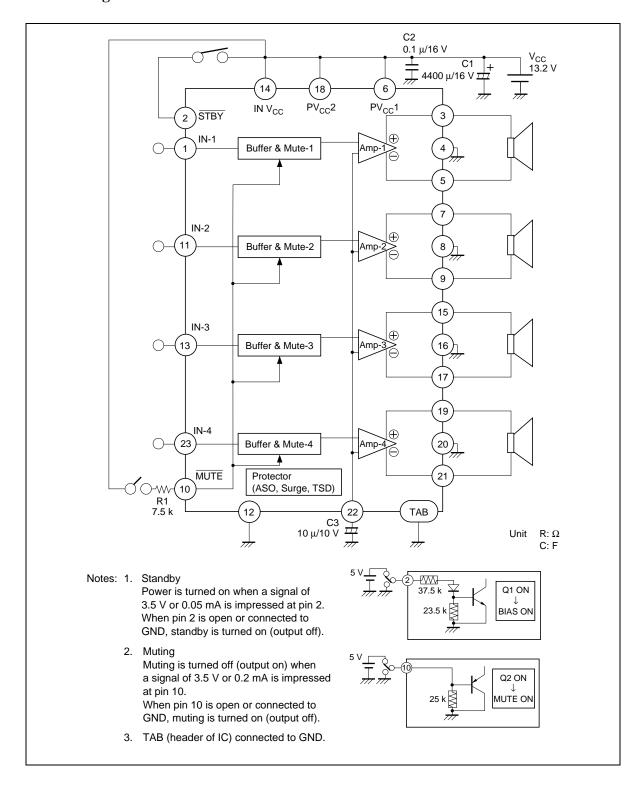
- 4 ch BTL power amplifiers
- Built-in standby circuit
- Built-in muting circuit
- Built-in protection circuit (surge, T.S.D and ASO)

Features

- Low power dissipation
- Soft thermal limiter
- Requires few external parts (C:3, R:1)
- Popping noise minimized
- Low output noise
- Built-in high reliability protection circuit
- Pin to pin with HA13153A/HA13154A/HA13155/HA13157/HA13158



Block Diagram

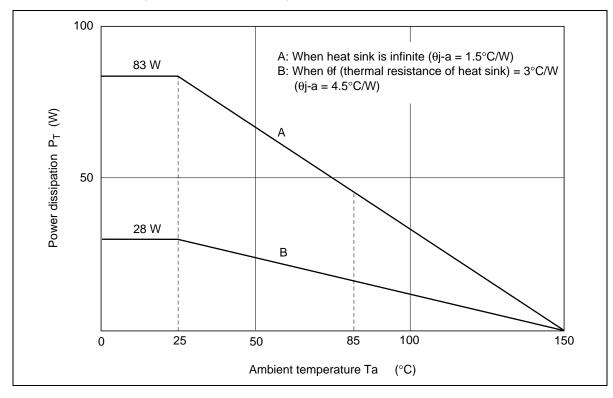


Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Operating supply voltage	V _{cc}	18	V
Supply voltage when no signal*1	V _{cc} (DC)	26	V
Peak supply voltage*2	V _{cc} (PEAK)	50	V
Output current*3	I _o (PEAK)	4	Α
Power dissipation*4	P _T	83	W
Junction temperature	Tj	150	°C
Operating temperature	Topr	-30 to +85	°C
Storage temperature	Tstg	-55 to +125	°C

Note: 1. Tolerance within 30 seconds.

- 2. Tolerance in surge pulse waveform.
- 3. Value per 1 channel.
- 4. Value when attached on the infinite heat sink plate at Ta = 25 °C. The derating carve is as shown in the graph below.



Electrical Characteristics (V $_{\rm CC}$ = 13.2 V, f = 1 kHz, R $_{\!\scriptscriptstyle L}$ = 4 $\Omega,$ Rg = 600 $\Omega,$ Ta = 25°C)

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Quiescent current	I _{Q1}	_	220	_	mA	Vin = 0
Output offset voltage	$\Delta V_{_{Q}}$	-180	0	+180	mV	
Gain	G _v	30.5	32	33.5	dB	
Gain difference between channels	$\Delta G_{\scriptscriptstyle ee}$	-1.0	0	+1.0	dB	
Rated output power	P _o	_	20	_	W	$V_{cc} = 13.2 \text{ V},$ THD = 10%, $R_L = 4 \Omega$
Max output power	P _{omax}	_	34	_	W	$V_{cc} = 13.7 \text{ V}, R_{L} = 4 \Omega$
Total harmonic distortion	T.H.D.	_	0.03	_	%	Po = 3 W
Output noise voltage	WBN	_	0.15	_	mVrms	Rg = 0Ω , BW = 20 to 20 kHz
Ripple rejection	SVR	_	55	_	dB	f = 120 Hz
Channel cross talk	C.T.	_	70	_	dB	Vout = 0 dBm
Input impedance	Rin	_	25	_	kΩ	
Standby current	I _{Q2}	_	_	10	μΑ	
Standby control voltage (high)	V _{STH}	3.5	_	V _{cc}	V	
Standby control voltage (low)	$V_{\mathtt{STL}}$	0	_	1.5	V	
Muting control voltage (high)	V _{MH}	3.5	_	V _{cc}	V	
Muting control voltage (low)	V _{ML}	0	_	1.5	V	
Muting attenuation	ATTM	_	70	_	dB	Vout = 0 dBm

Pin Explanation

Pin No.	Symbol	Functions	Input Impedance	DC Voltage	Equivalence Circuit
1	IN1	CH1 INPUT	25 kΩ (Typ)	0 V	1 → W → W S 25 k
11	IN2	CH2 INPUT	_		
13	IN3	CH3 INPUT	_		
23	IN4	CH4 INPUT			
2	STBY	Standby control	90 kΩ (at Trs. cutoff)	_	23.5 k
3	OUT1 (+)	CH1 OUTPUT	_	V _{cc} /2	3
5	OUT1 (-)	_			<i>'''</i>
7	OUT2 (+)	CH2 OUTPUT	_		
9	OUT2 (-)	_			
15	OUT3 (+)	CH3 OUTPUT	_		
17	OUT3 (-)	_			
19	OUT4 (+)	CH4 OUTPUT	_		
21	OUT4 (-)	_			
10	MUTE	Muting control	25 kΩ (Typ)	_	10 \$ 25 k
22	RIPPLE	Bias stability	_	V _{cc} /2	22 \frac{1}{2}

Pin Explanation (cont)

Pin No.	Symbol	Functions	Input Impedance	DC Voltage	Equivalence Circuit
6	PV _{cc} 1	Power of output stage	_	V _{cc}	_
18	PV _{cc} 2	_			
14	INV _{cc}	Power of input stage	_	V _{cc}	_
4	CH1 GND	CH1 power GND	_	_	_
8	CH2 GND	CH2 power GND	_		
16	CH3 GND	CH3 power GND	_		
20	CH4 GND	CH4 power GND	_		
12	IN GND	Input signal GND	_	_	_

Point of Application Board Design

- 1. Notes on Application Board's Pattern Design
- For increasing stability, the connected line of V_{cc} and OUTGND is better to be made wider and lower impedance.
- For increasing stability, it is better to place the capacitor between V_{cc} and GND (0.1 μ F) close to IC.
- It is better to place the grounding of resistor (Rg), between input line and ground, close to INGND (Pin 12) because if OUTGND is connected to the line between Rg and INGND, THD will become worse due to current from OUTGND.

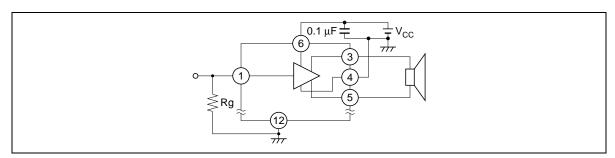


Figure 1 Notes on Application Board's Pattern Design

2. How to Reduce the Popping Noise by Muting Circuit

At normal operating circuit, Muting circuit operates at high speed under 1 µs.

In case popping noise becomes a problem, it is possible to reduce the popping noise by connecting capacitor, which determines the switching time constant, between pin 10 and GND. (Following figure 2)

We recommend value of capacitor greater then 1 µF.

Also transitional popping noise can be reduced sharply by muting before V_{cc} and Standby are ON/OFF.

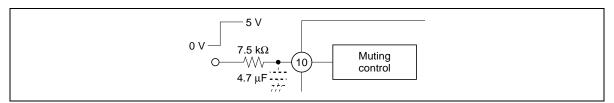
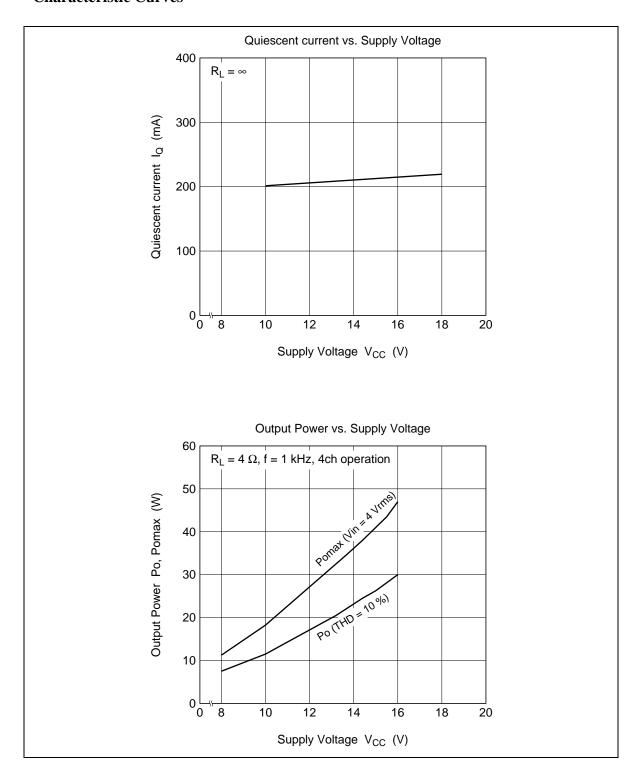


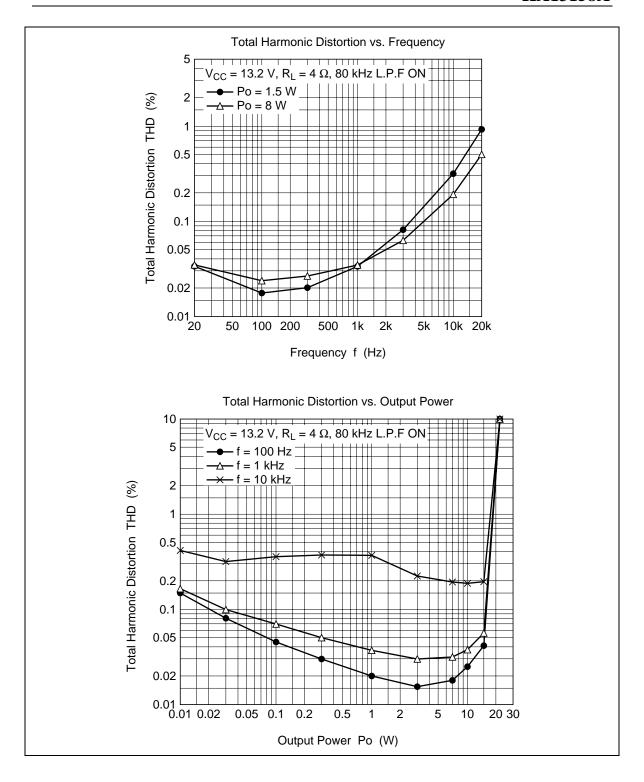
Figure 2 How to use Muting Circuit

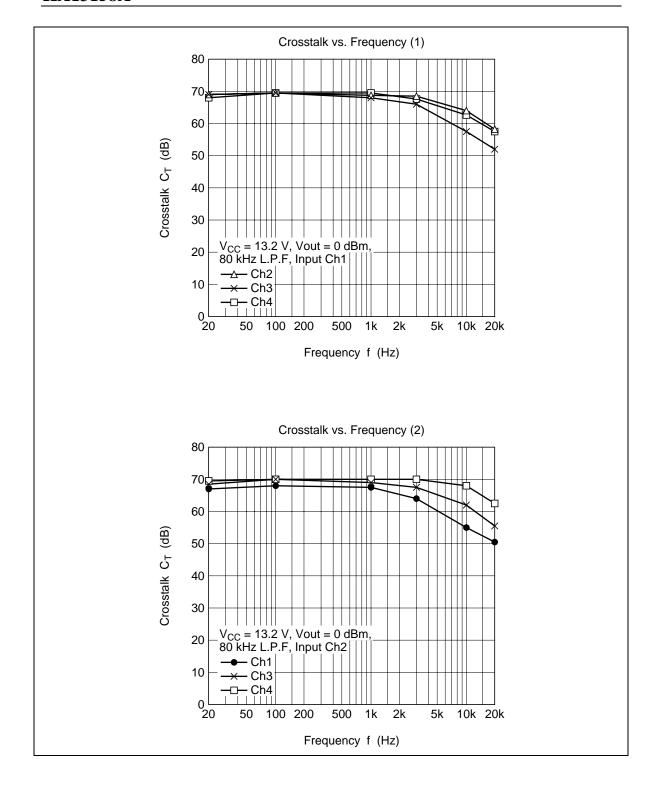
Table 1 Muting ON/OFF Time

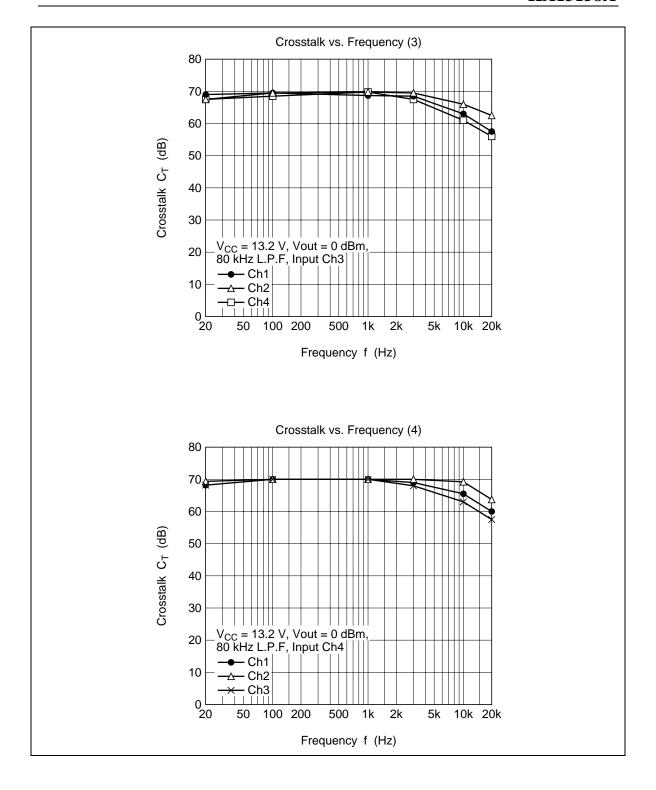
C (μF)	ON Time	OFF Time	
nothing	under 1 μs	under 1 μs	
0.47	2 ms	2 ms	
4.7	19 ms	19 ms	

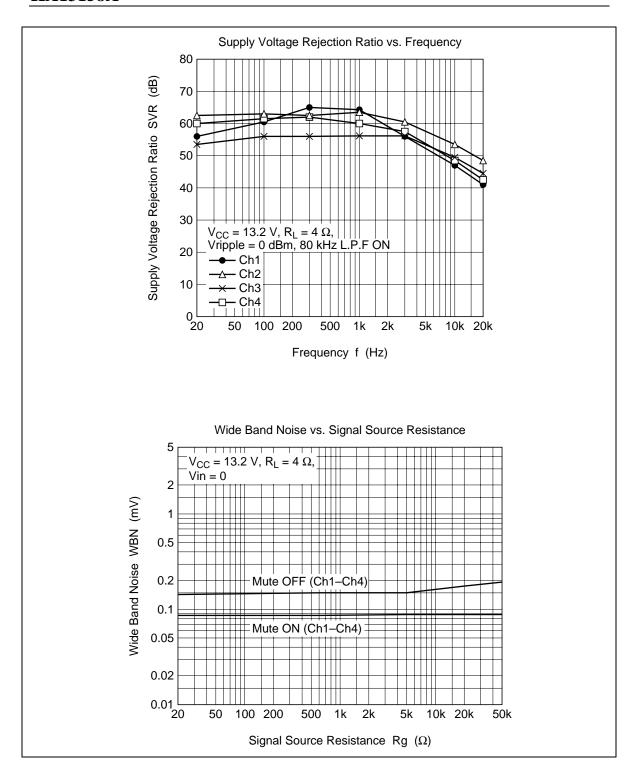
Characteristic Curves

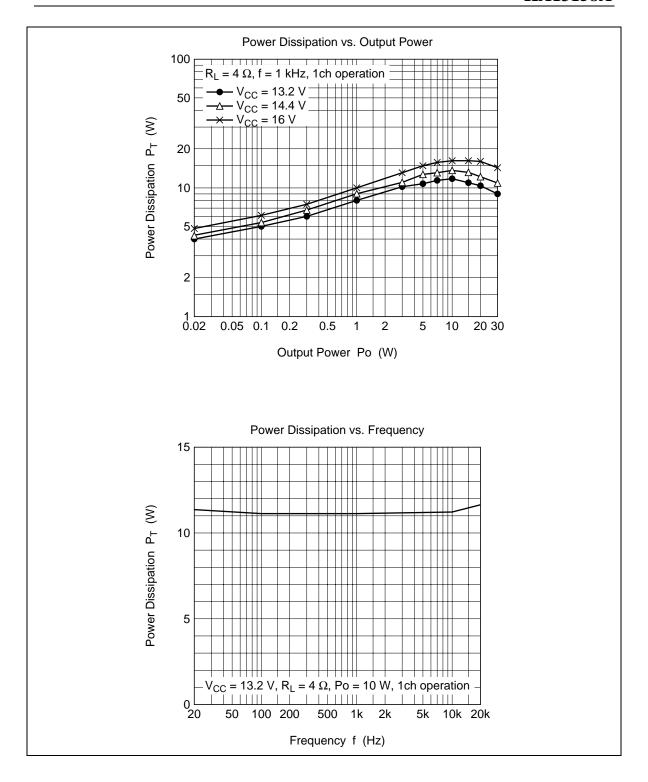




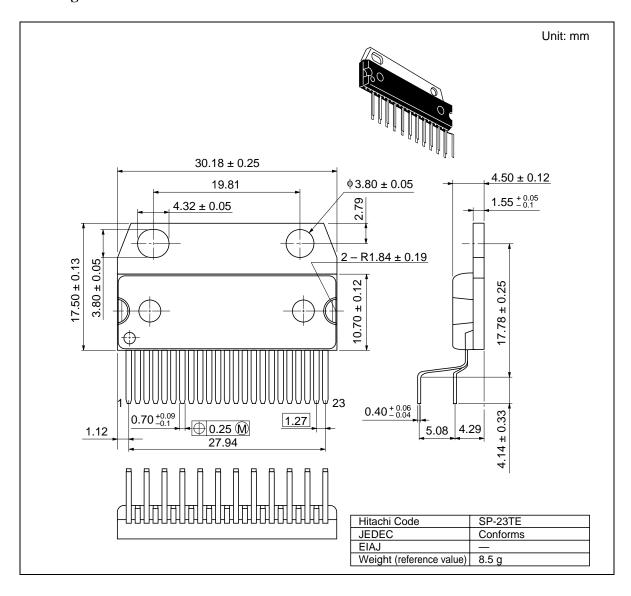








Package Dimensions



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