# HA13561F

## Combo (Spindle & VCM) Driver

# HITACHI

ADE-207-182 (Z)
1st Edition
July 1996

## Description

This COMBO Driver for HDD application consists of Sensorless Spindle Driver and BTL type VCM Driver.

Bipolar Process is applied and a "Soft Switching Circuit" for less commutation noise and a "Booster Circuit' for smaller Saturation Voltage of Output Transistor are also implemented.

## Features

- Soft Switching Driver

  Small Surface Mount Package: FP-80E (QFP80 Pin)

  Low thermal resistance: 35°C/W with 6 layer multi glass-epoxy board
- Low output saturation voltage
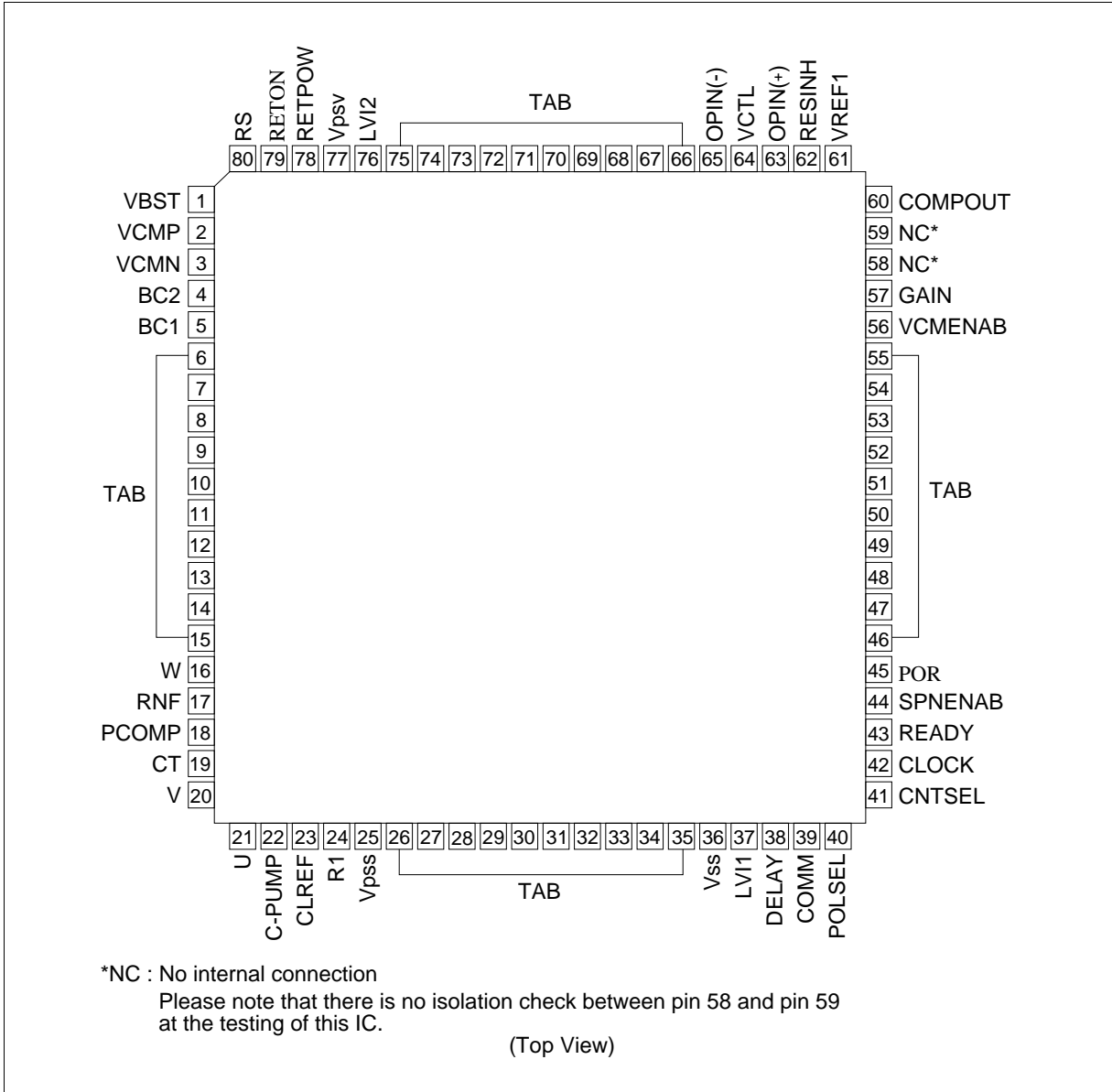  - Spindle    0.8 V Typ (@1.0 A)
  - VCM       0.8 V Typ (@0.8 A)

## Functions

- 1.8 A Max/3-phase motor driver
- 1.2 A Max BTL VCM Driver
- Auto retract
- Soft Switching Matrix
- Start up circuit
- Booster
- Speed Discriminator
- Internal Protector (OTSD, LVI)
- POR
- Power monitor

# HA13561F

## Pin Arrangement



*NC : No internal connection
Please note that there is no isolation check between pin 58 and pin 59
at the testing of this IC.

(Top View)

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## Pin Description

| Pin Number | Pin Name | Function |
| --- | --- | --- |
| 1 | VBST | Boosted voltage output to realize the low output saturation voltage |
| 2 | VCMP | Output terminal on VCM driver |
| 3 | VCMN | Output terminal on VCM driver |
| 4 | BC2 | To be attached the external capacitor for booster circuitry |
| 5 | BC1 | ditto |
| 6 to 15 | GND | Ground pins |
| 16 | W | W phase output terminal on spindle motor driver |
| 17 | RNF | Sensing input for output current on spindle motor driver |
| 18 | PCOMP | To be attached the external capacitor for phase compensation of spindle motor driver |
| 19 | CT | To be attached the center tap of the spindle motor for B-EMF sensing |
| 20 | V | V phase output terminal on spindle motor driver |
| 21 | U | U phase output terminal on spindle motor driver |
| 22 | C-PUMP | To be attached the external integral constants for speed control of spindle motor |
| 23 | CLREF | Reference voltage input for current limiter of spindle motor driver |
| 24 | R1 | To be attached the external resistor for setting up the oscillation frequency of start-up circuitry and the gain of speed control loop of spindle motor driver |
| 25 | Vpss | Power supply for spindle motor driver |
| 26 to 35 | GND | Ground pins |
| 36 | $V_{ss}$ | Power supply for small signal block |
| 37 | LVI1 | Sensing input for power monitor circuitry |
| 38 | DELAY | To be attached the external capacitor to generate the delay time for power on reset signal |
| 39 | COMM | To be attached the external capacitor for setting up the oscillation frequency |
| 40 | POLSEL | To be selected the input status corresponding to the pole number of spindle motor |
| 41 | CNTSEL | To select the count Number of Speed Discriminator |
| 42 | CLOCK | Master clock input for this IC |
| 43 | READY | Output of speed lock detector for spindle motor |
| 44 | SPNENAB | To select the status of spindle motor driver |
| 45 | $\overline{POR}$ | Output of power on reset signal for HDD system |
| 46 to 55 | GND | Ground pins |
| 56 | VCMENAB | To select the status of VCM driver |
| 57 | GAIN | To select the Transfer conductance gm of VCM driver |

# HA13561F

## Pin Description (cont)

| Pin Number | Pin Name | Function |
|---|---|---|
| 58 | NC | No function |
| 59 | NC | ditto |
| 60 | COMPOUT | Comparator output to detect the direction of output current on VCM driver |
| 61 | VREF1 | Regulated voltage output to be used as reference of peripheral ICs |
| 62 | RESINH | Used for inhibiting the restart function of the spindle motor driver after power down |
| 63 | OPIN (+) | Non inverted input of OP.Amp. to be used for filtering the signal on PWMOUT |
| 64 | VCTL | OP. Amp. output, this signal is used as control signal for VCM driver output |
| 65 | OPIN (−) | Inverted input of OP.Amp. to be used for filtering the signal on PWMOUT |
| 66 to 75 | GND | Ground pins |
| 76 | LVI2 | Sensing input for power monitor circuitry |
| 77 | Vpsv | Power supply for VCM driver |
| 78 | RETPOW | Power supply for retract circuitry |
| 79 | $\overline{\text{RETON}}$ | To be attached the base terminal of external transistor for retracting |
| 80 | RS | Sensing input for output current on VCM driver |

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## Block Diagram

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## Truth Table

**Table 1    Truth Table (1)**

| SPNENAB | Spindle Driver |
|---------|----------------|
| H | ON |
| Open | Cut off |
| L | Braking |

**Table 2    Truth Table (2)**

| VCMENAB | VCM Driver |
|---------|-----------|
| H | ON |
| L | Cut off |

**Table 3    Truth Table (3)**

| OTSD | Spindle Driver | VCM Driver | Retract Driver |
|------|----------------|------------|----------------|
| not Active | See table 1 | See table 2 | Cut off |
| Active | Cut off | Cut off | ON |

**Table 4    Truth Table (4)**

| POLSEL | (D1) | Comment |
|--------|------|---------|
| H | — | Test Mode |
| Open | 1/12 | for 8 poles motor |
| L | 1/18 | for 12 poles motor |

**Table 5    Truth Table (5)**

| CNTSEL | CNT | Rotation Speed (at CLOCK = 5 MHz) |
|--------|-----|-----------------------------------|
| H | 2605 | 3,600 rpm |
| Open | 2084 | 4,500 rpm |
| L | 1736 | 5,400 rpm |

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**Table 6  Truth Table (6)**

| RESINH | Spindle Driver |
|--------|----------------|
| H | Inhibiting the restart after power down |
| L | Not inhibiting the restart after power down |

**Table 7  Truth Table (7)**

| GAIN | VCM Driver |
|------|------------|
| H | High Gain Mode |
| L | Low Gain Mode |

# HA13561F

## Timing Chart

### 1. Power on reset (1)



Note: 1. How to determine the threshold Voltage Vsd and the delay time $t_{DLY}$ both are shown in the external components table.

### 2. Power on reset (2)



Note: 2. Retract driver need B-EMF voltage or another power supply.

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### 3. Motor start-up seaquence

(a) Timing chart of start-up seaquence



Note *1. Speed lock detection range ΔNo is as follows.

ΔNo = 1.2% when CNTSEL=H
= 1.5% when CNTSEL=Open
= 1.8% when CNTSEL=L

*2. READY output goes to High, if the rotation speed error keeps to be less than ΔNo longer time than tdelay.

$$t_{delay} = \frac{500 \cdot 10^7}{f_{clk} [Hz]} \; [ms]$$

*3. The turning point of driving mode from switching synchronize to the turning point of READY output from Low to High.

(b) Retry circuitry for misstart-up



The HA13561F has the motor stop detector as shown hatching block. This function is monitoring the situation of the motor while the motor is running by B-EMF sensing. If the motor will be caused a misstarting up, the motor will be automatically restarted within 200 ms after the motor stopped. This function increase the reliability for the motor starting up.

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### 4. Braking & Shut down the Spindle Driver



Note:    The SPNENAB should be selected the open state after braking to reduce the supply current from Vps and $V_{SS}$.
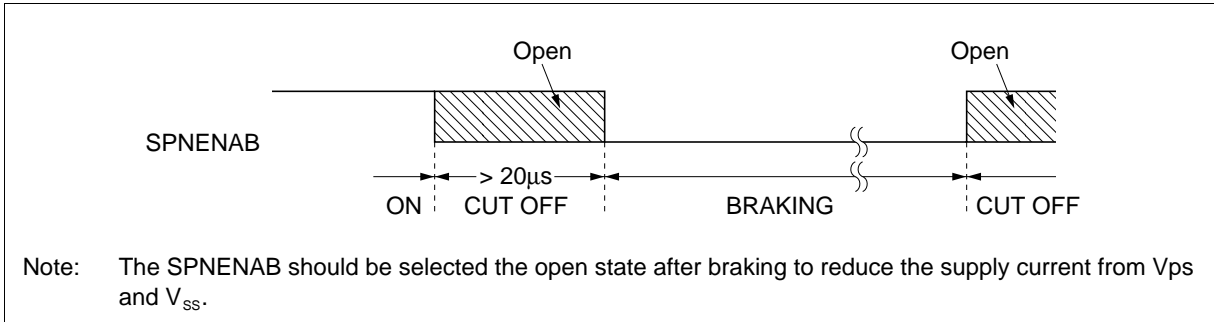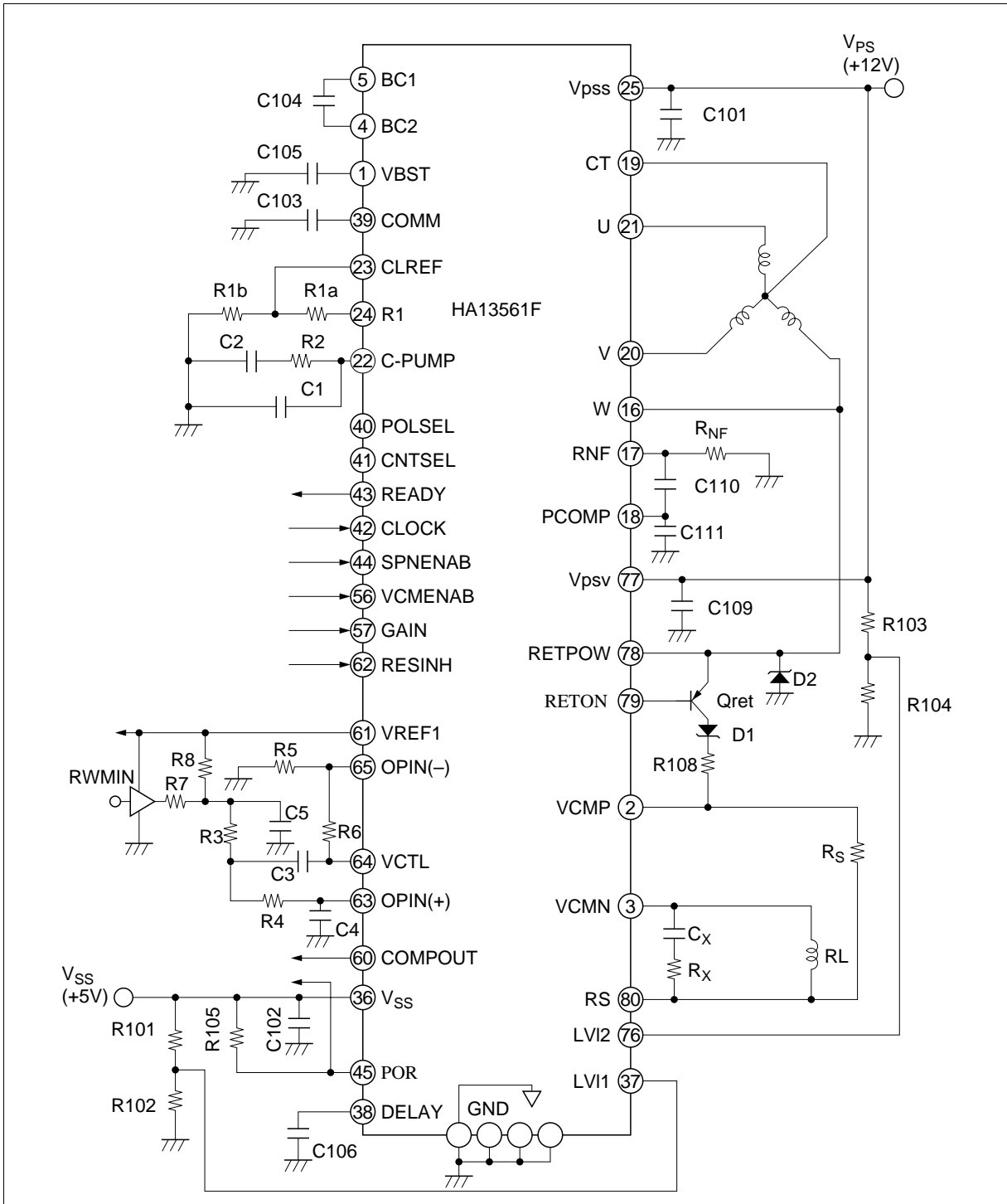
### 5. Start-up of the Spindle motor



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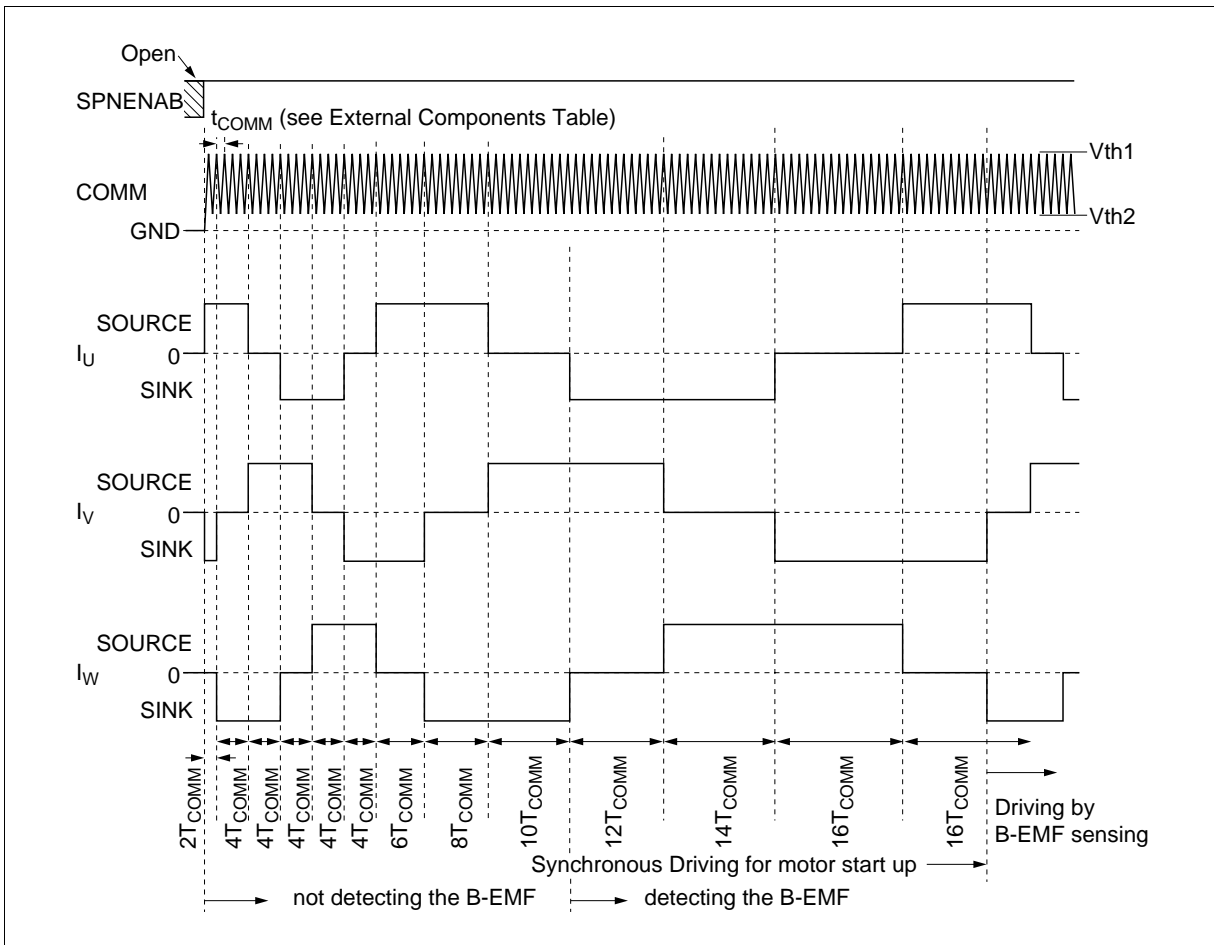
## 6. Acceleration and Running the spindle motor
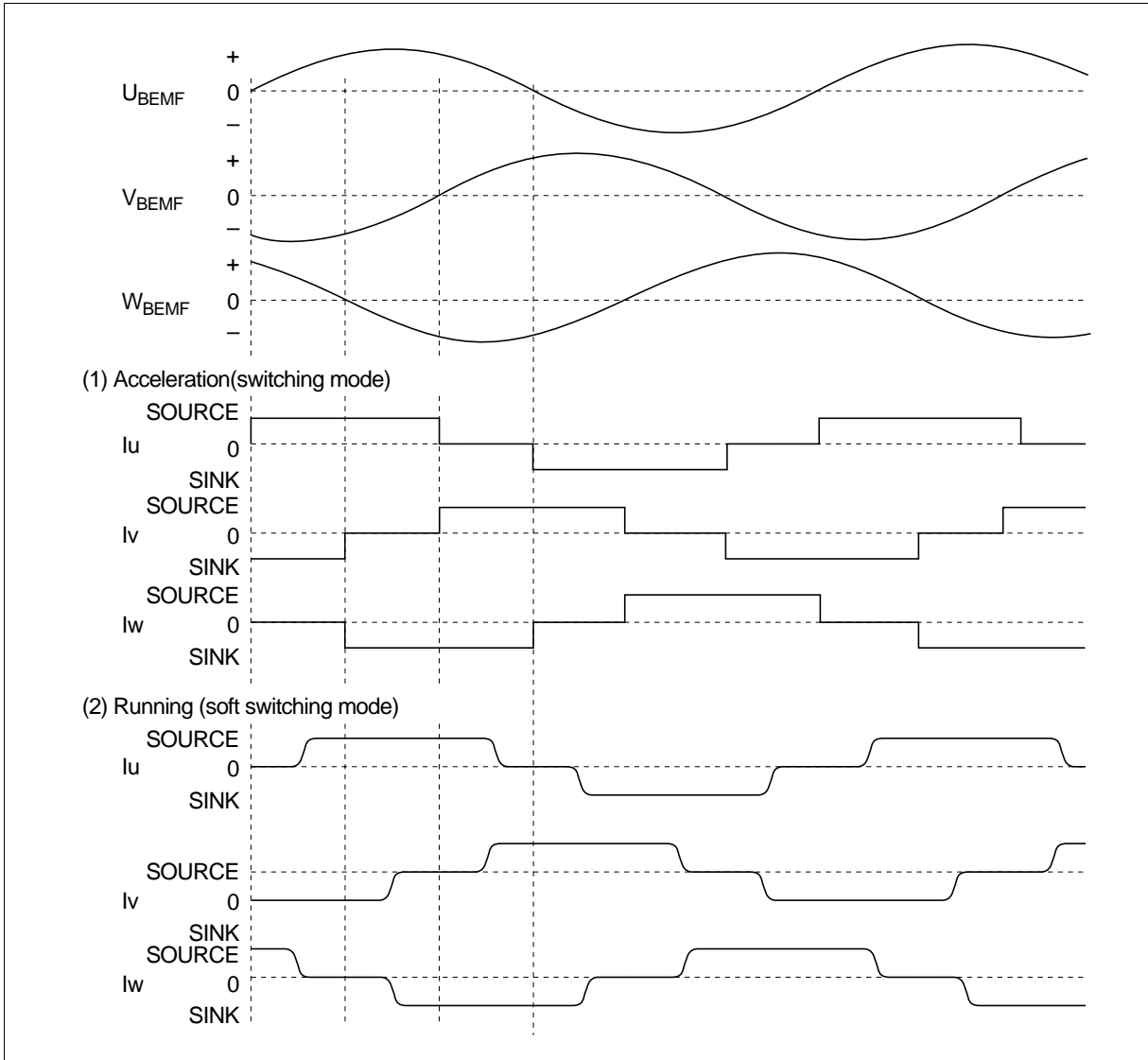
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## Application

## External Components

| Parts No. | Recommended Value | Purpose | Note |
|---|---|---|---|
| R1a | (R1a + R1b) ≥ 10 kΩ | V/I converter | 1, 4, 6 |
| R1b | (R1a + R1b) ≥ 10 kΩ | | |
| R2 | — | Integral constant | 3 |
| R3 to R8 | — | PWM filter | 9 |
| R101, R102 | — | Setting of LVI1 voltage | 7 |
| R103, R104 | — | Setting of LVI2 voltage | 7 |
| R105 | 5.6 kΩ | Pull up | |
| R108 | — | Limitation for Retract current | 12 |
| RS | 1.0 Ω | Current sensing for VCM Driver | 10 |
| Rnf | — | Current sensing for Spindle Driver | 1 |
| $R_x$ | — | Reduction for gain peaking | 11 |
| C1, C2 | — | Integral constant | 3 |
| C3 to C6 | — | PWM filter | 9 |
| $C_x$ | — | Reduction for gain peaking | 11 |
| C101 | ≥ 0.1 μF | Power supply by passing | |
| C102 | ≥ 0.1 μF | Power supply by passing | |
| C103 | — | Oscillation for start-up | 6 |
| C104 | 0.22 μF | for booster | |
| C105 | 2.2 μF | for booster | |
| C106 | — | Delay for POR | 8 |
| C109 | ≥ 0.1 μF | Power supply by passing | |
| C110, C111 | 0.33 μF | Phase compensation | |
| Qret | — | Retract Driver | 12 |
| D1 | — | Protection for Qret | 12 |
| D2 | TBD | Protection for parasitic phenomena | |

Notes: 1. Output maximum current on spindle motor driver Ispnmax is determined by following equation.

$$Ispnmax = \frac{R1b}{R1a + R1b} \cdot \frac{V_{R1}}{R_{NF}} \quad [A] \tag{1}$$

where, $V_{R1}$: Reference Voltage on Pin 24 [V] (= 1.3)

2. Input clock frequency fclk on pin 42 is determined by following equation.

$$fclk = \frac{4}{5} \cdot N_O \cdot P \cdot D1 \cdot (CNT - 0.5) \quad [Hz] \tag{2}$$

where, $N_O$: Standard rotation speed [rpm]
P: Number of pole
D1: Dividing ratio on divider 1

D1 = 1/12 (when Pin 40 = Open) for 8 pole motor

= 1/18 (when Pin 40 = Low) for 12 pole motor

CNT: Count number on speed discriminator

CNT = 2605 (when Pin 41 = High)

= 2084 (when Pin 41 = Open)

= 1736 (when Pin 41 = Low)

3. Integral constants R2, C1 and C2 can be designed as follows.

$$\omega_O = \frac{1}{10} \cdot 2 \cdot \pi \cdot \frac{N_O}{60} \qquad \text{[rad/s]}$$

(3)

$$R2 = \frac{1}{9.55} \cdot \frac{Rnf \cdot J \cdot \omega_O \cdot N_O \cdot (R1a + R1b)}{V_{R1} \cdot K_T \cdot Gctl} \qquad [\Omega]$$

(4)

$$C1 = \frac{1}{\sqrt{10} \cdot \omega_O \cdot R2} \qquad \text{[F]}$$

(5)

$$C2 = 10 \cdot C1 \qquad \text{[F]}$$

(6)

where, J: Moment of inertia [kg•cm•s$^2$]

$K_T$: Torque constant [kg•cm/A]

Gctl: Current control amp gain from pin 22 to pin 17 (= 0.5)

4. It is notice that rotation speed error Nerror is caused by leak current Icer2 on pin 22 and this error depend on R1a and R1b as following equation.

$$\text{Nerror} = \text{Icer2} \cdot \frac{(R1a + R1b)}{VR1} \cdot 100 \qquad \text{[\%]}$$

(7)

where, Icer2: leak current on pin 22 [A]

5. Oscillation period $t_{COMM}$ on pin 39 which period determine the start up characteristics, is should be chosen as following equation.

$$t_{COMM} = \frac{1}{8} \cdot \sqrt{\frac{J}{P \cdot K_T \cdot Ispnmax}} \quad \text{to} \quad \frac{1}{4} \cdot \sqrt{\frac{J}{P \cdot K_T \cdot Ispnmax}} \qquad \text{[s]}$$

(8)

6. The capacitor C103 on pin 39 can be determined by $t_{COMM}$ and following equation.

$$C103 = \frac{1}{4} \cdot \frac{VR1}{R1a + R1b} \cdot \frac{t_{COMM}}{Vth_H - Vth_L} \qquad \text{[F]}$$

(9)

where, $Vth_H$: Threshold voltage on start up circuit [V] (= 2.0)

$Vth_L$: Threshold voltage on start up circuit [V] (= 0.5)

7. LVI operatig voltage Vsd1, Vsd2 and its hysteresis voltage Vhys1, Vhys2 can be determined by following equations.

for $V_{SS}$

$$Vsd1 = \left(1 + \frac{R101}{R102}\right) \cdot Vth4 \qquad \text{[V]}$$

(10)

$$Vhys1 = \left(1 + \frac{R101}{R102}\right) \cdot Vhyspm \qquad \text{[V]}$$

(11)

for Vps

$$Vsd2 = \left(1 + \frac{R103}{R104}\right) \bullet Vth3 \qquad [V]$$

(12)

$$Vhys2 = \left(1 + \frac{R103}{R104}\right) \bullet Vhyspm \qquad [V]$$

(13)

where, Vth3, Vth4: Threshold voltage on pin 37 and pin 76 [V] (= 1.39)

Vhyspm: Hysteresis voltage on pin 37 and pin 76 [mV] (= 40)

Shut down voltage Vsd1, Vsd2 can be designed by the following range.

Vsd1 ≥ 4.25 [V], Vsd2 ≥ 10 [V]

8. The delay time $t_{DLY}$ of POR for power on reset is determined as follows.

$$t_{DLY} = \frac{C106 \bullet Vth5}{I_{CH3}} \qquad [s]$$

(14)

where, Vth4: Threshold voltage on pin 38 [V] (= 1.4)

$I_{CH3}$: Charge current on pin 38 [μA] (= 10)

9. The differential voltage (Vctl – $V_{REF1}$) using for control of VCM driver depend on PWMDAC inputs LSB, MSB as follows.

$$Vctl - V_{REF1} = 2 \bullet V_{REF1} \bullet \frac{D_{PWM} - 50}{100} \bullet \frac{R6}{R5} \bullet H_{FLT}(s)$$

(15)

where, $D_{PWM}$: Duty cycle on PWMIN [%]

$H_{FLT(S)}$: Transfer function from pin 62 (PWMOUT) to pin 64 (Vctl) as shown in equation (17)

To be satisfied with above equation (15), it is notice that the ratio of R6 to R7 must be choosen as shown below.

$$\frac{R8}{R7} = 2 \bullet \frac{R6}{R5} \bullet \frac{1}{1 - \frac{R6}{R5}}$$

(16)

$H_{FLT}(s)$

$$= \frac{1}{\left[\begin{array}{l} 1 + s \bullet \left[C5 \bullet R// - C3 \bullet (R// + R3) \bullet \frac{R6}{R5} + C4 \bullet (R// + R3 + R4)\right] \\ + s^2 \bullet \left[C5 \bullet C4 \bullet R// \bullet (R3 + R4) - C5 \bullet C3 \bullet R// \bullet R3 \bullet \frac{R6}{R5} + C3 \bullet C4 \bullet R4 \bullet (R// + R3)\right] \\ + s^3 \bullet C3 \bullet C4 \bullet C5 \bullet R// \bullet R3 \bullet R4 \end{array}\right]}$$

(17)

where, $$R// = \frac{R7 \bullet R8}{R7 \bullet R8}$$

(18)

If you choose the R// << R3, then equation (17) can be simplified as following equation.

$$H_{FLT}(s) = \frac{1}{1 + \frac{s}{\omega_O}} \bullet \frac{1}{1 + 2 \bullet \zeta \bullet \left(\frac{s}{\omega n}\right) + \left(\frac{s}{\omega n}\right)^2}$$

(19)

where,

$$\omega_O = \frac{1}{C5 \cdot R//} \tag{20}$$

$$\omega n = \frac{1}{\sqrt{C3 \cdot C4 \cdot R3 \cdot R4}} \tag{21}$$

$$\zeta = \frac{C4 \cdot (R3 + R4) - C3 \cdot R3 \cdot \frac{R6}{R5}}{2 \cdot \sqrt{C3 \cdot C4 \cdot R3 \cdot R4}} \tag{22}$$

10. The relationship between the output current Ivcm and the input voltage ($Vctl - V_{REF1}$) on VCM driver is as follows.

$$Ivcm(s) = \left(Vctl - V_{REF1}\right) \cdot Kvcm \cdot \frac{1}{Rs} \cdot Hvcm(s) \tag{23}$$

where,    Vctl:      Input control voltage for VCM driver on pin 64 [V]
            $V_{REF1}$:     Reference voltage on pin 61 [V] (= 4.6)
            Kvcm:     DC gain of VCM driver
                      (= 1.82 for High gain mode)
                      (= 0.45 for Low gain mode)
            Hvcm(s): Transfer function of VCM driver as shown following equation

$$Hvcm(s) = \frac{1}{1 + 2 \cdot \zeta_{VCM} \cdot \left(\frac{s}{\omega_{VCM}}\right) + \left(\frac{s}{\omega_{VCM}}\right)^2} \tag{24}$$

where,

$$\omega_{VCM} = \sqrt{\omega_P \cdot \frac{Rs}{Lm}} \tag{25}$$

$$\zeta_{VCM} = \frac{1}{2} \cdot \left(1 + \frac{R_L}{Rs}\right) \cdot \sqrt{\frac{1}{\omega_P} \cdot \frac{Rs}{Lm}} \tag{26}$$

where,   $\omega p$:   Bandwidth of internal power amplifiers for VCM driver [rad/s]
                (= $3 \cdot \pi \cdot 10^6$)
        Lm:   Inductance of the VCM coil [H]
        $R_L$:    Resistance of the VCM coil [$\Omega$]

and from above equations the -3 dB bandwidth $f_{VCMC}$ of VCM driver is as following equation.

$$f_{VCMC} = \frac{\omega_{VCM}}{2 \cdot \pi} \cdot \sqrt{\left[1 - 2 \cdot \zeta_{VCM}^2\right] + \sqrt{\left[2 \cdot \zeta_{VCM}^2 - 1\right]^2 + 1}} \tag{27}$$

11. The frequency response of VCM driver maybe have a gain peaking because of the resonation of the motor coil impedance. If you want to tune up for this characteristics, you can reduce the peaking by additional snubber circuit $R_x$ and $C_x$ as follows.
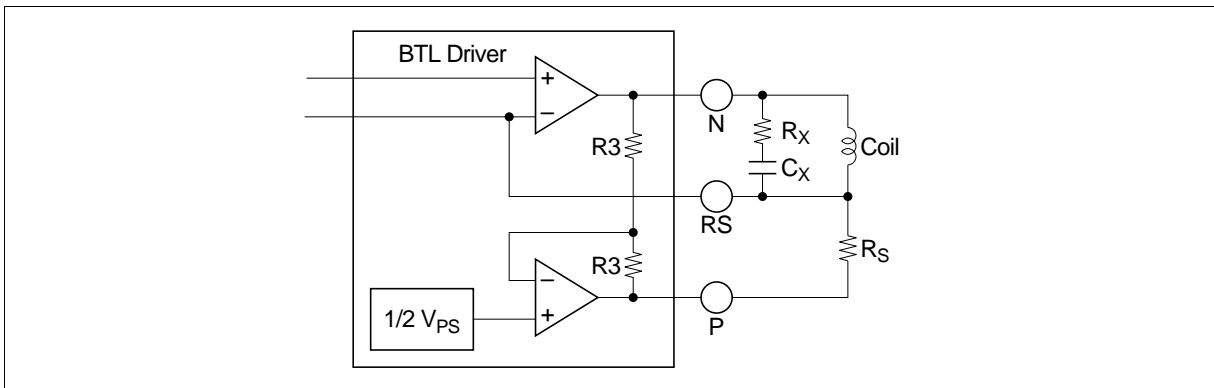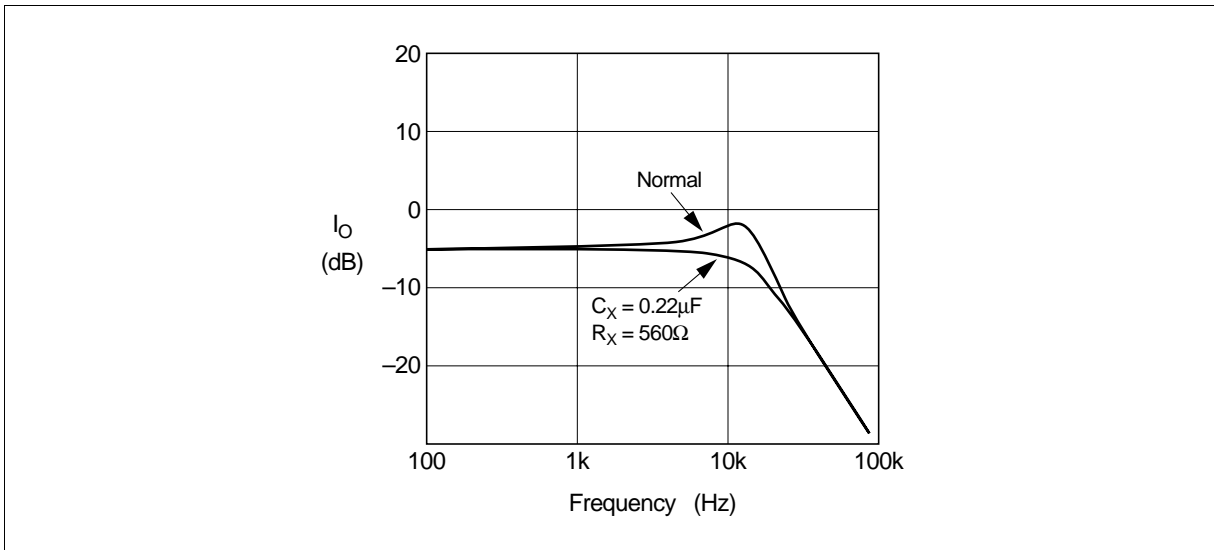


**Figure 1   VCM Driver Block Diagram**



(for example)   $R_L = 14.7\ \Omega$, $R_S = 1\ \Omega$, $L = 1.7$ mH, Gain = L

12. The retract current Iret is determined by following equation.

$$\text{Iret} = \frac{\text{Vretpow} - \text{Vsat(Qret)} - V_F(\text{D1}) - \text{Vsat}_{VL}}{\text{R108} + \text{Rs} + R_L}$$

(28)

where,  Vretpow:     Applied voltage on pin 78 [V]

Vsat (Qret): Saturation voltage of Qret [V]

$V_F$ (D1):     Foward voltage of D1 [V]

## Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Rating | Unit | Notes |
|---|---|---|---|---|
| Power supply voltage | Vps | +15 | V | 1 |
| Signal supply voltage | $V_{SS}$ | +7 | V | 2 |
| Input voltage | $V_{IN}$ | $V_{SS}$ | V | 3 |
| Output current-Spindle | Iospn (Peak) | 1.8 | A | |
| | Iospn (DC) | 1.2 | A | |
| Output current-VCM | Iovcm (Peak) | 1.2 | A | |
| | Iovcm (DC) | 0.8 | A | |
| Power dissipation | $P_T$ | 5 | W | |
| Junction temperature | Tj | +150 | °C | |
| Storage temperature | Tstg | −55 to +125 | °C | |

Notes: 1. Operating voltage range is 10.2 V to 13.8 V.

2. Operating voltage range is 4.25 V to 5.75 V

3. Applied to Pin 40, 41, 42, 44, 56, 57 and pin 62

4. Operating junction temperature range is Tjop = 0°C to +125°C

5. ASO of upper and lower power transistor are shown below.
   Operating locus must be within the ASO.

6. The OTSD (Over Temperature Shut Down) function is built in this IC to avoid same damages by over heat of this chip. However, please note that if the junction temperature of this IC becomes higher than the operating maximum junction temperature (Tjopmax = 125°C), the reliability of this IC often goes down.

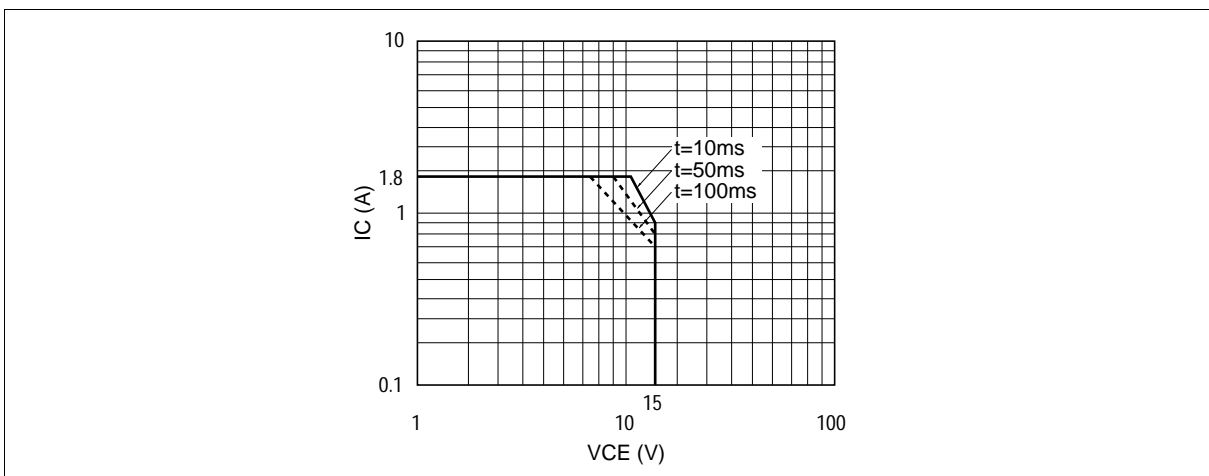7. Thermal resistance: $\theta$j-a $\leq$ 35°C/W with 6 layer multi glass-epoxy board.
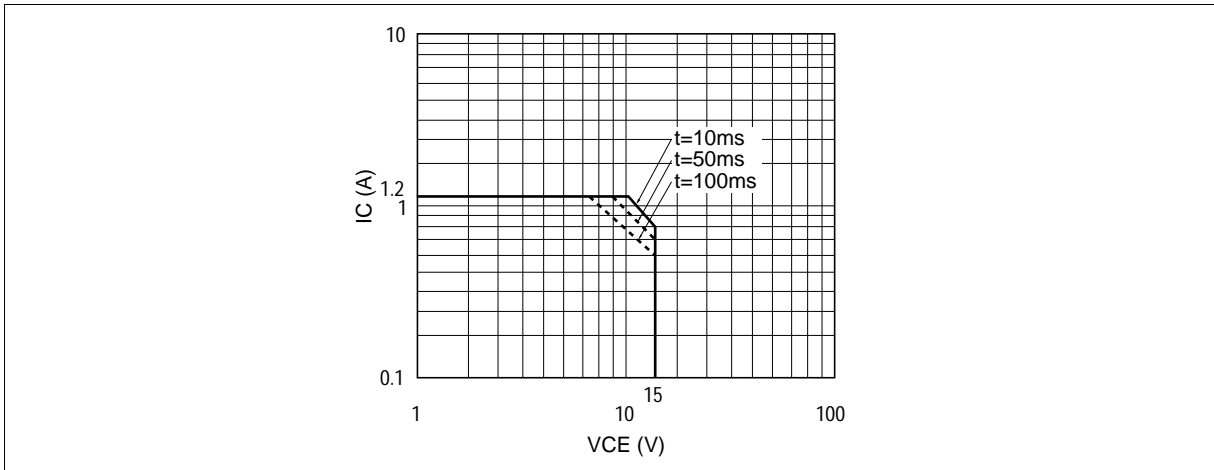


**Figure 2   ASO of Output Stages (Spindle)**

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**Figure 3   ASO of Output Stages (VCM)**

## Electrical Characteristics (Ta = 25°C, Vps = 12 V, $V_{SS}$ = 5 V)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Note |
|---|---|---|---|---|---|---|---|---|---|
| Supply current | for $V_{SS}$ | $I_{SS0}$ | — | 5.8 | 7.0 | mA | SPNENAB = Open VCMENAB = L | 36 | |
| | | $I_{SS1}$ | — | 21 | 27 | mA | SPNENAB = H VCMENAB = H | 36 | |
| | for Vps | Ips0 | — | 1.7 | 2.2 | mA | SPNENAB = Open VCMENAB = L | 25, 77 | |
| | | Ips1 | — | 19 | 24 | mA | SPNENAB = H VCMENAB = H | 25, 77 | |
| Logic input 1 (GAIN) (RESINH) | Input low voltage | $V_{IL1}$ | — | — | 0.8 | V | | 57, 62 | |
| | Input high voltage | $V_{IH1}$ | 2.0 | — | — | V | | | |
| | Input low current | $I_{IL1}$ | — | — | ±10 | µA | Input = GND | | |
| | Input high current | $I_{IH1}$ | — | — | ±10 | µA | Input = 5.0 V | | |
| Logic input 2 (CLOCK) | Input low voltage | $V_{IL2}$ | — | — | 0.8 | V | | 42 | |
| | Input high voltage | $V_{IH2}$ | 3.5 | — | — | V | | | |
| | Input low current | $I_{IL2}$ | — | −180 | −260 | µA | Input = GND | | |
| | Input high current | $I_{IH2}$ | — | 230 | 330 | µA | Input = 5.0 V | | |
| Logic input 3 (VCMENAB) | Input low voltage | $V_{IL3}$ | — | — | 0.8 | V | | 56, 59 | |
| | Input high voltage | $V_{IH3}$ | 2.0 | — | — | V | | | |
| | Input low current | $I_{IL3}$ | — | — | ±10 | µA | Input = GND | | |
| | Input high current | $I_{IH3}$ | — | — | 330 | µA | Input = 5.0 V | | |
| Logic input 4 (SPNENB) | Input low voltage | $V_{IL4}$ | — | — | 1.0 | V | | 44 | |
| | Input middle voltage | $V_{IM4}$ | 2.0 | — | 3.1 | V | | | |
| | Input high voltage | $V_{IH4}$ | 3.9 | — | — | V | | | |
| | Input low current | $I_{IL4}$ | −75 | −105 | −150 | µA | Input = GND | | |
| | Input high current | $I_{IH4}$ | 75 | 105 | 150 | µA | Input = 5.0 V | | |

## Electrical Characteristics (Ta = 25°C, Vps = 12 V, $V_{SS}$ = 5 V) (cont)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Note |
|---|---|---|---|---|---|---|---|---|---|
| Logic input 4 (SPNENB) | Input dead current | $I_{DEAD}$ | — | — | ±10 | µA | | 44 | |
| Logic input 5 (POLSEL) (CONTSEL) | Input low voltage | $V_{IL5}$ | — | — | 1.0 | V | | 40, 41 | |
| | Input middle voltage | $V_{IM5}$ | 2.0 | — | 3.1 | V | | | |
| | Input high voltage | $V_{IH5}$ | 3.9 | — | — | V | | | |
| | Input low current | $I_{IL5}$ | −38 | −53 | −75 | µA | Input = GND | | |
| | Input high current | $I_{IH5}$ | 38 | 53 | 75 | µA | Input = 5.0 V | | |
| Spindle driver | Total saturation voltage | Vsatspn | — | 0.8 | 1.1 | V | Ispn = 1.0 A | 16, 20, 21 | |
| | | | — | — | 0.5 | V | Ispn = 0.35 A | | |
| | Saturation at braking | Vbreak | — | — | 0.7 | V | Ibreak = 0.6 A | | |
| | Leak current | Icer1 | — | — | ±2.0 | mA | SPNENAB = Open | | |
| | Current limiter reference voltage | $V_{OCL}$ | 430 | 480 | 530 | mV | $V_{CLREF}$ = 500 mV $R_{NF}$ = 1.0 Ω | 17 | |
| | Control amp gain | Gctl | — | −2 | ±2 | dB | $R_{NF}$ = 1.0 Ω | 17, 22 | |
| B-EMF amp. | Input sensitivity | Vmin | — | 100 | — | mVp-p | | 16, 20, 21 | 1 |
| Charge pump | Reference voltage | VR1 | 1.06 | 1.17 | 1.28 | V | R1a + R1b = 24 Ω C-PUMP = 1.0 V | 22, 24 | |
| | Charge current | $I_{CH1}$ | 40 | 45 | 50 | µA | | | |
| | Discharge current | $I_{DIS1}$ | −40 | −45 | −50 | µA | | | |
| | Leak current | Icer2 | — | — | ±50 | nA | | | |
| Speed discri | Operating frequency | fclk | — | — | 8.0 | MHz | | 42 | |
| Start up circuit | Threshold voltage | $Vth_H$ | 1.6 | 1.8 | 2.0 | V | | 24, 39 | |
| | | $Vth_L$ | 0.3 | 0.5 | 0.7 | V | | | |
| | Charge current | $I_{CH2}$ | 21 | 23 | 26 | µA | R1a + R1b = 24 kΩ COMM = 1 V | | |
| | Discharge current | $I_{DIS2}$ | −19 | −22 | −25 | µA | | | |

## Electrical Characteristics (Ta = 25°C, Vps = 12 V, $V_{SS}$ = 5 V) (cont)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Note |
|---|---|---|---|---|---|---|---|---|---|
| READY | Output high voltage | Vohr | $V_{SS}$ − 0.4 | — | $V_{SS}$ | V | $I_O$ = −1 mA | 43 | |
| | Output low voltage | Volr | — | — | 0.4 | V | $I_O$ = 1 mA | | |
| VCM driver | Total saturation voltage | Vsatvcm | — | 0.8 | 1.1 | V | Ivcm = 0.8 A | 2, 3 | |
| | | | — | 0.4 | 0.55 | V | Ivcm = 0.4 A | | |
| | Output leak current | Icer3 | — | — | ±2 | mA | Vce = 15 V | | |
| | Total output offset voltage | Voff(H) | — | — | ±20 | mV | $V_{CTL}$ = OP (−) $V_{REF}$ = OP (+) | 2, 80 | |
| | | Voff(L) | — | — | ±10 | mV | | | |
| | Output quiescent voltage | Vqvcm | 5.6 | 6.0 | 6.4 | V | $R_L$ = 10 Ω $R_S$ = 1.0 Ω | 2, 3 | |
| | Total Gain Bandwidth | B | — | 26 | — | kHz | $R_S$ = 1.0 Ω, $R_L$ = 28 Ω | 2, 3 | 1 |
| | | | — | 50 | — | kHz | $R_S$ = 1.0 Ω, $R_L$ = 14 Ω | | |
| | Transfer gain | gm (H) | — | 1.74 | ±5% | A/V | Higain-mode $R_S$ = 1.0 Ω, $R_L$ = 14 Ω | 2, 64, 80 | |
| | | gm (L) | — | 0.44 | ±5% | A/V | Logain-mode $R_S$ = 1.0 Ω, $R_L$ = 14 Ω | | |
| Retract driver | Retpow voltage | Vretpow | 0.8 | — | — | V | Ireton = 0.1 mA | 78 | |
| | Retout sink current | Ireton | 5 | 8 | — | mA | Vretpow = 4.0 V | | |
| | Output leak current | Icer4 | — | — | ±10 | μA | Vreton = 15 V, Vretpow = 15 V | 79 | |
| | Low side saturation voltage | VsatVL | 0.1 | 0.23 | 0.35 | V | Iret = 0.1 A | 3 | |
| OP Amp | Input current | Iinop | — | — | ±500 | nA | | 63, 65 | |
| | Input offset voltage | Vosop | — | — | (±7) | mV | | | 1 |
| | Common mode input voltage range | Vcmop | 0 | — | Vps − 0.2 | V | | | |
| | Output high voltage | Vohop | Vps − 1.3 | — | — | V | Iout = 1.0 mA | 64 | |

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**Electrical Characteristics** (Ta = 25°C, Vps = 12 V, $V_{SS}$ = 5 V) (cont)

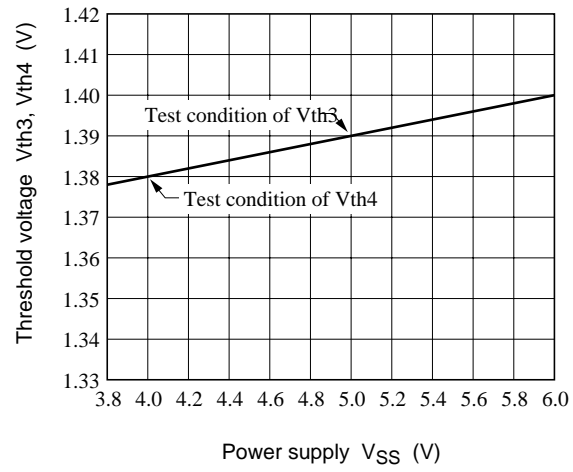| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Note |
|---|---|---|---|---|---|---|---|---|---|
| OP Amp | Output low voltage | Volop | — | — | 1.1 | V | Iout = 1.0 mA | 64 | |
| Comparator | Input sensitivity | Vmin2 | ±9 | 0 | — | mV | | 2, 3, 60 | |
| | Output low voltage | Volcp | — | — | 0.4 | V | $I_O$ = 1 mA | 60 | |
| | Output high voltage | Vohcp | $V_{SS}$ – 1.8 | — | $V_{SS}$ | V | $I_O$ = 1 mA | | |
| Vref1 | Output voltage | Vref1 | — | 4.6 | ±3% | V | $I_O$ = 20 mA | 61 | |
| | Output resistance | Ro1 | — | — | 5.0 | Ω | $I_O$ = 20 mA | | |
| Power monitor | Threshold voltage | Vth3 | — | 1.39 | +3% −2% | V | $V_{SS}$ = 5 V | 76 | 2 |
| | Hysteresis | Vhyspm 1 | 25 | 40 | 55 | mV | $V_{SS}$ = 5 V | | |
| | Threshold voltage | Vth4 | — | 1.38 | +3% −2% | V | $V_{SS}$ = 4 V | 37 | 2 |
| | Hysteresis | Vhyspm 2 | 25 | 40 | 55 | mV | $V_{SS}$ = 4 V | | |
| POR | Output low voltage | $V_{OL2}$ | — | — | 0.4 | V | $I_O$ = 1 mA | 45 | |
| | | $V_{OL3}$ | — | — | 0.4 | V | $I_O$ = 1 mA $V_{SS}$ = Vps = 1.0 V | | |
| | Output leak current | Icer5 | — | — | ±10 | µA | Vpor = 7 V | | |
| | Threshold voltage | Vth5 | — | 1.4 | ±5% | V | | 38 | |
| | Charge current | $I_{CH3}$ | — | 12 | ±25% | µA | | | |
| | Discharge current | $I_{DIS3}$ | 10 | — | — | mA | | | |
| OTSD | Operating temperature | Tsd | 125 | 150 | — | °C | | | 1 |
| | Hysteresis | Thys | — | 25 | — | °C | | | 1 |

Notes: 1. Design guide only.
2. Variations of threshold voltage Vth3 and Vth4 depending on the power supply $V_{SS}$ are shown in Figure.4.

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**Figure 4**

## Package Dimensions

Unit: mm



| Hitachi code | FP-80E |
|---|---|
| EIAJ code | — |
| JEDEC code | — |

17.2 ± 0.3

□14

60    41

61    40

0.65

80    21

1    20

0.30 ± 0.10

$\oplus$ 0.13 Ⓜ

2.70 $^{+0.20}_{-0.16}$

3.05 Max

0.17 ± 0.05

1.60

0 – 5 °

0.8 ± 0.3

0.10

0.10

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