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# HA13705C

IPIC (Intelligent Power IC) High Side Solenoid Driver

# HITACHI

ADE-207-207 (Z)

1st Edition

July 1996

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## Description

The HA13705C is high side power driver IC with protectors and diagnostic function. The device is especially designed to switch inductive loads.

## Functions

- Power MOS source follower output (2 A)
- With Over Voltage Shut Down circuit (OVSD)
- With Over Current protector circuit (OCSD)
- With Over Temperature Shut Down circuit (OTSD)
- With diagnostic circuit and status output
- With fail safe function under input open circuit condition
- With low voltage inhibit circuit (LVI)
- With output negative voltage clamp circuit

## Features

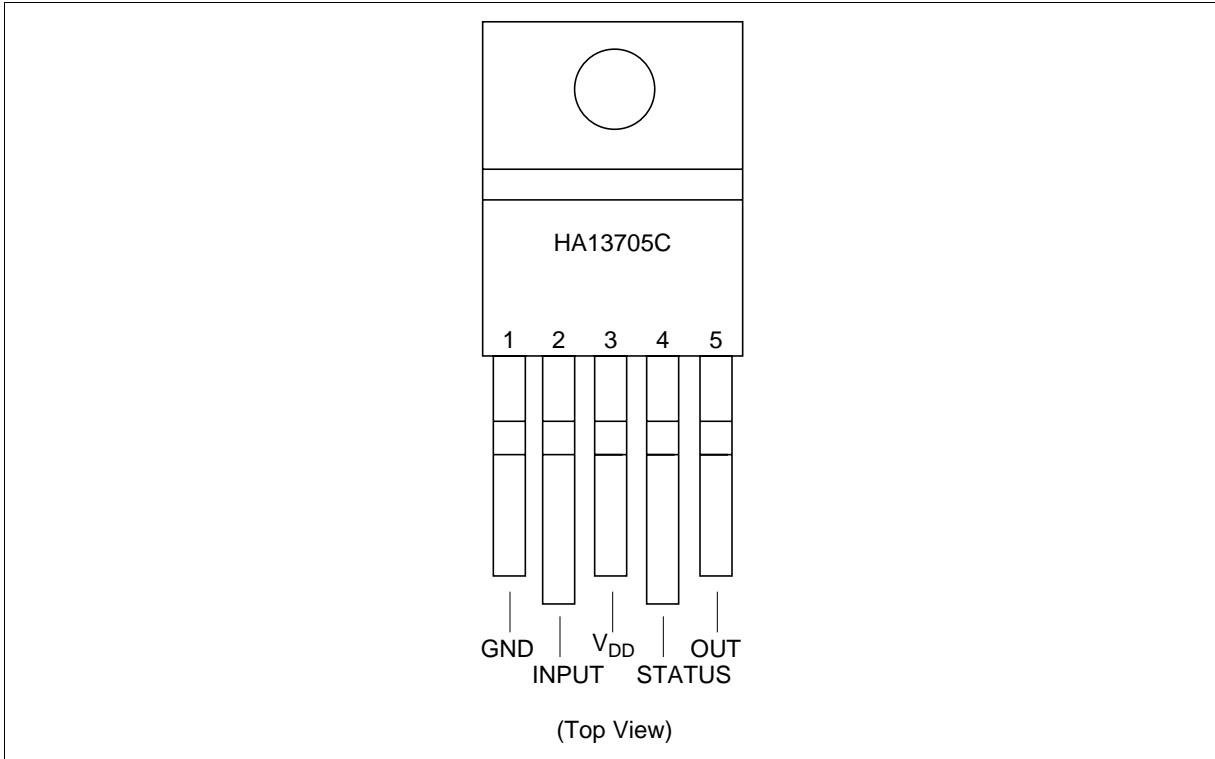
- Protected against 60 V load dump condition
- Low  $R_{ON}$  (0.17  $\Omega$  Typ)
- Wide operating supply voltage range ( $V_{DD} = 7$  V to 25 V)
- High sustaining voltage ( $-25$  V)
- Protected against reverse supply voltage ( $-13$  V)
- Protected against short circuit condition
- Input compatible with TTL, LS-TTL, or 5 V CMOS

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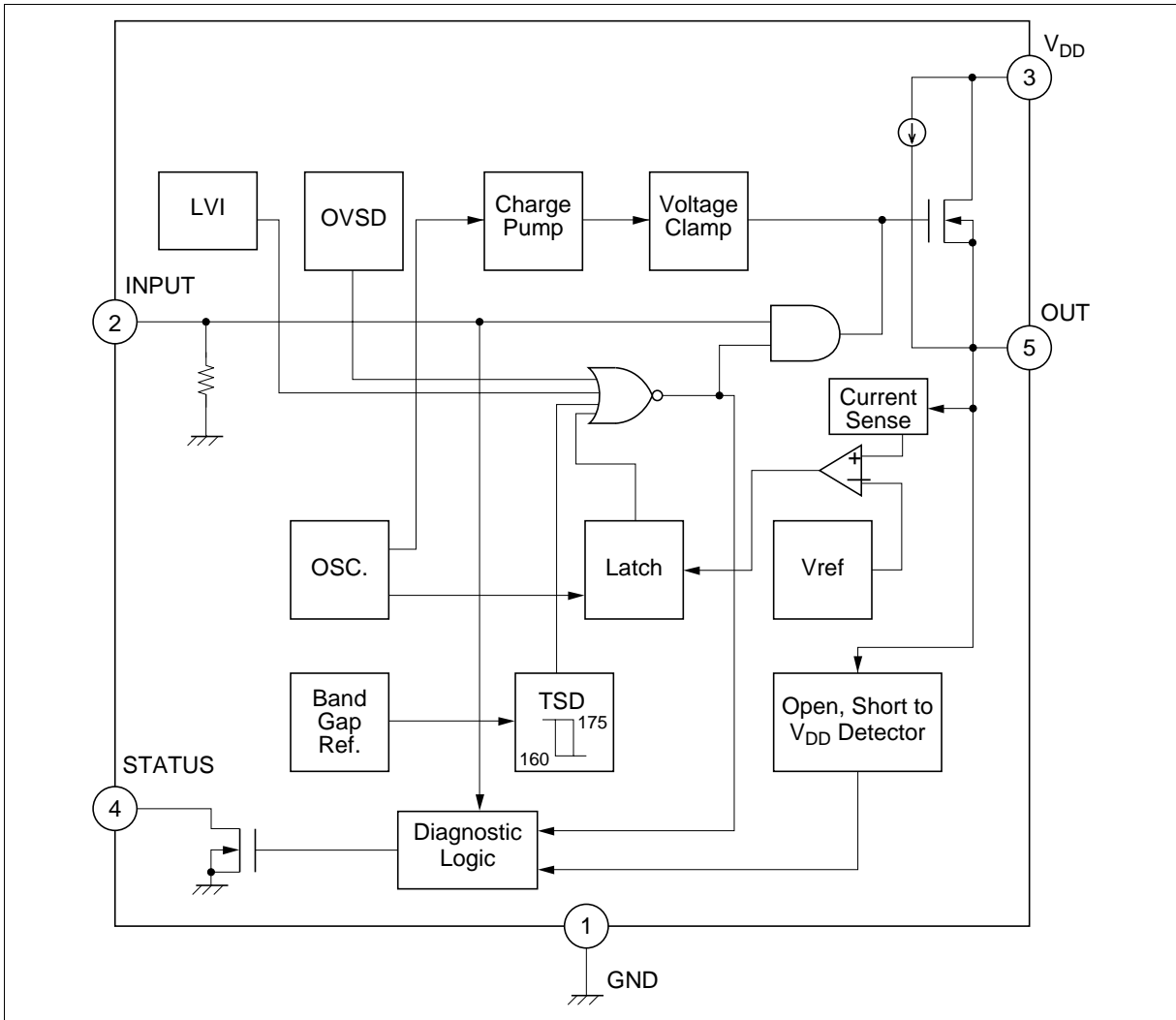
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## Pin Arrangement



Block Diagram



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### Truth Table

Mode	In	Out	Status
Normal	L	L	L
	H	H	H
Load short	L	L	L
	H	L	L
Load open	L	H	H
	H	H	H
Short to $V_{DD}$	L	H	H
	H	H	H
OTSD <sup>1</sup>	L	L	L
	H	L	L
OVSD <sup>2</sup>	L	L	H
	H	L	H
LVI <sup>3</sup>	L	L	H
	H	L	H

L : Low level (0.8 V)

H : High level (2.0 V)

Notes: 1. OTSD: Over temperature shut down  
2. OVSD: Over voltage shut down  
3. LVI: Low voltage inhibit

**Absolute Maximum Ratings** (Ta = 25°C)

Item	Symbol	Rating	Unit	Notes
Continuous supply voltage	V <sub>DD</sub>	-13 to 35	V	1
Transient supply voltage	V <sub>DD</sub>	60	V	2
Input voltage	V <sub>IN</sub>	-0.3 to 30	V	
Output voltage	V <sub>out</sub>	-25 to V <sub>DD</sub>	V	3
Status voltage	V <sub>s</sub>	-0.3 to +15	V	
Output current	I <sub>out</sub>	—	A	3, 4
Status current	I <sub>s</sub>	5	mA	
Power dissipation	P <sub>T</sub>	—	W	5
Package thermal resistance/ Junction to case	θ <sub>j-c</sub>	5	°C/W	
Package thermal resistance/ Junction to air	θ <sub>j-a</sub>	70	°C/W	
Junction temperature range	T <sub>j</sub>	-40 to 150	°C	
Storage temperature range	T <sub>stg</sub>	-55 to +150	°C	

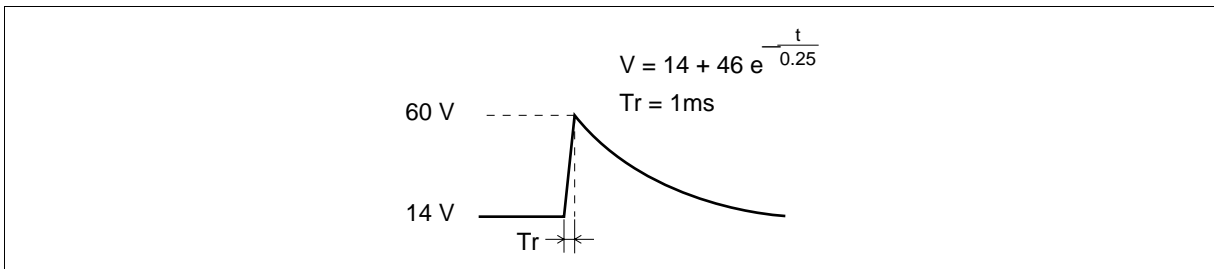
Notes: 1. Recommended operating voltage:

V<sub>DD</sub> = 7 to 16 V (Normal)

16 to 25 V (Jump up start 5 minutes MAX)

-13 V (Reverse Battely 5 minutes MAX)

2. Load dump condition

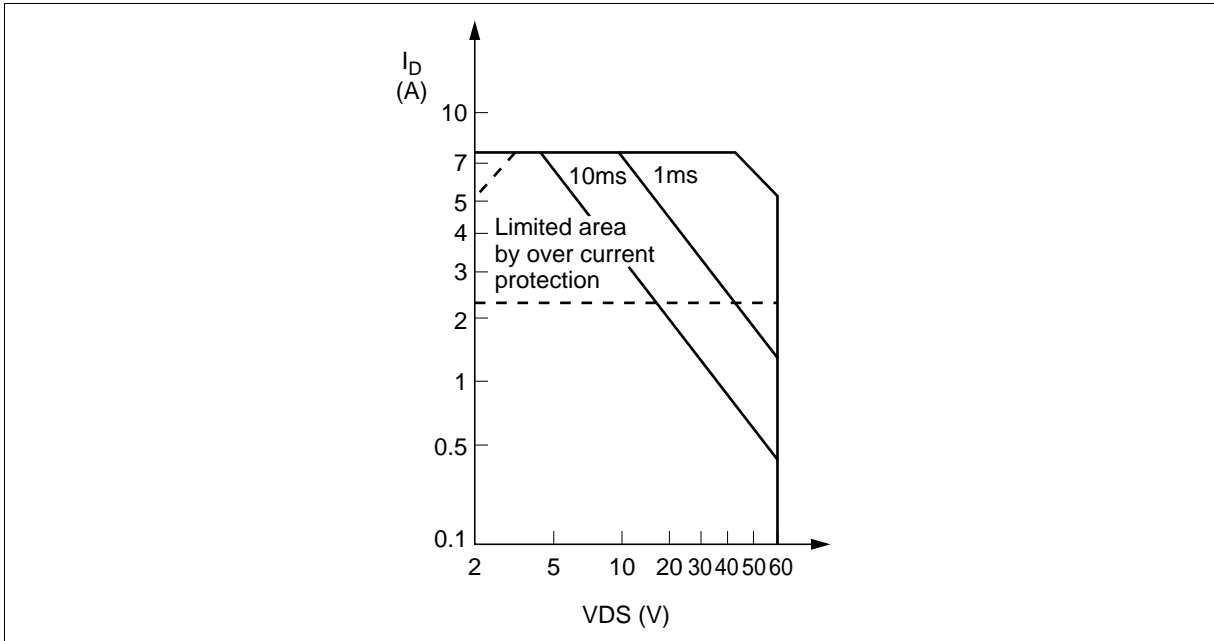


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### 3. Output Transistor ASO (Reference Data)



4. Internally limited

5. Maximum power dissipation ( $P_T$  (Max)) can be defined as:

$$P_T \text{ (Max)} = (T_{jopr}(\text{Max}) - T_{\text{ambient}}) / (\theta_{j-c} + \theta_{c-a})$$

$\theta_{c-a}$ : Thermal resistance between case and air (Depend on heat sink size)

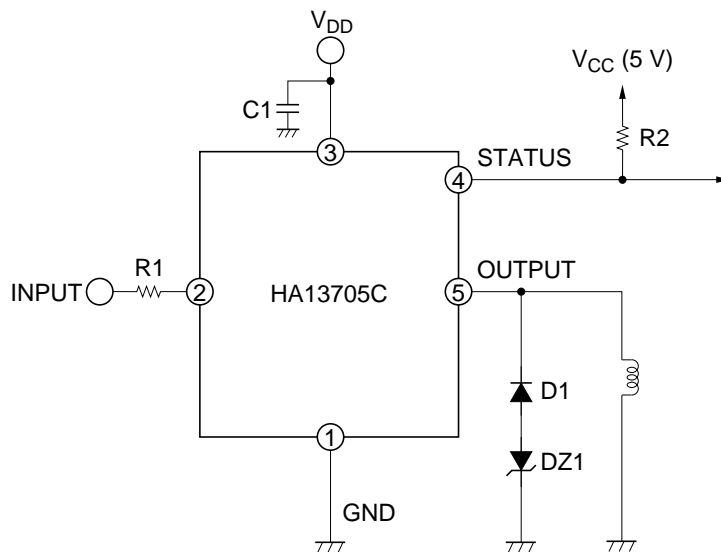
**Electrical Characteristics** (Ta = 25°C, V<sub>CC</sub> = 12 V ±10%)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Pin	Note	
Output R (ON)	R <sub>DS(ON)</sub>	—	0.17	0.36	Ω	I <sub>O</sub> = 2 A (@T <sub>J</sub> = -40 to 150°C)	5		
Operating supply voltage range	V <sub>DD</sub>	7	—	25	V		3		
Quiescent current	I <sub>DD1</sub>	—	—	0.3	mA	V <sub>IN</sub> = 0 V, V <sub>out</sub> = 0 V	3		
	I <sub>DD2</sub>	—	6.0	10.0	mA	V <sub>IN</sub> = 5.5 V, V <sub>out</sub> = open	3		
Output leakage current	I <sub>LEAK</sub>	—	—	0.1	mA	V <sub>DD</sub> = 25 V, V <sub>IN</sub> = 0 V, V <sub>out</sub> = 0 V	5		
Input threshold voltage	V <sub>IL</sub>	—	—	0.8	V		2		
	V <sub>IH</sub>	2.0	—	—	V		2		
Input current	I <sub>IL</sub>	-10	—	60	μA	V <sub>IN</sub> = 0.8 V	2		
	I <sub>IH</sub>	50	—	300	μA	V <sub>IN</sub> = 5.0 V	2		
Propagation delay time	t <sub>d(ON)</sub>	—	—	50	μs	I <sub>O</sub> = 1 A	2, 5		
	t <sub>r</sub>	—	—	90	μs		5		
	t <sub>d(OFF)</sub>	—	—	50	μs		2, 5		
	T <sub>f</sub>	—	—	50	μs		5		
Open det. threshold current	I <sub>OD</sub>	2	10	100	μs		4, 5		
Current limiter operating level	I <sub>CS</sub>	3.0	4.3	7.5	A		5		
LVI operating level	L.V.I	—	5	6	V		3		
Over voltage shut down	Operating level	OVSD	26	29	33	V		3	
	Hysteresis	VHYS	0.15	0.5	1.5	V		3	
Output sustain voltage	V <sub>(SUS)</sub>	—	—	-25	V	I <sub>out</sub> = 20 mA	5		
Over temperature shut down	Operating level	OTSD	150	175	—	°C		5	1
	Hysteresis	THYS	—	15	—	°C		5	1
Status on voltage	V <sub>SL</sub>	—	—	0.4	V	I <sub>S</sub> = 1 mA	4		
Status leakage current	I <sub>S(Leak)</sub>	-10	—	100	μA	V <sub>S</sub> = 5.0 V	4		

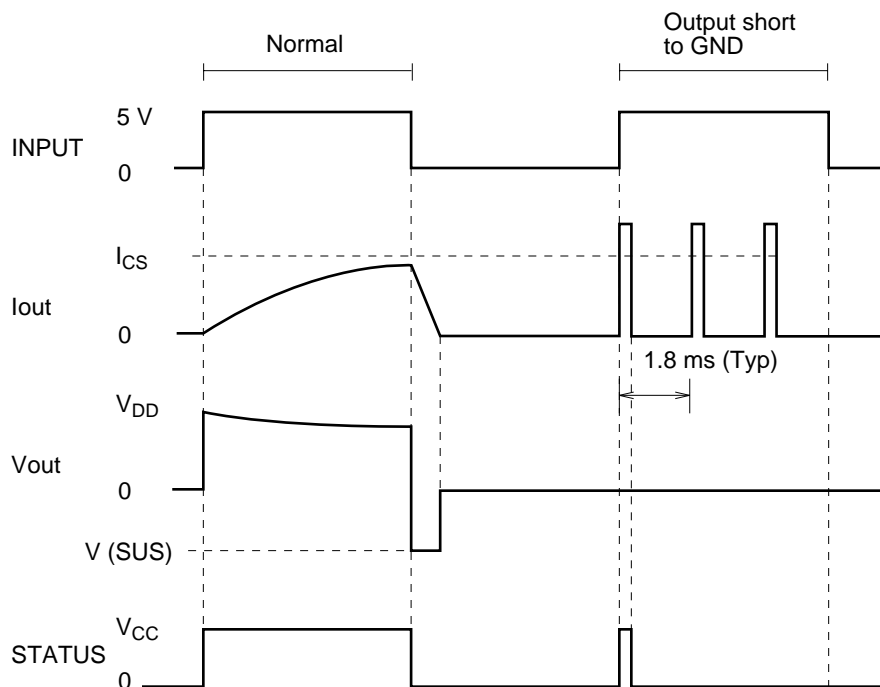
Notes: 1. Design parameter only (no test)

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## Solenoid Drive Application and it's Waveform



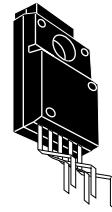
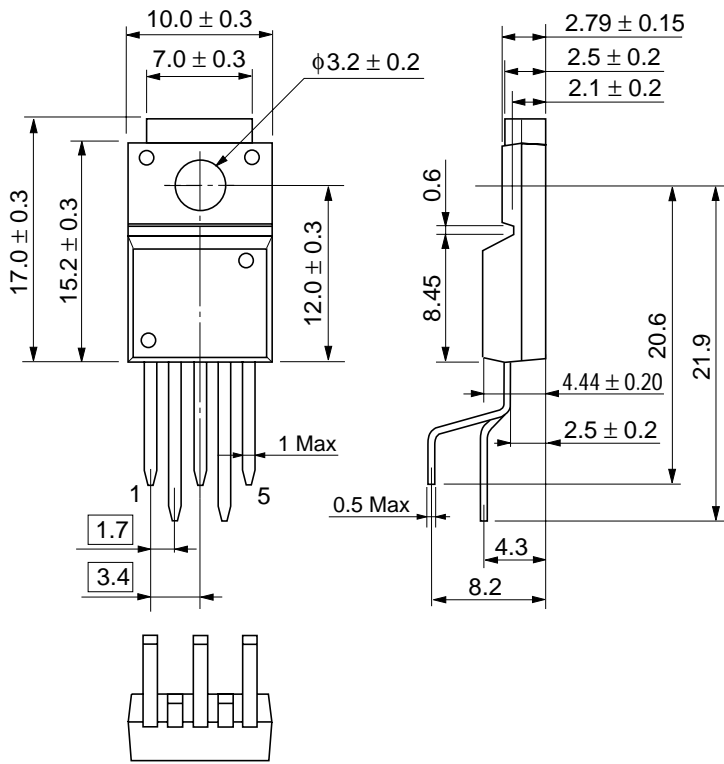
- R1 : Input series resistance to protect CMOS driver.
- R2 : Pull up resistance at status output.
- C1 : The capacitor to compensate the inductance at  $V_{DD}$  line.
- D1, DZ1 : for Reverse voltage clamp





Package Dimensions

Unit: mm



Hitachi Code	SP-5TA
JEDEC	—
EIAJ	—
Weight (reference value)	2.0 g

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