
HA16103 FPJ/FPK

Watchdog Timer

HITACHI

Description

The HA16103FPJ/FPK monolithic voltage control is designed for microcomputer systems. In addition to voltage regulator, it includes watch dog timer function, power on reset function, and output voltage monitor function.

It is suitable for battery use microcomputer systems.

Functions

- 5 V regulated power supply
- Power on reset pulse generator
- Watch dog timer
- Low voltage inhibit protection

Features

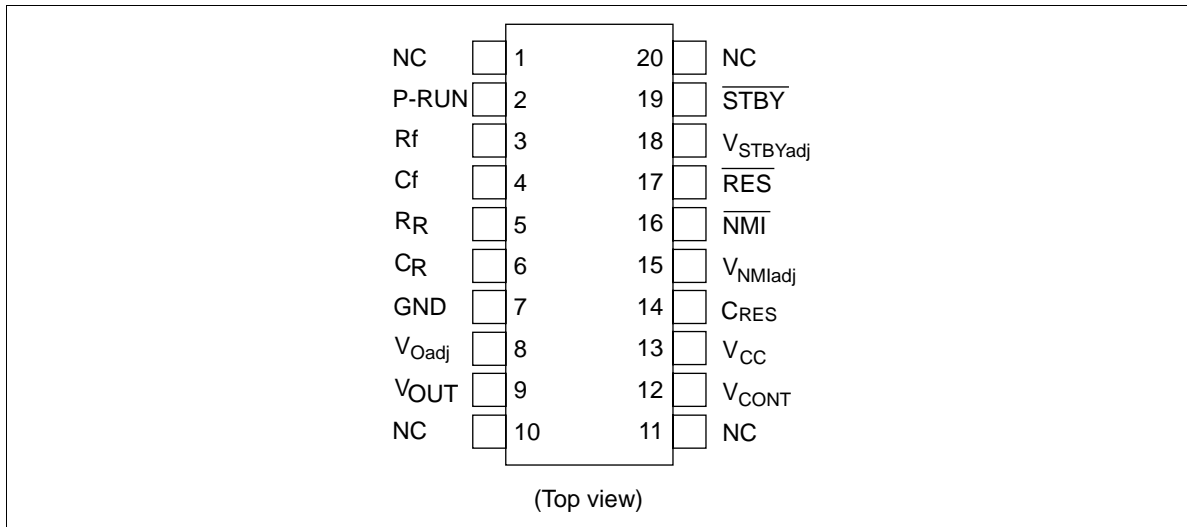
- Wide operational supply voltage range ($V_{CC} = 6$ to 40 V)
- Various control signals are generated when microcomputer system runaway occurs. (\overline{NMI} signal and \overline{STBY} signal are generated by detecting voltage level, and \overline{RES} signal is generated by monitoring the time after \overline{NMI} signal is detected)
- Regulated voltage, \overline{NMI} detecting voltage, \overline{STBY} detecting voltage are adjustable.
- At low voltage and re-start, the delay time of \overline{RES} signal is adjustable
- Watchdog timer filtering uses the minimum clock input pulse width and maximum cycle detection method

Ordering Information

Type No.	Package
HA16103FPJ	FP-20DA
HA16103FPK	FP-20DA

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Pin Arrangement

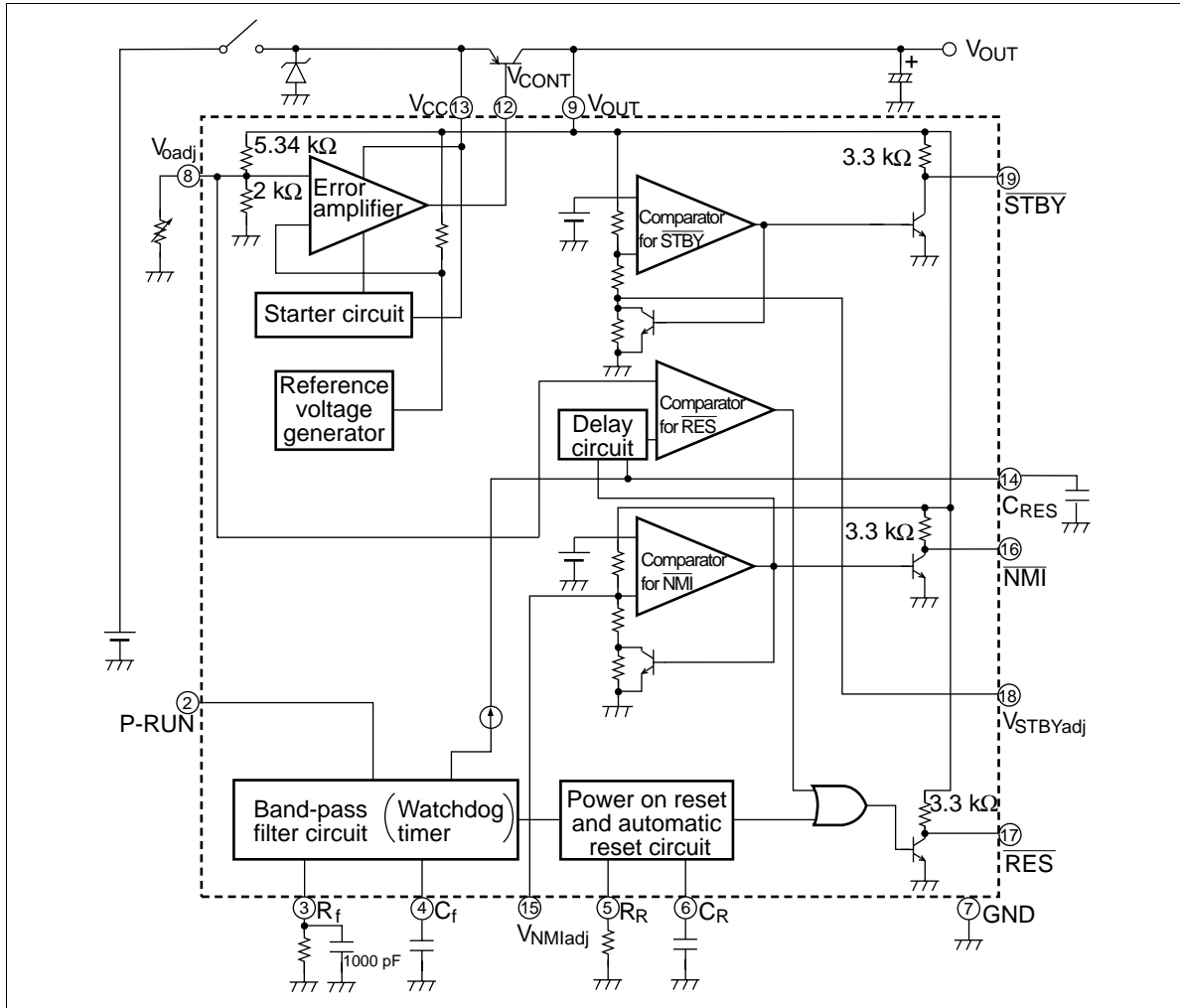


Pin Functions

No.	Pin Name	Description
1	NC	NC pin
2	P-RUN	P-RUN signal input pin for watchdog timer
3	Rf	Connect resistor Rf. Frequency bandwidth of the filter circuit depends on Rf
4	Cf	Connect resistor Cf. Frequency bandwidth of the filter circuit depends on Cf
5	R _R	Connect resistor R _R . Reset-signal power-on time depends on R _R
6	C _R	Connect resistor C _R . Reset-signal power-on time depends on C _R
7	GND	Ground
8	V _{oadj}	5-V reference voltage fine-tuning pin. Connect a resistor between this pin and GND. The value of output voltage is given by $V_{OUT} = \{1 + 5.34/(R1 // 2.0)\} \times V_{oadj}$ Unit for R1: kΩ
9	V _{OUT}	Connect the collector of an external PNP-type transistor. The pin supplies 5-V regulated voltage for internal circuit
10	NC	NC pin
11	NC	NC pin
12	V _{CONT}	The external PNP-type transistor's base control pin
13	V _{CC}	Supply voltage pin. Operating supply voltage range is 6.0 to 40 V.
14	C _{RES}	If the voltage of V _{OUT} pin declines to less than Detection voltage(1) (because of an instant power cut or other cause), \overline{NMI} signals are generated. If $t_{RES} \approx 0.5 \cdot Rf \cdot C_{RES}$ (sec) has passed since then, \overline{RES} signals are generated. If the voltage of V _{OUT} pin inclines to more than Detection voltage(1) (in case of re-start from LVI state), \overline{NMI} signals are stop. $t_r \approx 0.5 \cdot Rf \cdot C_{RES}$ (sec) has passed since then, \overline{RES} signals are stop. Connect capacitor C _{RES} between this pin and GND to adjust the \overline{RES} signals delay time(t_{RES} , t_r). If delay time is unnecessary, make this pin open ($t_{RES} = 2 \mu s$ typ. $t_r = 10 \mu s$ typ. at open)
15	V _{NMIadj}	\overline{NMI} detection voltage fine-tuning pin. Connect a resistor between this pin and V _{OUT} pin or GND. The value of output voltage is given by $V_{NMI} = \{1 + (R2 // 25.5)/(R3 // 10.6)\} \times V_{NMIadj}$. Unit for R2, R3: kΩ
16	\overline{NMI}	\overline{NMI} signal output pin. Connect to pin \overline{NMI} of the microcomputer
17	\overline{RES}	\overline{RES} signal output pin. Connect to pin \overline{RES} of the microcomputer
18	V _{STBYadj}	\overline{STBY} detection voltage tuning pin. Connect a resistor between this pin and V _{OUT} or GND. The value of output voltage is given by $V_{STBY} = 1.89 \times \{1 + 21/(7.9 + 8.85 // R4)\} \times V_{STBYadj}$ Unit for R4: kΩ
19	\overline{STBY}	\overline{STBY} signal output pin. Connect to pin \overline{STBY} of the microcomputer
20	NC	NC pin

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Block Diagram



Functional Description

Stabilized Power Supply Function

The stabilized power supply includes the following features:

- Wide range of operating input voltage from 6 V to 40 V to provide stabilized voltages
- Availability of any output current, by simply replacing the external transistor
- Fine adjustment of output voltage

Figure 1 shows the fine adjustment circuit of the output circuit. Select the resistor R1 as shown in equation 1.

Add a resistor between GND and Voadj to increase the output voltage.

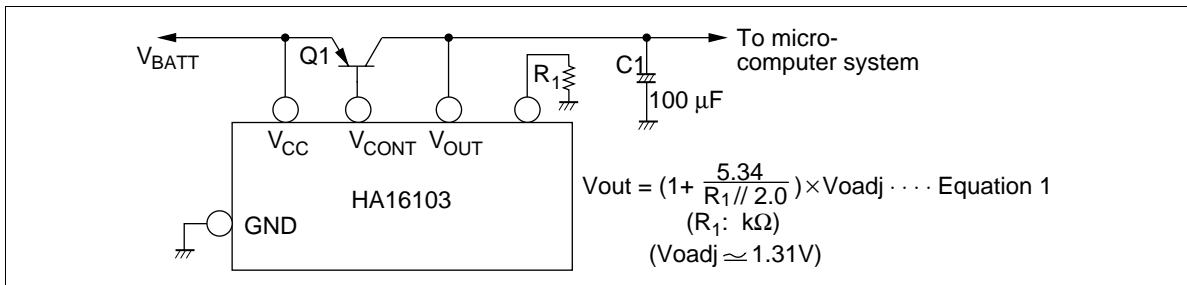


Figure 1 Fine Adjustment Circuit of Output Voltage

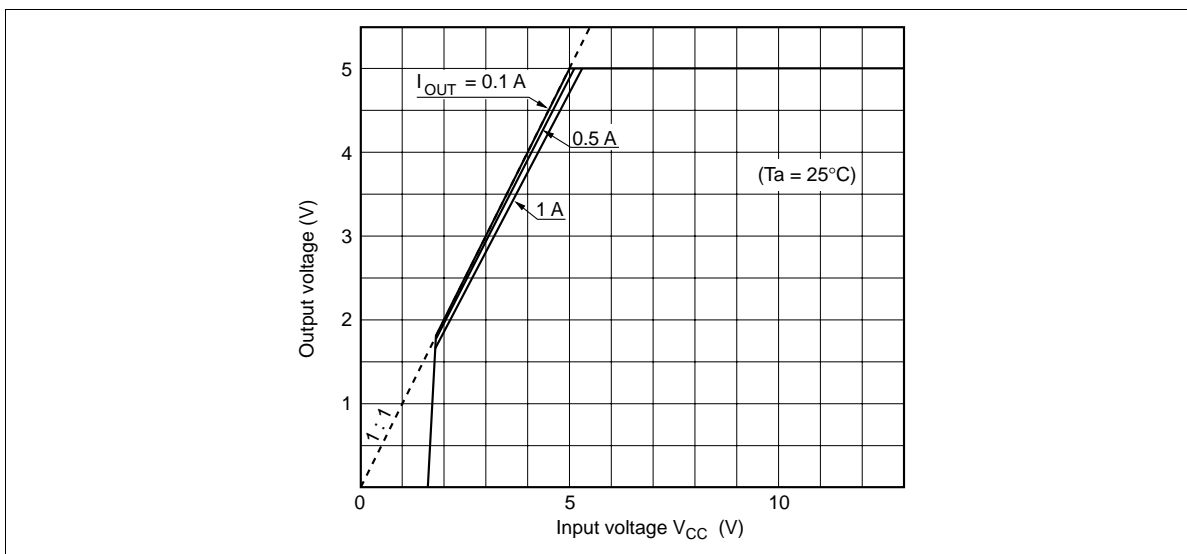


Figure 2 Output Voltage Characteristic

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Power-On Reset Function

The system contains the power-on reset function required when a microcomputer is turned on.

The reset period may be set with external components R_R and C_R . Equation 2 specifies how to determine the reset period (t_{on}) and figure 3 shows the characteristic of the circuit.

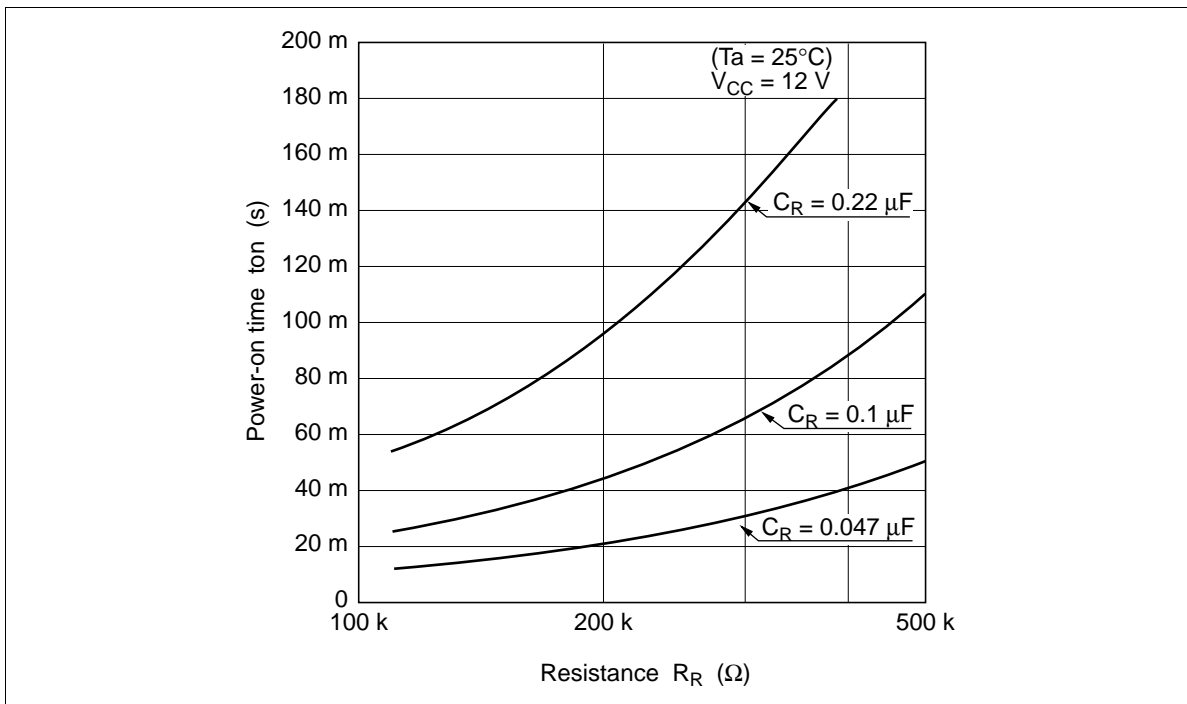
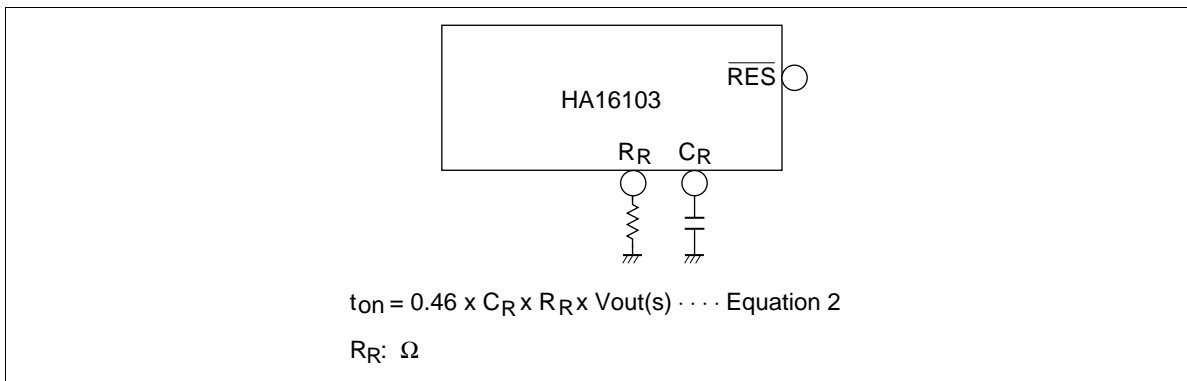


Figure 3 Characteristic of Power-On Reset Circuit

Watchdog Timer Function

The system contains a bandpass filter for pulse width detection, which outputs a reset pulse when input pulses are not at the preselected frequency (at either a higher or lower frequency).

The RC characteristic of the bandpass filter may be set with external components Rf and Cf. Equation 3 specifies how to determine the minimum pulse width (tmin) for runaway detection of the bandpass filter, and figure 4 shows the characteristic of the filter.

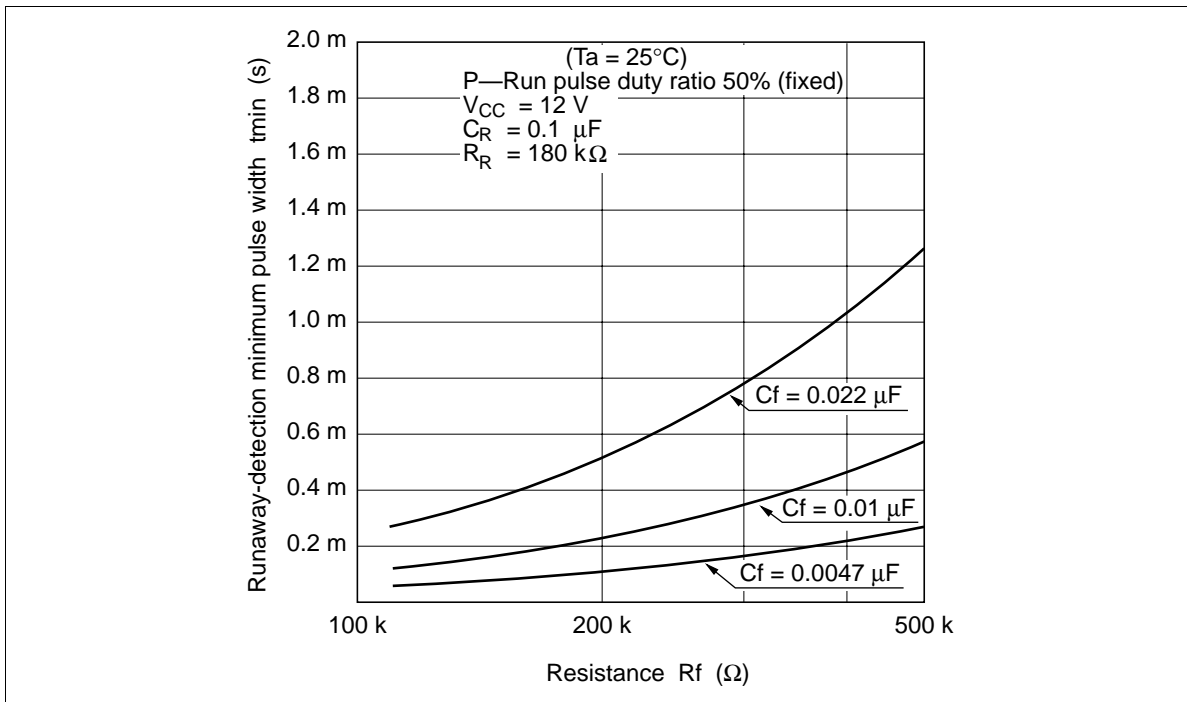
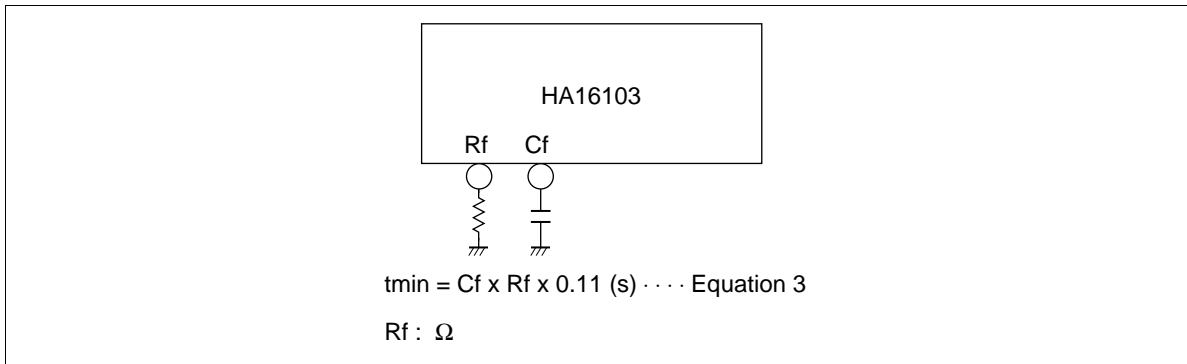


Figure 4 Characteristic of Power-On Reset Circuit

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Low Voltage Monitoring Function

The system contains a circuit to send a control signal to the microcomputer when the output voltage drops. The circuit includes the following features.

- Two-point monitoring of output voltage (V_{NMI} and V_{STBY})
- Availability of fine adjustment of V_{th1} (V_{NMI}) and V_{th2} (V_{STBY})
- Output of control signal in standby mode of microcomputer

Figure 5 shows the timing chart of control signals when the output voltage drops.

If the output voltage drops below V_{th1} (4.60 V), the \overline{NMI} signal rises to request the microcomputer to issue the \overline{NMI} interrupt signal. The \overline{RES} signal falls t_{RES} seconds after the \overline{NMI} signal rises. If the output voltage drops further to below V_{th2} (3.2 V), the \overline{STBY} signal rises to enable the micro-computer to enter standby mode.

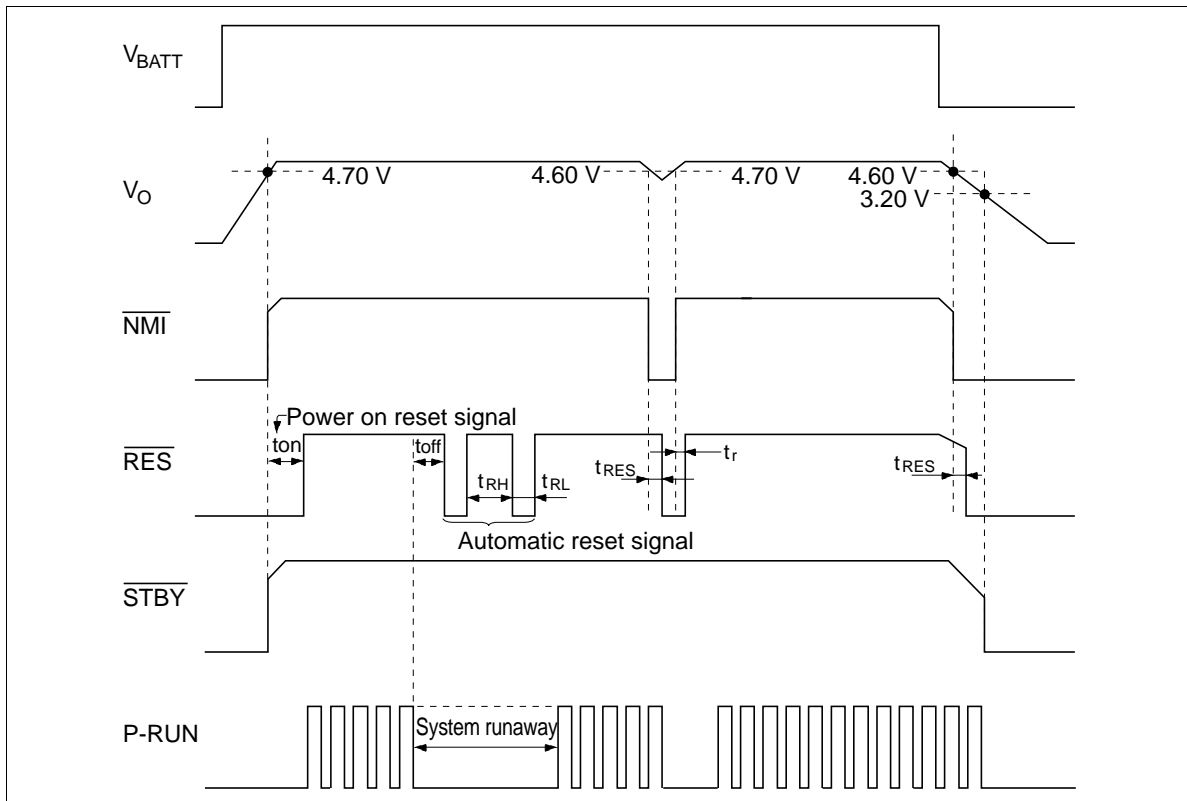


Figure 5 Timing Chart for Low Voltage Monitoring

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Units
		HA16103FPJ	HA16103FPK	
V _{CC} supply voltage	V _{CC}	40	40	V
Control pin voltage	V _{CONT}	40	40	V
Control pin current	I _{CONT}	20	20	mA
V _{OUT} pin voltage	V _{OUT}	12	12	V
Power dissipation	P _T	400* ¹	400* ²	mW
Operating ambient temperature range	T _{opr}	-40 to +85	-40 to +125	°C
Storage temperature range	T _{stg}	-50 to +125	-50 to +150	°C

Notes: 1. Value under Ta ≤ 77°C. If Ta is greater, 8.3 mW/°C derating occurs.

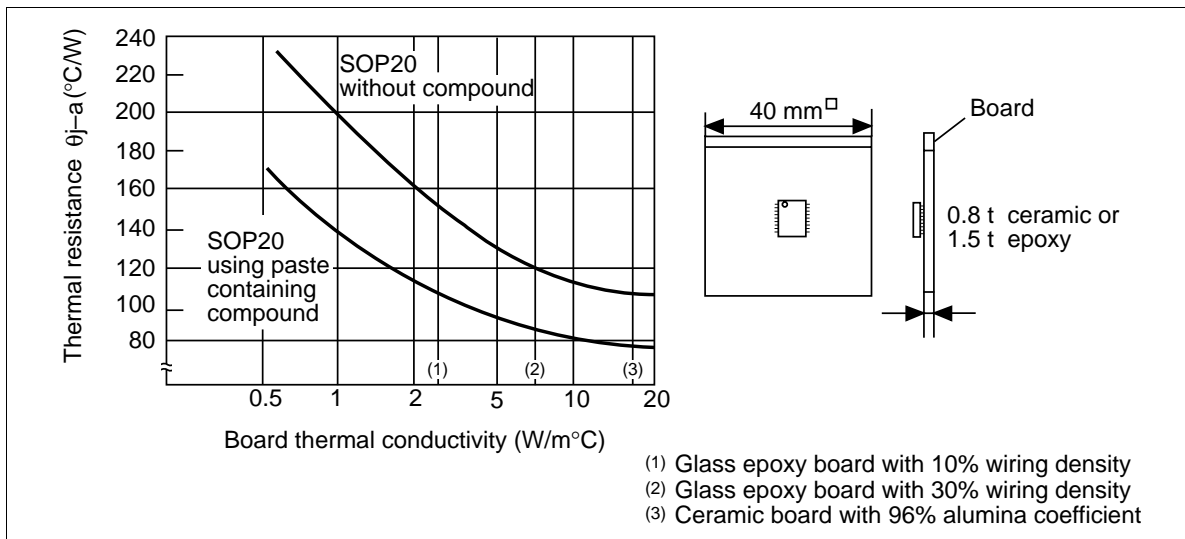
2. Allowable temperature of IC junction part, T_j (max), is as shown below.

$$T_j (\text{max}) = \theta_{j-a} \cdot P_c (\text{max}) + T_a$$

(θ_{j-a} is thermal resistance value during mounting, and P_c (max) is the maximum value of IC power dissipation.)

Therefore, to keep T_j (max) ≤ 125°C, wiring density and board material must be selected according to the board thermal conductivity ratio shown below.

Be careful that the value of P_c (max) does not exceed that P_T.



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Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$)

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Item		Symbol	Min	Typ	Max	Unit	Test Condition
	Supply current	I_{CCL}	—	8	12	mA	$V_{CC} = 12\text{ V}$
Regulator	Output voltage	V_{O1}	4.80	5.00	5.20	V	$V_{CC} = 6\text{ to }17.5\text{ V}$ $I_{OUT} = 0.5\text{ A}$, $R_1 = 30\text{ k}\Omega$
		V_{O2}	4.70	5.00	5.30	V	$V_{CC} = 6\text{ to }17.5\text{ V}$ $I_{OUT} = 1\text{ A}$, $R_1 = 30\text{ k}\Omega$
	Line regulation	V_{oline}	-50	—	50	mV	$V_{CC} = 6\text{ to }17.5\text{ V}$ $I_{OUT} = 1\text{ A}$, $R_1 = 30\text{ k}\Omega$
	Load regulation	V_{oload}	-100	—	100	mV	$I_{OUT} = 10\text{ mA to }0.5\text{ A}$, $R_1 = 30\text{ k}\Omega$
	Ripple rejection	R_{REJ}	45	75	—	dB	$V_i = 0.5\text{ V}_{rms}$, $f_i = 1\text{ kHz}$, $R_1 = 30\text{ k}\Omega$
	Output voltage Temperature coefficient	$\delta V_O / \delta T$	—	0.6	—	mV/°C	$V_{CC} = 12\text{ V}$, $R_1 = 30\text{ k}\Omega$
Clock input	"L"-input voltage	V_{IL}	—	—	0.8	V	
	"H"-input voltage	V_{IH}	2.0	—	—	V	
	"L"-input current	I_{IL}	-120	-60	—	μA	$V_{IL} = 0\text{ V}$
	"H"-input current	I_{IH}	—	0.3	0.5	mA	$V_{IH} = 5\text{ V}$

Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
NMI output	NMI pin "L"-level voltage	V_{OL1}	—	—	0.4	V	$I_{OL1} = 2\text{ mA}$
	NMI pin "H"-level voltage	V_{OH1}	—	V_{O1} (V_{O2})	—	V	
	NMI function start V_{OUT} voltage	V_{NMI}	—	0.7	1.4	V	
STBY output	STBY pin "L"-level voltage	V_{OL2}	—	—	0.4	V	$I_{OL2} = 2\text{ mA}$
	STBY pin "H"-level voltage	V_{OH2}	—	V_{O1} (V_{O2})	—	V	
	STBY function start V_{OUT} voltage	V_{STBY}	—	0.7	1.4	V	
RES output	RES pin "L"-level voltage	V_{OL3}	—	—	0.4	V	$I_{OL3} = 2\text{ mA}$
	RES pin "H"-level voltage	V_{OH3}	—	V_{O1} (V_{O2})	—	V	
	RES function start V_{OUT} voltage	V_{RES}	—	0.7	1.4	V	
	Power on time	t_{ON}	25	40	60	ms	$R_f = 180\text{ k}\Omega$, $R_R = 180\text{ k}\Omega$
	Clock off reset time	t_{OFF}	80	130	190	ms	$C_f = 0.01\text{ }\mu\text{F}$, $C_R = 0.1\text{ }\mu\text{F}$
	Reset pulse "L"-level time	t_{RL}	15	20	30	ms	$R_f = 180\text{ k}\Omega$, $R_R = 180\text{ k}\Omega$ $C_f = 0.01\text{ }\mu\text{F}$, $C_R = 0.1\text{ }\mu\text{F}$
	Reset pulse "H"-level time	t_{RH}	37	60	90	ms	$R_f = 180\text{ k}\Omega$, $R_R = 180\text{ k}\Omega$ $C_f = 0.01\text{ }\mu\text{F}$, $C_R = 0.1\text{ }\mu\text{F}$
Low Voltage protecton	Detection voltage(1)	V_{H1}	4.40	4.60	4.80	V	
	Detection voltage(1) Hysteresis width	V_{HYS1}	50	100	150	mV	
	Detection voltage(2)	V_{H2}	2.9	3.2	3.5	V	
	Detection voltage(2) Hysteresis width	V_{HYS2}	1.35	1.5	1.65	V	
	Reset pulse	inhibit t_{RES}	—	200	—	μs	$C_{RES} = 2200\text{ pF}$
	Delay time	restart t_r	—	200	—	μs	$C_{RES} = 2200\text{ pF}$

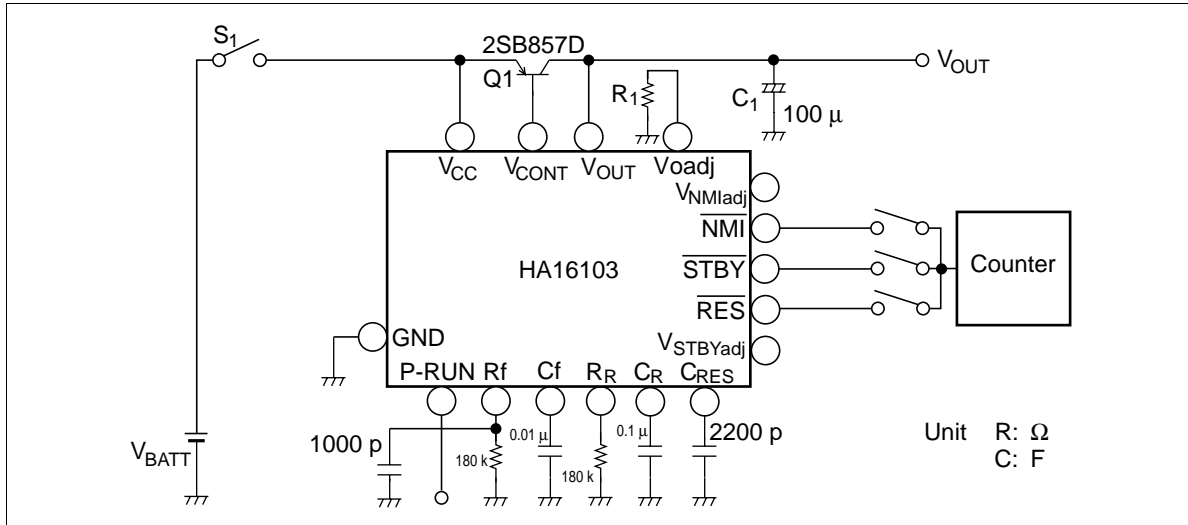
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Electrical Characteristics ($T_a = -40$ to 125°C , $V_{CC} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $R1 = 30\text{ k}$)
(cont)

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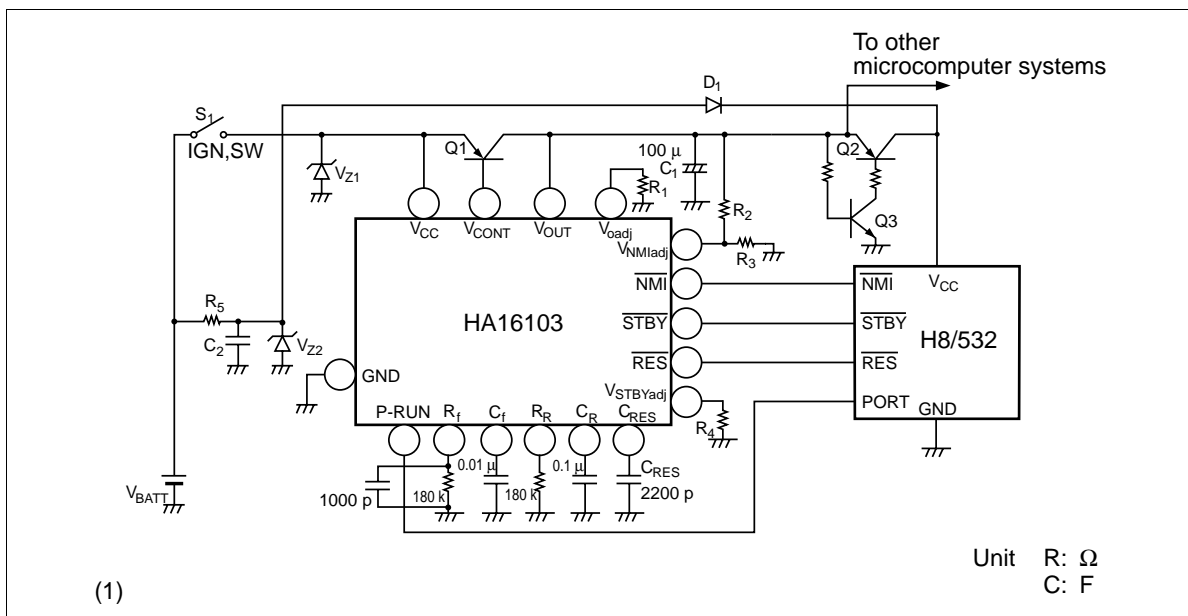
Item		Symbol	Min	Typ	Max	Unit	Test Condition
	Supply current	I_{CC1}	—	7	13	mA	
Regulator	Output voltage	V_{out1}	4.80	5.00	5.20	V	$V_{CC} = 6$ to 17.5 V $I_{OUT} = 0.5\text{ A}$
	Line regulation	V_{oline}	-50	—	50	mV	$V_{CC} = 6$ to 17.5 V $I_{OUT} = 0.5\text{ A}$
	Load regulation	V_{oload}	-100	—	100	mV	$I_{OUT} = 10\text{ mA}$ to 0.5 A
Clock input	"L"-input voltage	V_{IL}	—	—	0.4	V	
	"H"-input voltage	V_{IH}	2.4	—	—	V	
	"L"-input current	I_{IL}	-120	-60	—	μA	$V_{IL} = 0\text{ V}$
	"H"-input current	I_{IH}	—	0.3	0.6	mA	$V_{IH} = 5\text{ V}$
NMI output	NMI pin "L"-level voltage	V_{OLN}	—	—	0.5	V	$I_{OL1} = 2\text{ mA}$
	NMI pin "H"-level voltage	V_{OHN}	—	V_{OUT1}	—	V	
STBY output	STBY pin "L"-level voltage	V_{OLS}	—	—	0.5	V	$I_{OL2} = 2\text{ mA}$
	STBY pin "H"-level voltage	V_{OHS}	—	V_{OUT1}	—	V	
RES output	RES pin "L"-level voltage	V_{OLR}	—	—	0.5	V	$I_{OL3} = 2\text{ mA}$
	RES pin "H"-level voltage	V_{OHR}	—	V_{OUT1}	—	V	
	Power on time	t_{ON}	25	40	60	ms	$R_f = 180\text{ k}\Omega$, $R_R = 180\text{ k}\Omega$
	Clock off reset time	t_{OFF}	70	130	200	ms	$C_f = 0.01\text{ }\mu\text{F}$, $C_R = 0.1\text{ }\mu\text{F}$
	Reset pulse "L"-level time	t_{RL}	15	20	30	ms	$R_f = 180\text{ k}\Omega$, $R_R = 180\text{ k}\Omega$ $C_f = 0.01\text{ }\mu\text{F}$, $C_R = 0.1\text{ }\mu\text{F}$
	Reset pulse "H"-level time	t_{RH}	30	60	100	ms	$R_f = 180\text{ k}\Omega$, $R_R = 180\text{ k}\Omega$ $C_f = 0.01\text{ }\mu\text{F}$, $C_R = 0.1\text{ }\mu\text{F}$
Low Voltage protecton	Detection voltage(1)	V_{NMI}	4.35	4.60	4.85	V	
	Detection voltage(2)	V_{STBY}	2.80	3.20	3.60	V	

Test Circuit



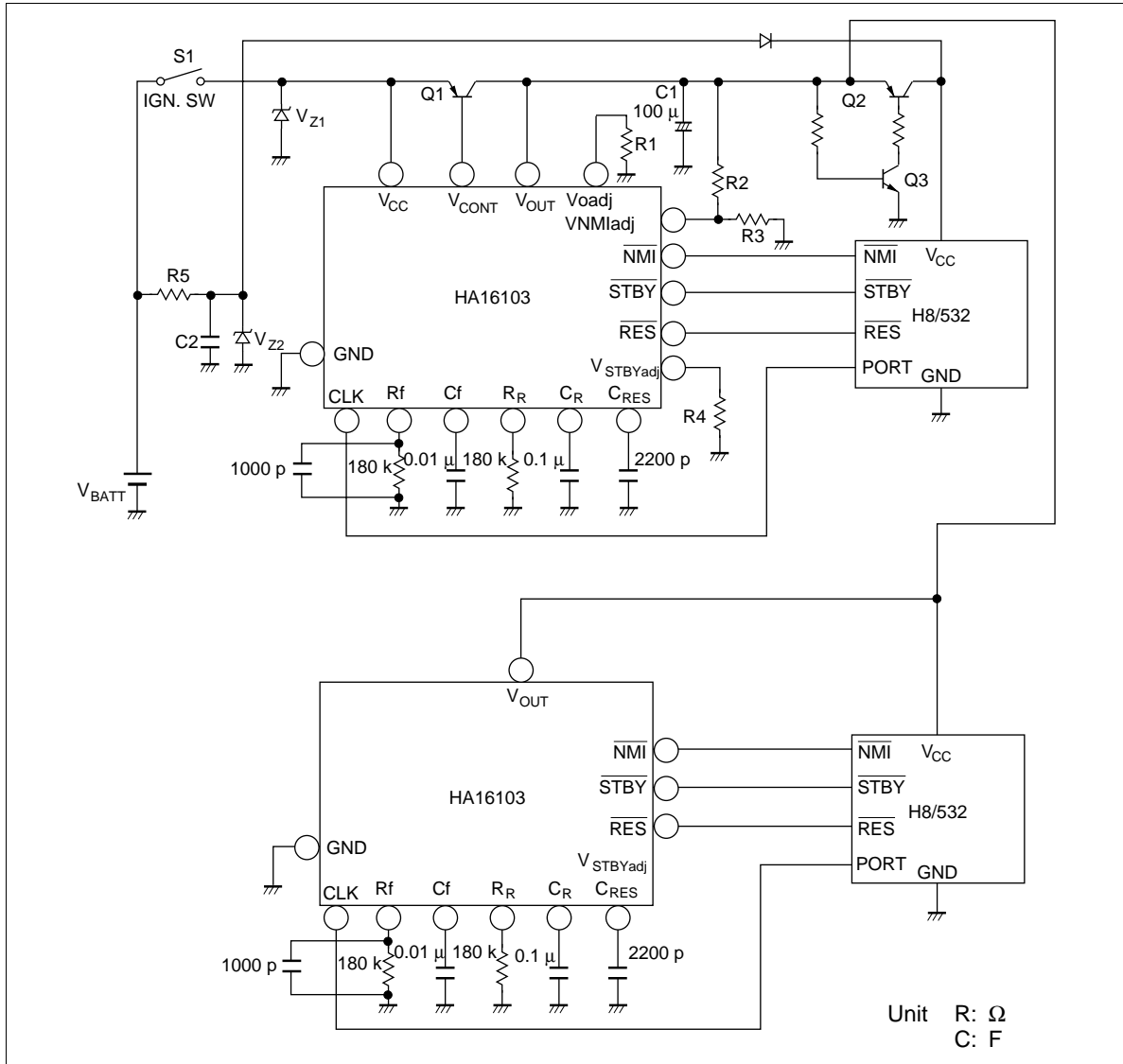
Sample Connection Circuit

Sample Connection Circuit between HA16103 and H8/532



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Sample Connection Circuit between HA16103 and H8/532 (2)



Precautions

If the IC's ground potential varies suddenly by several volts due to wiring impedance (see figure 6), a false $\overline{\text{RES}}$ pulse may be output. The reason for this is that potentials in the $\overline{\text{RES}}$ pulse generating circuit change together with the $V_{\text{OUT}}\text{-GND}$ potential. The reference potential of the comparator in figure 7 and the potential of the external capacitor have different impedances as seen from the comparator, causing a momentary inversion. The solution is to stabilize the ground potential. Two ways of stabilizing the IC's ground line are:

- Separate the IC's ground line from highcurrent ground lines.
- Increase the capacitance (C_0) used to smooth the V_{OUT} output.

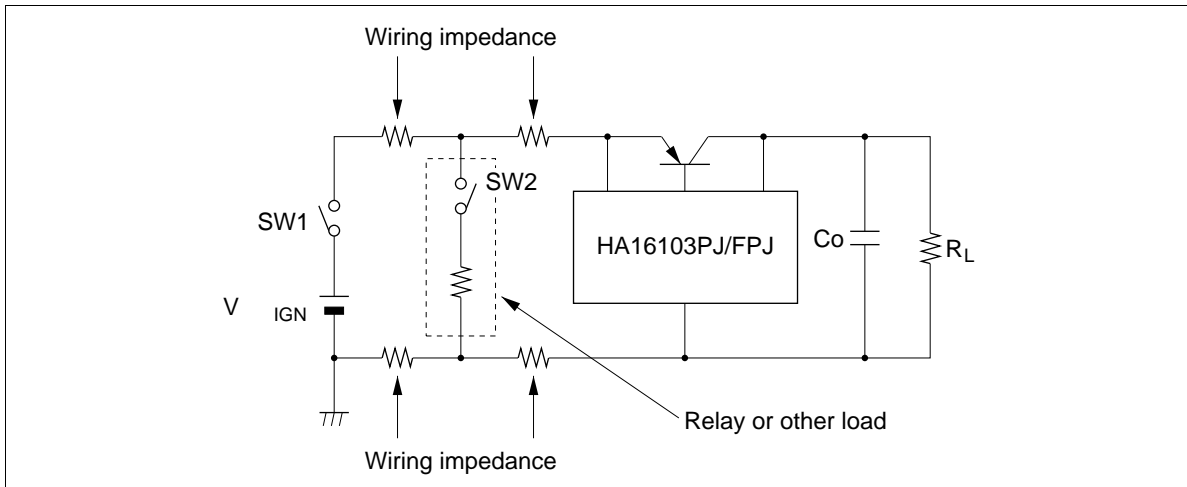


Figure 6 Typical Circuit

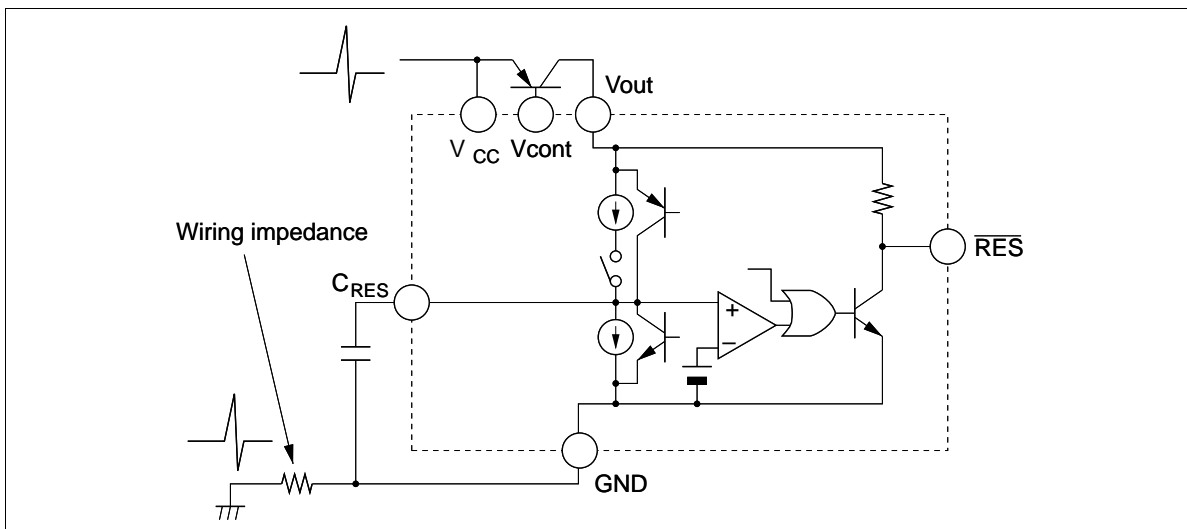
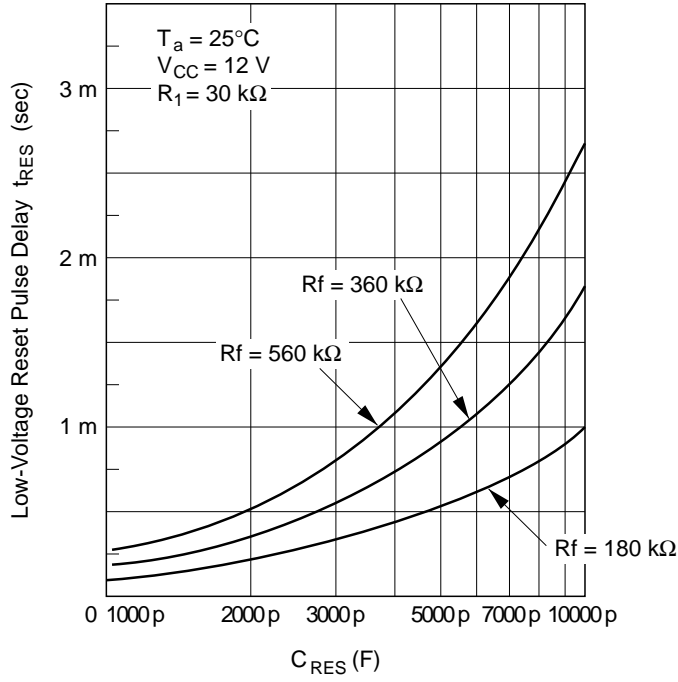


Figure 7 $\overline{\text{RES}}$ Comparator

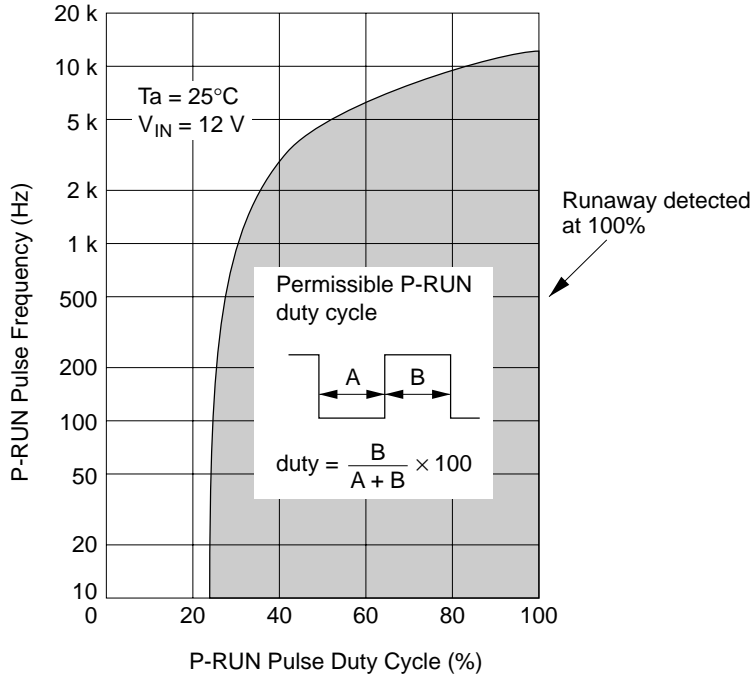
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• Low-voltage inhibit section

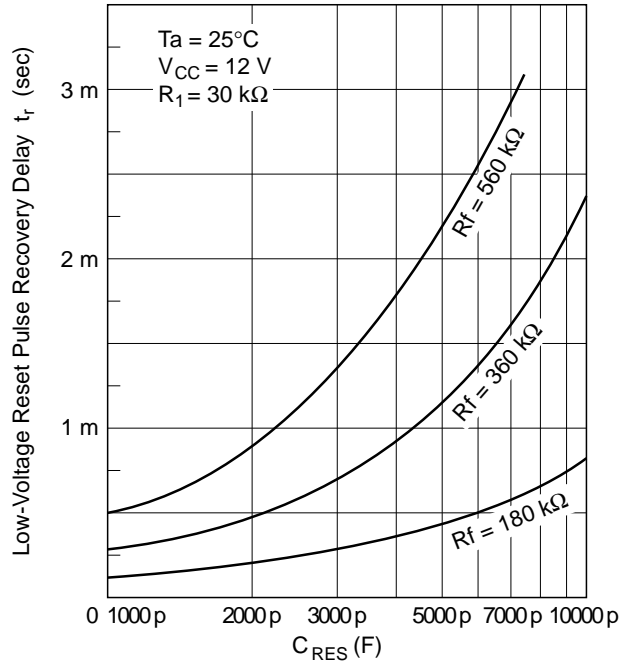
Low-Voltage Reset Pulse Delay vs. C_{RES}



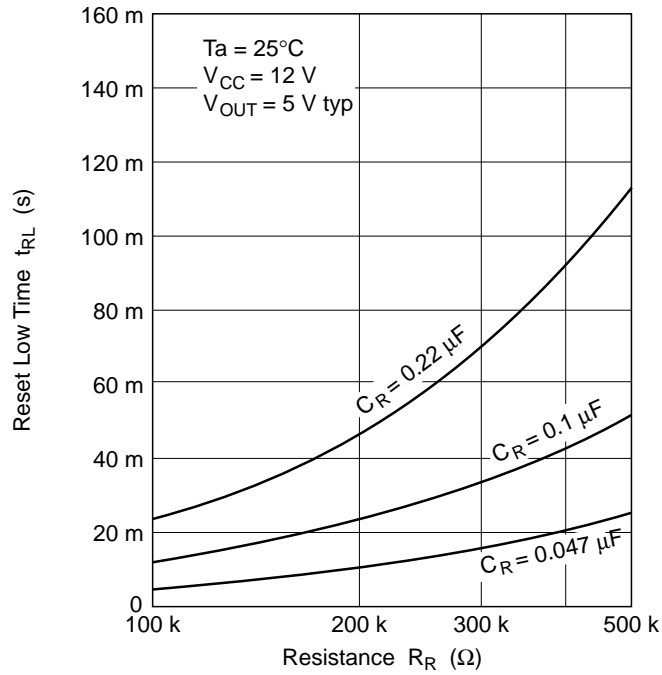
Permissible P-RUN Pulse Duty Cycle vs. P-RUN Pulse Frequency



- Low-voltage inhibit section
Low-Voltage Reset Pulse Recovery Delay vs. C_{RES}

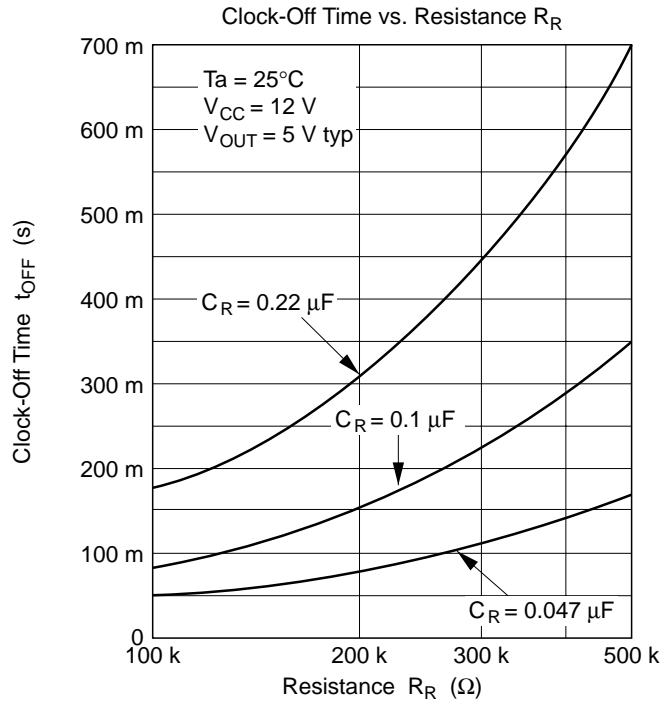


- Power-on and auto-reset section
Reset Low Time vs. Resistance R_R

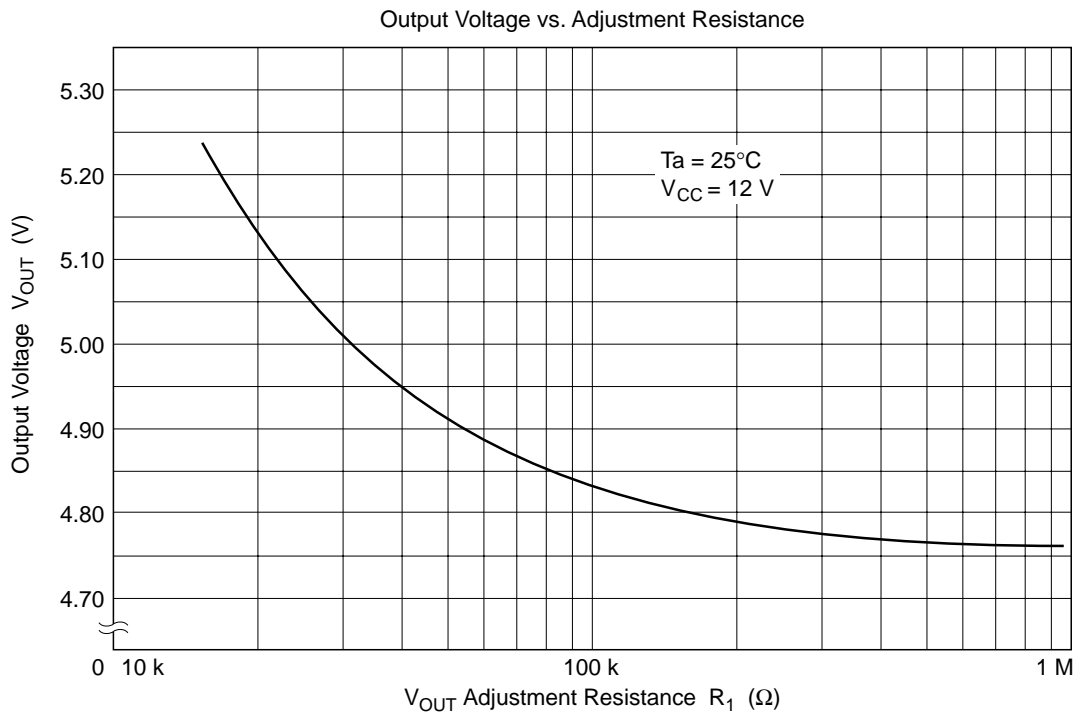


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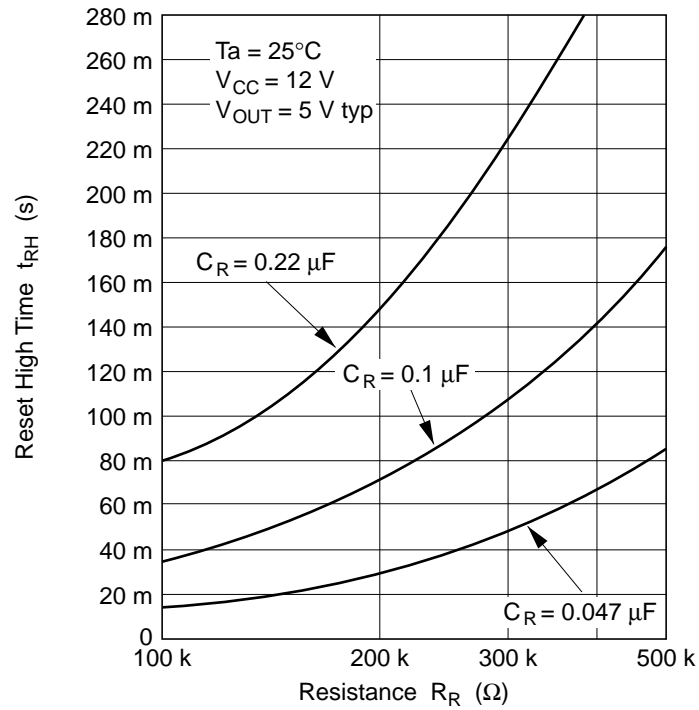
- Power-on and auto-reset section



- Vref section

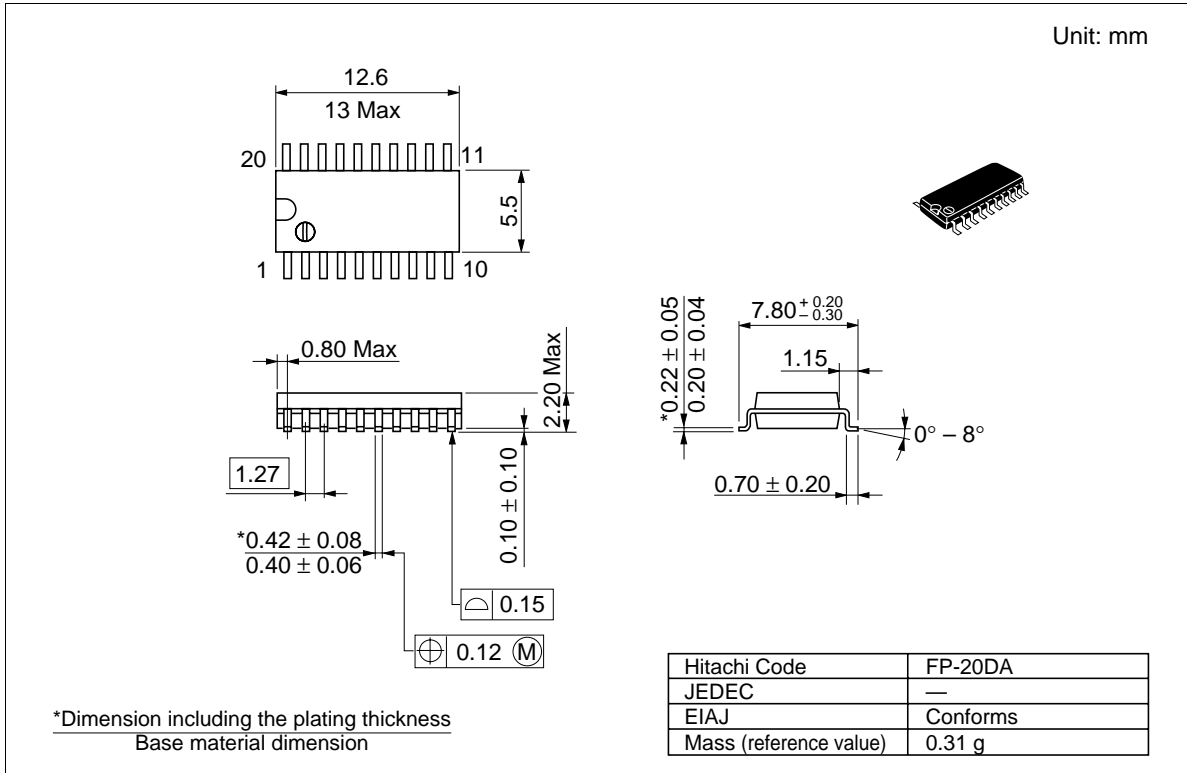


• Power-on and auto-reset section
Reset High Time vs. Resistance R_R



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Package Dimensions



Cautions

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