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Renesas Technology Corp. Customer Support Dept. April 1, 2003



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Silicon N Channel Power MOS FET Power Switching



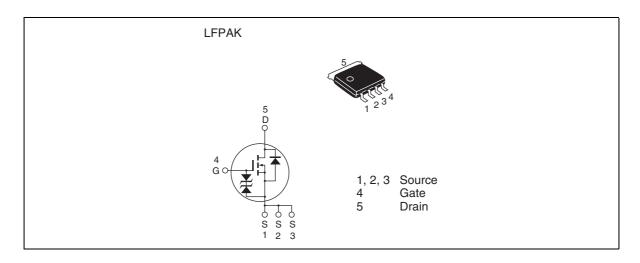
ADE-208-1581B(Z)

Preliminary 3rd. Edition Aug. 2002

Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance $R_{_{DS(on)}} = 12.5 \text{ m}\Omega \text{ typ. (at } V_{_{GS}} = 10 \text{ V})$

Outline



Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	100	V
Gate to source voltage	V _{gss}	±20	V
Drain current	I _D	25	A
Drain peak current	Note1 D(pulse)	100	A
Body-drain diode reverse drain current	I _{DR}	25	A
Avalanche current	I Note 3	25	A
Avalanche energy	E _{AR} Note 3	62.5	mJ
Channel dissipation	Pch ^{Note2}	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to + 150	°C

Notes: 1. $PW \le 10 \ \mu s$, duty cycle $\le 1\%$

2. Tc=25°C

3. Value at Tch = 25°C, Rg \geq 50 Ω

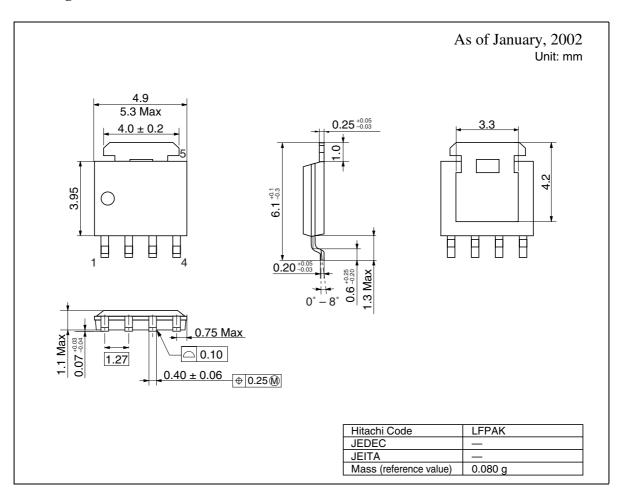
Electrical Characteristics

 $(Ta = 25^{\circ}C)$

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{\rm (BR)DSS}$	100	—	—	V	$I_{\rm D} = 10 \text{ mA}, V_{\rm GS} = 0$
Gate to source breakdown voltage	$V_{\scriptscriptstyle (BR)GSS}$	±20	_	_	V	$I_{_{\rm G}} = \pm 100 \ \mu A, \ V_{_{\rm DS}} = 0$
Gate to source leak current	I _{GSS}	_		±10	μA	$V_{_{\rm GS}} = \pm 16 \text{ V}, \text{ V}_{_{\rm DS}} = 0$
Zero gate voltage drain current	I _{DSS}	_		1	μA	$V_{_{\rm DS}} = 100 \text{ V}, \text{ V}_{_{\rm GS}} = 0$
Gate to source cutoff voltage	$V_{_{GS(off)}}$	2.0		3.5	V	$V_{_{DS}} = 10 \text{ V}, \text{ I}_{_{D}} = 1 \text{ mA}$
Static drain to source on state	${\rm R}_{\rm DS(on)}$	_	12.5	16.0	mΩ	$I_{D} = 12.5 \text{ A}, V_{GS} = 10 \text{ V}^{Note4}$
resistance	$R_{\rm DS(on)}$	_	13.5	18.0	mΩ	$I_{D} = 12.5 \text{ A}, V_{GS} = 7 \text{ V}^{Note4}$
Forward transfer admittance	ly _{fs} l	27	45	—	S	$I_{D} = 12.5 \text{ A}, V_{DS} = 10 \text{ V}^{Note4}$
Input capacitance	Ciss	_	6500		pF	V _{DS} = 10 V
Output capacitance	Coss	_	480		pF	$V_{gs} = 0$
Reverse transfer capacitance	Crss	_	210		pF	f = 1 MHz
Total gate charge	Qg	—	105	—	nc	V _{DD} = 50 V
Gate to source charge	Qgs	_	20		nc	V _{GS} = 10 V
Gate to drain charge	Qgd	_	22		nc	I _D = 25 A
Turn-on delay time	t _{d(on)}	—	25	—	ns	$V_{\rm GS} = 10$ V, $I_{\rm D} = 12.5$ A
Rise time	t _r	_	24	_	ns	$V_{\text{DD}} \cong 30 \text{ V}$
Turn-off delay time	t _{d(off)}	_	100	_	ns	$R_{L} = 2.4 \Omega$
Fall time	t _r	_	12	_	ns	Rg = 4.7 Ω
Body-drain diode forward voltage	V_{df}	_	0.83	1.08	V	$IF = 25 A, V_{GS} = 0^{Note4}$
Body-drain diode reverse recovery time	t _{rr}	—	55		ns	IF = 25 A, V _{αs} = 0 diF/ dt = 100 A/ μs

Notes: 4. Pulse test

Package Dimensions



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