

To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HAT2142H

Silicon N Channel Power MOS FET
Power Switching

RENESAS

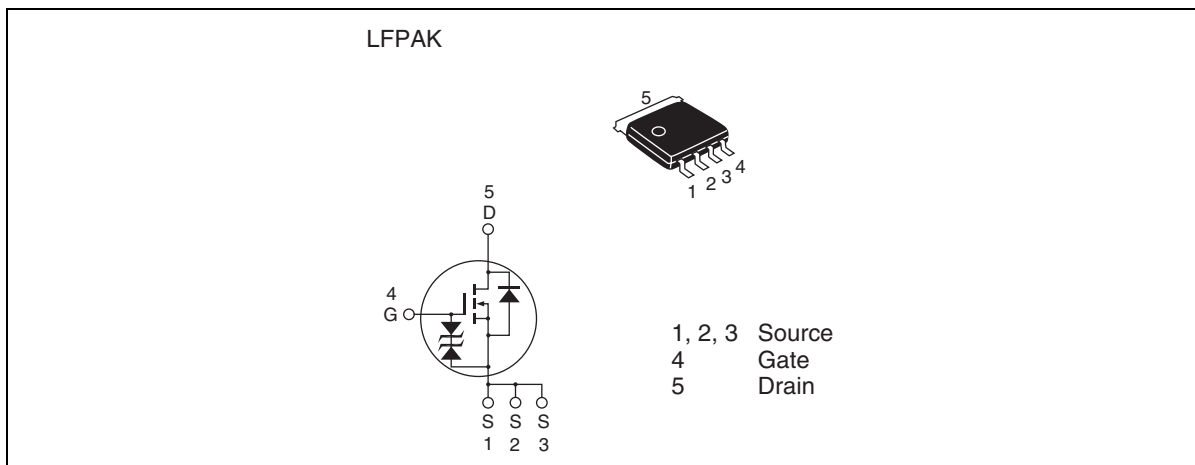
ADE-208-1583E (Z)

6th. Edition
Sep. 2002

Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 35 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline



HAT2142H

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	100	V
Gate to source voltage	V _{GSS}	± 20	V
Drain current	I _D	10	A
Drain peak current	I _{D(pulse)} ^{Note1}	40	A
Body-drain diode reverse drain current	I _{DR}	10	A
Avalanche current	I _{AP} ^{Note 3}	10	A
Avalanche energy	E _{AR} ^{Note 3}	10	mJ
Channel dissipation	P _{ch} ^{Note2}	15	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	– 55 to + 150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics

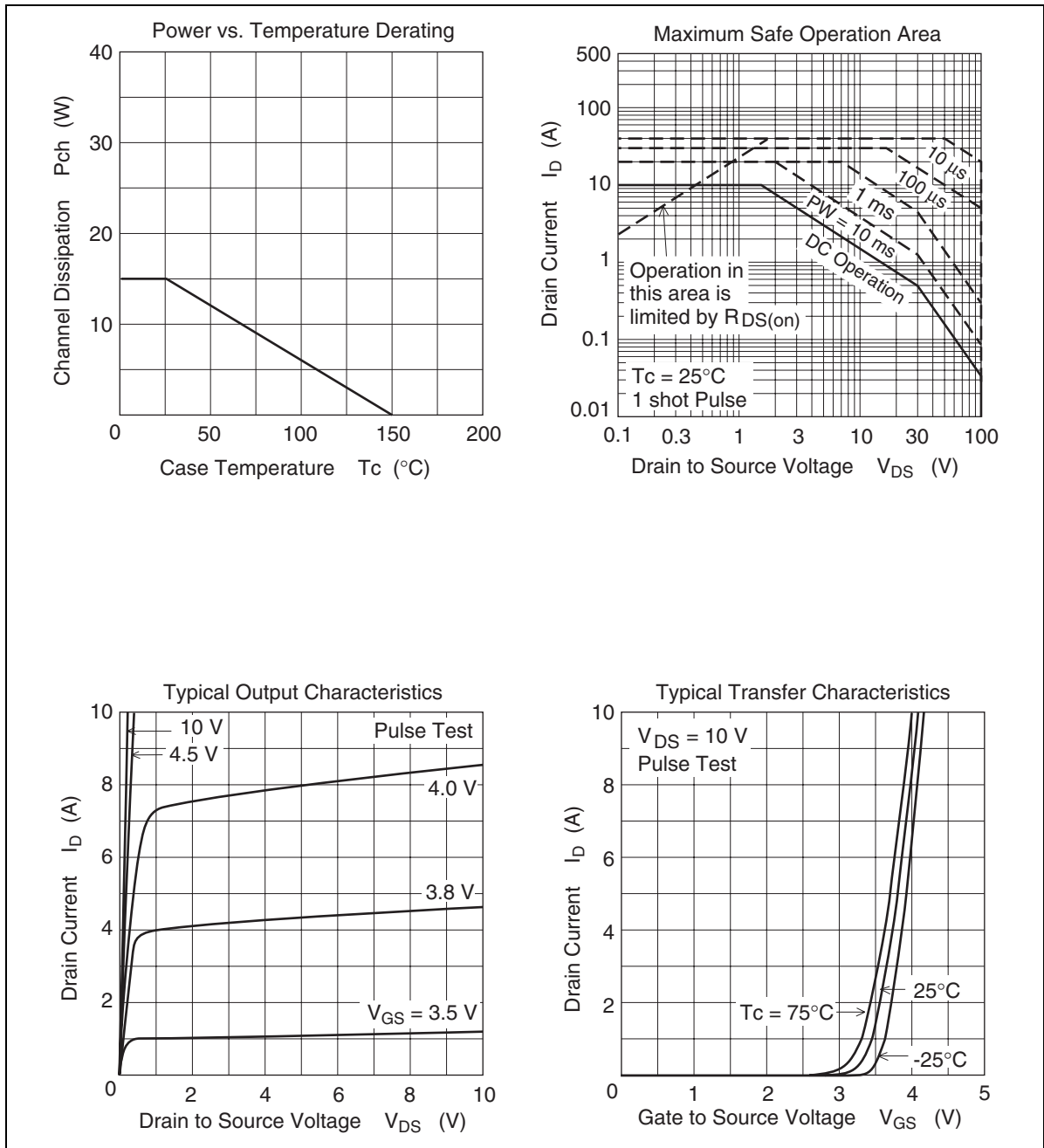
(Ta = 25°C)

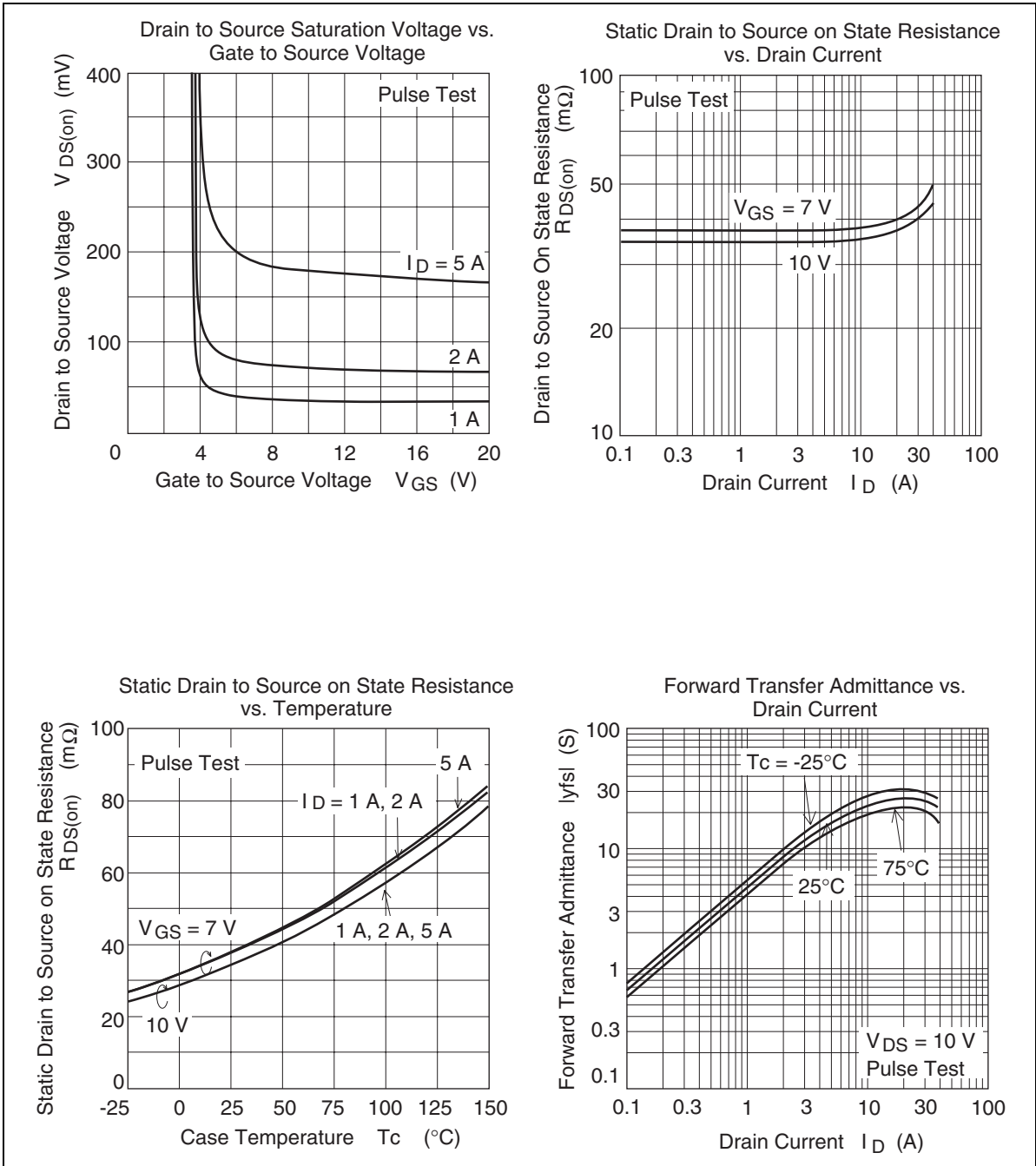
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	35	44	$\text{m}\Omega$	$I_D = 5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	38	51	$\text{m}\Omega$	$I_D = 5 \text{ A}$, $V_{GS} = 7 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	9	15	—	S	$I_D = 5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	Ciss	—	2000	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	175	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	90	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	32	—	nc	$V_{DD} = 50 \text{ V}$
Gate to source charge	Qgs	—	8.0	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	7.5	—	nc	$I_D = 10 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	18	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 5 \text{ A}$
Rise time	t_r	—	11	—	ns	$V_{DD} \cong 30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	60	—	ns	$R_L = 6 \Omega$
Fall time	t_f	—	9	—	ns	$R_g = 4.7 \Omega$
Body–drain diode forward voltage	V_{DF}	—	0.82	1.07	V	$I_F = 10 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 10 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

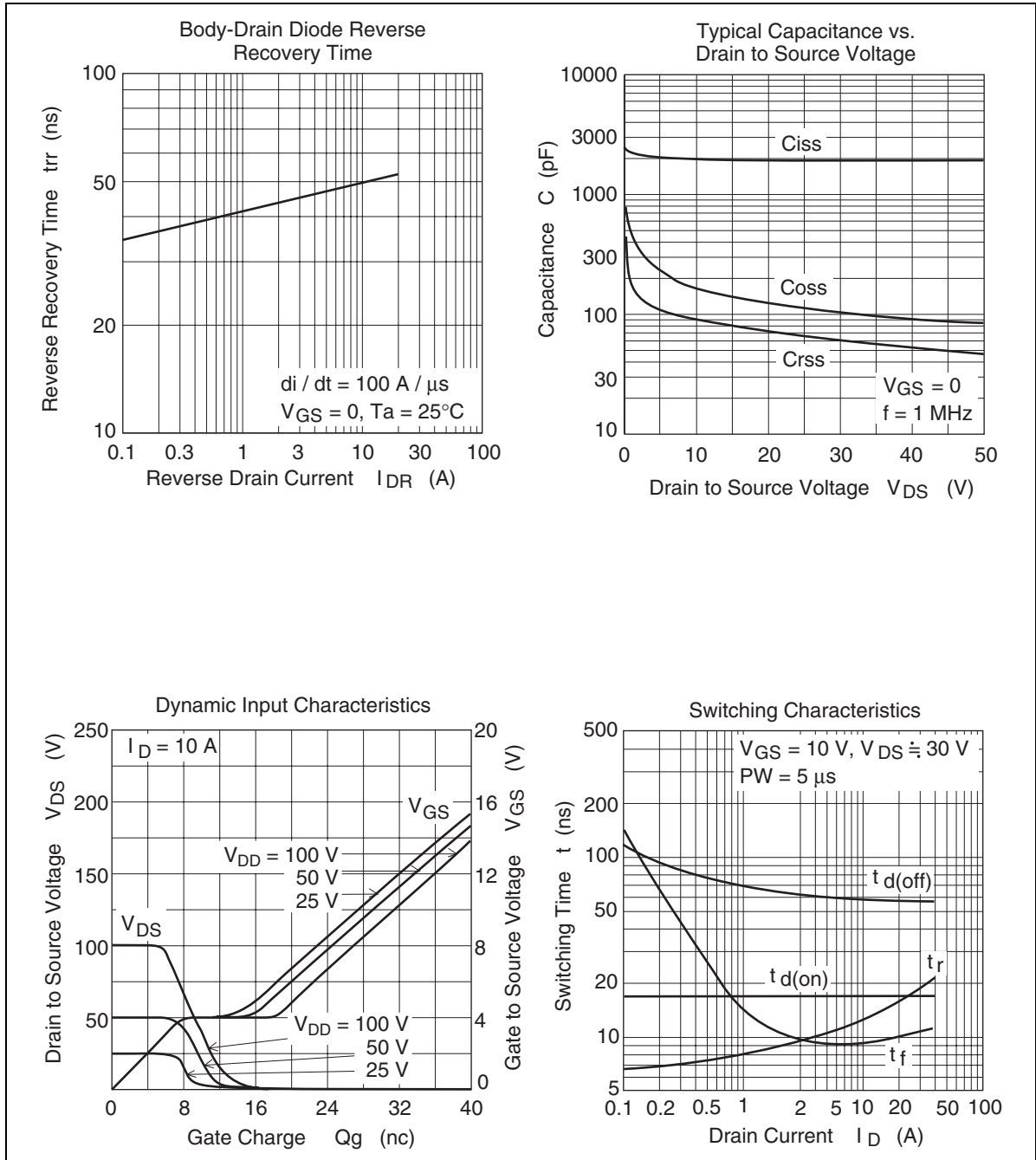
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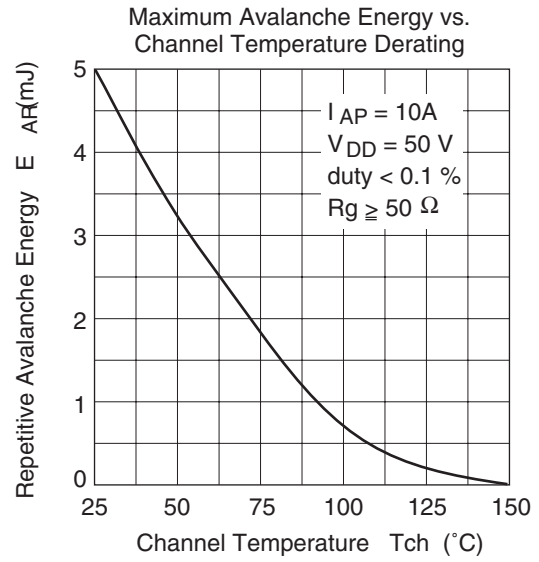
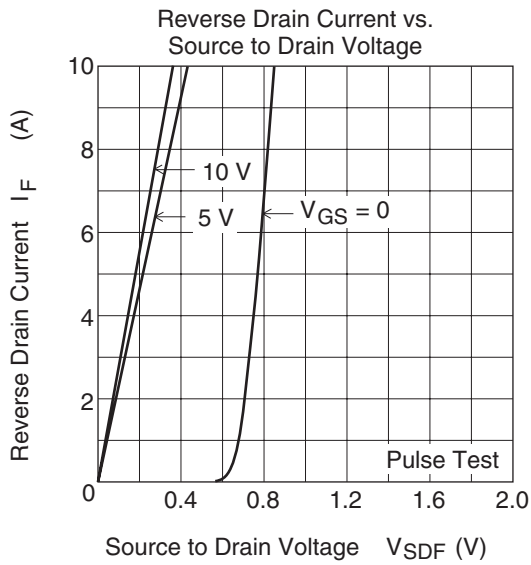
Main Characteristics



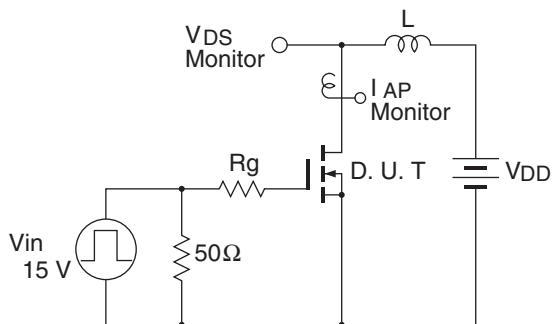


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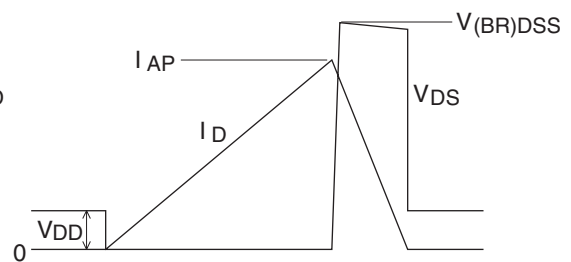


Avalanche Test Circuit

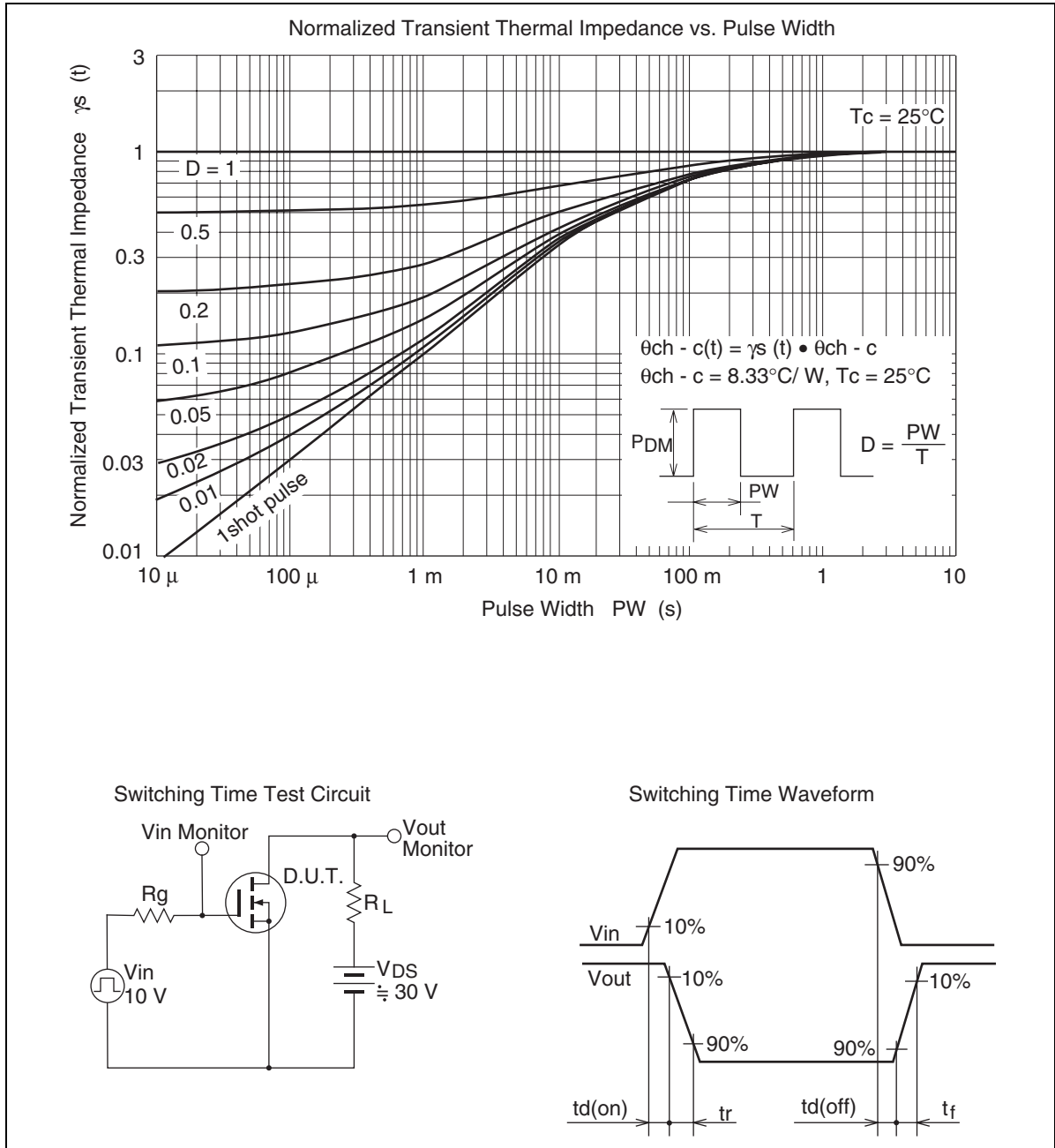


Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

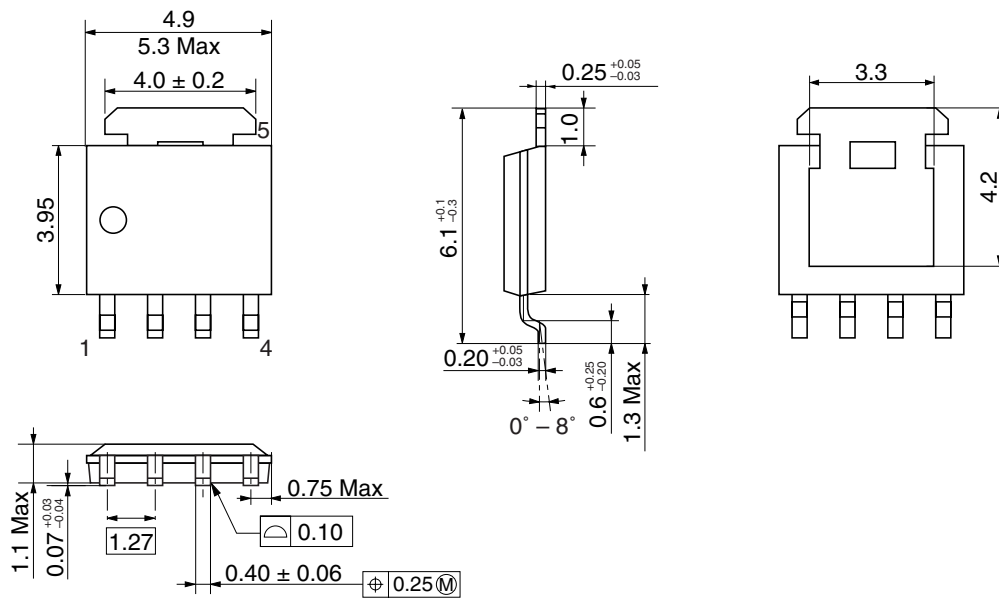


HAT2142H



Package Dimensions

As of January, 2002
Unit: mm



Hitachi Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

HAT2142H

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