HEWLETT PACKARD

High Bandwidth, Analog/Video Optocouplers

Technical Data

HCPL-4562
HCNW4562

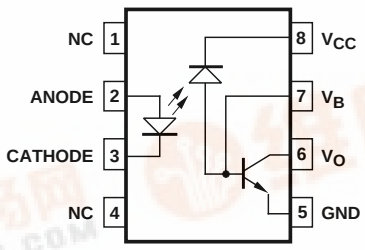
Features

- **Wide Bandwidth[1]:**
  17 MHz (HCPL-4562)
  9 MHz (HCNW4562)
- **High Voltage Gain[1]:**
  2.0 (HCPL-4562)
  3.0 (HCNW4562)
- **Low G_V Temperature Coefficient: -0.3%/°C**
- **Highly Linear at Low Drive Currents**
- **High-Speed AlGaAs Emitter**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute (5000 V rms for 1 minute for HCPL-4562#020 and HCNW4562) per UL 1577
  CSA Approved
  VDE 0884 Approved
  $-V_{IORM}$ = 1414 V peak for HCNW4562
  BSI Certified (HCNW4562)
- **Available in 8-Pin DIP and Widebody Packages**

Applications

- **Video Isolation for the Following Standards/ Formats: NTSC, PAL, SECAM, S-VHS, ANALOG RGB**
- **Low Drive Current Feedback Element in Switching Power Supplies, e.g., for ISDN Networks**
- **A/D Converter Signal Isolation**
- **Analog Signal Ground Isolation**
- **High Voltage Insulation**

Functional Diagram



Description

The HCPL-4562 and HCNW4562 optocouplers provide wide bandwidth isolation for analog signals. They are ideal for video isolation when combined with their application circuit (Figure 4). High linearity and low phase shift are achieved through an AlGaAs LED combined with a high speed detector. These single channel optocouplers are available in 8-Pin DIP and Widebody package configurations.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Selection Guide

Single Channel Packages	
8-Pin DIP (300 Mil)	**Widebody (400 Mil)**
HCPL-4562	HCNW4562

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

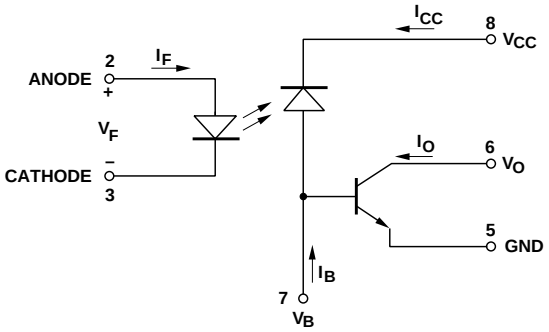
HCPL-4562#XXX

- 020 = UL 5000 V rms/1 Minute Option*
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets are available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

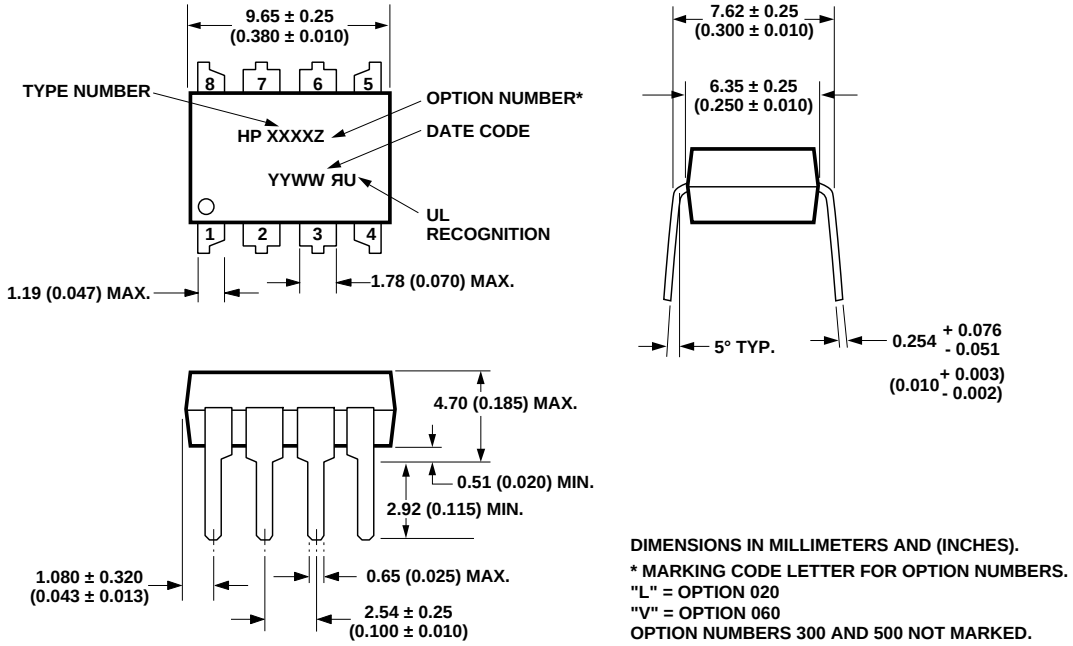
*For HCPL-4562 only.
†Gull wing surface mount option applies to through hole parts only.

Schematic



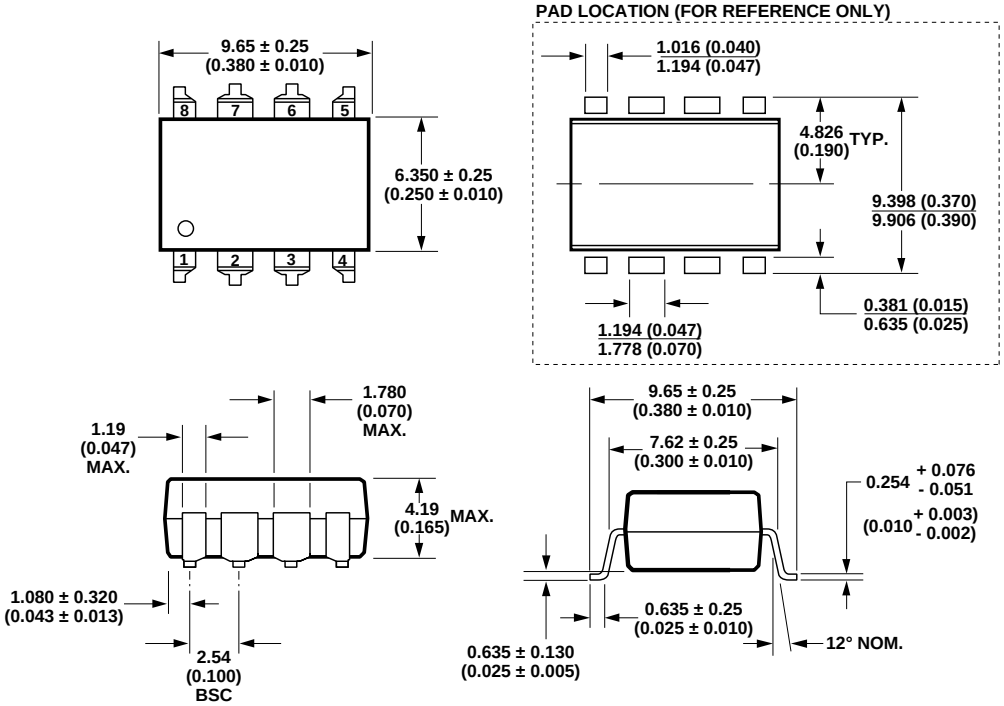
Package Outline Drawings

8-Pin DIP Package (HCPL-4562)



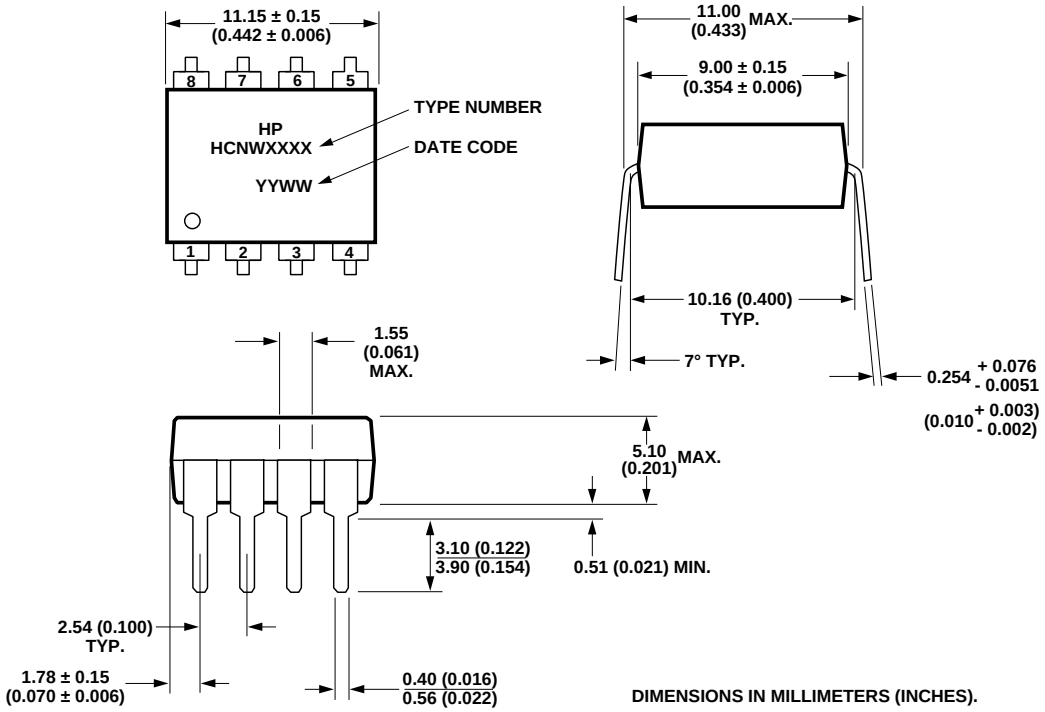
DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS.
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4562)

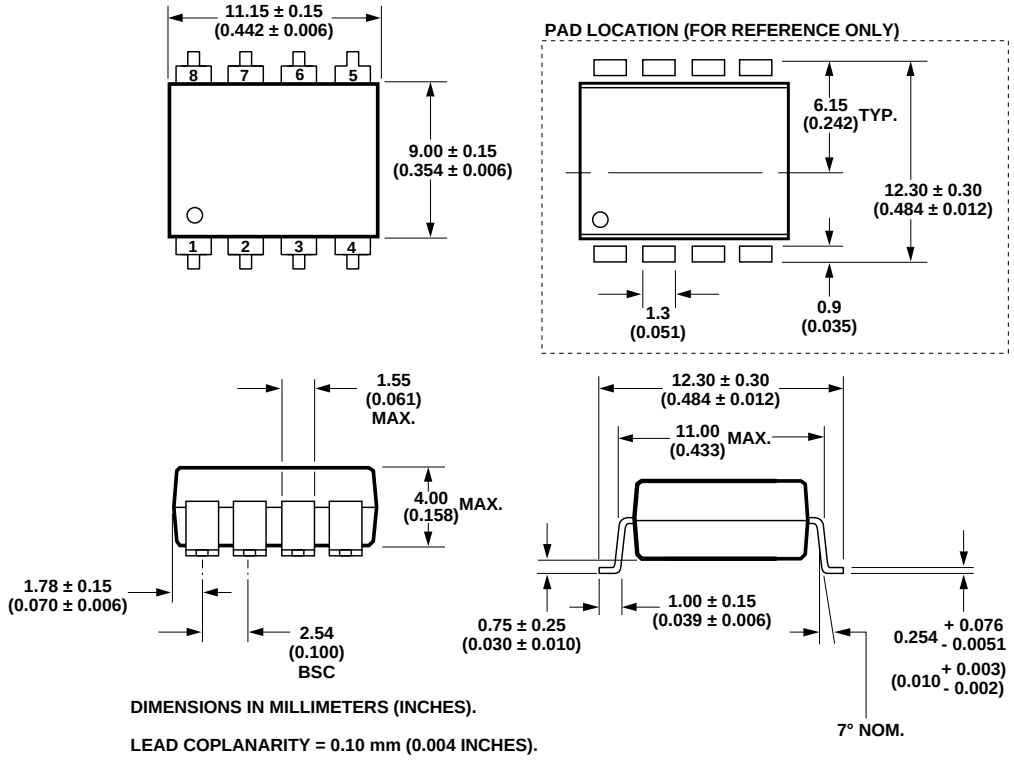


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

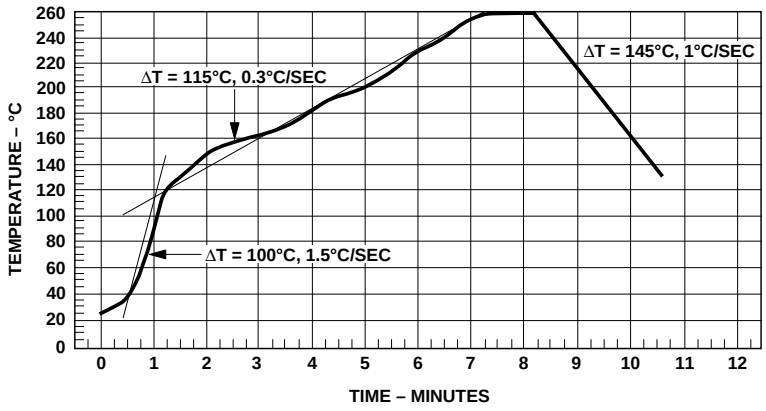
8-Pin Widebody DIP Package (HCNW4562)



8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW4562)



Solder Reflow Temperature Profile (Gull Wing Surface Mount Option Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92 (HCNW4562 only).

BSI

Certification according to BS415:1994 (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications (HCNW4562 only).

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photo-emitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCNW4562 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 17, Thermal Derating curve.) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 150 400 700	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	℃	
Operating Temperature	T_A		-40	85	℃	
Average Forward Input Current	$I_{F(avg)}$	HCPL-4562		12	mA	
		HCNW4562		25		
Peak Forward Input Current	$I_{F(PEAK)}$	HCPL-4562		18.6	mA	
		HCNW4562		40		
Effective Input Current	$I_{F(EFF)}$	HCPL-4562		12.9	mA rms	
Reverse LED Input Voltage (Pin 3-2)	V_R	HCPL-4562		1.8	V	
		HCNW4562		3		
Input Power Dissipation	P_{IN}	HCNW4562		40	mW	
Average Output Current (Pin 6)	$I_{O(AVG)}$			8	mA	
Peak Output Current (Pin 6)	$I_{O(PEAK)}$			16	mA	
Emitter-Base Reverse Voltage (Pin 5-7)	V_{EBR}			5	V	
Supply Voltage (Pin 8-5)	V_{CC}		-0.3	30	V	
Output Voltage (Pin 6-5)	V_O		-0.3	20	V	
Base Current (Pin 7)	I_B			5	mA	
Output Power Dissipation	P_O			100	mW	2
Lead Solder Temperature 1.6 mm Below Seating Plane, 10 Seconds up to Seating Plane, 10 Seconds	T_{LS}	HCPL-4562		260	℃	
		HCNW4562		260	℃	
Reflow Temperature Profile	T_{RP}	Option 300	See **Package Outline Drawings** Section			

Recommended Operating Conditions

Parameter	Symbol	Device	Min.	Max.	Units	Note
Operating Temperature	T_A	HCPL-4562	-10	70	℃	
Quiescent Input Current	I_{FQ}	HCPL-4562		6	mA	
		HCNW4562		10		
Peak Input Current	$I_{F(PEAK)}$	HCPL-4562		10	mA	
		HCNW4562		17		

Electrical Specifications (DC)

T_A = 25°C, I_F = 6 mA for HCPL-4562 and I_F = 10 mA for HCNW4562 (i.e., Recommended I_{FQ}) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Base Photo Current	I_{PB}		13	31	65	µA	I_F = 10 mA	$V_{PB} \geq 5$ V	2, 6	
		HCPL-4562		19.2			I_F = 6 mA			
I_{PB} Temperature Coefficient	$\Delta I_{PB}/\Delta T$			-0.3		%/°C	2 mA < I_F < 10 mA, $V_{PB} \geq 5$ V		2	
I_{PB} Nonlinearity		HCPL-4562		0.25		%	2 mA < I_F < 10 mA		2, 6	3
		HCNW4562		0.15			6 mA < I_F < 14 mA			
Input Forward Voltage	V_F	HCPL-4562	1.1	1.3	1.6	V	I_F = 5 mA		5	
		HCNW4562	1.2	1.6	1.8		I_F = 10 mA			
Input Reverse Breakdown Voltage	BV_R	HCPL-4562	1.8	5		V	I_R = 10 µA			
		HCNW4562	3				I_R = 100 µA			
Transistor Current Gain	h_{FE}		60	160			I_C = 1 mA, V_{CE} = 1.25 V			
Current Transfer Ratio	CTR	HCPL-4562		45		%	V_{CE} = 1.25 V, $V_{PB} \geq 5$ V		8, 9	4
		HCNW4562		52						
DC Output Voltage	V_{OUT}	HCPL-4562		4.25		V	G_V = 2, V_{CC} = 9 V		4, 15	
		HCNW4562		5.0						

Small Signal Characteristics (AC)

T_A = 25°C, I_F = 6 mA for HCPL-4562 and I_F = 10 mA for HCNW4562 (i.e., Recommended I_{FO}) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Voltage Gain	G_V (0.1 MHz)	HCPL-4562	0.8	2.0	4.2		V_{IN} = 1 V_{P-P}	1	6
		HCNW4562		3.0					
G_V Temperature Coefficient	$\Delta G_V/\Delta T$			-0.3		%/°C	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	1, 11	
Base Photo Current Variation	Δi_{PB} (6 MHz)	HCPL-4562		1.1	3.0	-dB	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	3, 10, 12	
		HCNW4562		0.36					
-3 dB Frequency (i_{PB})	i_{PB} (-3 dB)	HCPL-4562	6	15		MHz	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	3, 10, 12	7
		HCNW4562		13					
-3 dB Frequency (G_V)	G_V (-3 dB)	HCPL-4562	6	17		MHz	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	1, 11	7
		HCNW4562		9					
Gain Variation	ΔG_V (6 MHz)	HCPL-4562		1.1	3.0	-dB	T_A = 25°C; V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	1, 11	
		HCNW4562		0.54					
		HCPL-4562		0.8			T_A = -10°C; V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz		
				1.5			T_A = 70°C; V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz		
	ΔG_V (10 MHz)	HCPL-4562		1.15		-dB	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz		
		HCNW4562		2.27					
Differential Gain at f = 3.58 MHz		HCPL-4562		± 1.0		%	I_{Fac} = 0.7 mA p-p, I_{Fdc} = 3 to 9 mA	3, 7	8
		HCNW4562		± 0.9			I_{Fac} = 1 mA p-p, I_{Fdc} = 7 to 13 mA		
Differential Phase at f = 3.58 MHz		HCPL-4562		± 1		deg.	I_{Fac} = 0.7 mA p-p, I_{Fdc} = 3 to 9 mA	3, 7	9
		HCNW4562		± 0.6			I_{Fac} = 1 mA p-p, I_{Fdc} = 7 to 13 mA		
Total Harmonic Distortion	THD	HCPL-4562		2.5		%	V_{IN} = 1 V_{P-P}, f = 3.58 MHz, G_V = 2	4	10
		HCNW4562		0.75					
Output Noise Voltage	V_O(noise)			950		µV rms	10 Hz to 10 MHz	1	
Isolation Mode Rejection Ratio	IMRR	HCPL-4562		122		dB	f = 120 Hz, G_V = 2	14	11
		HCNW4562		119					

Package Characteristics

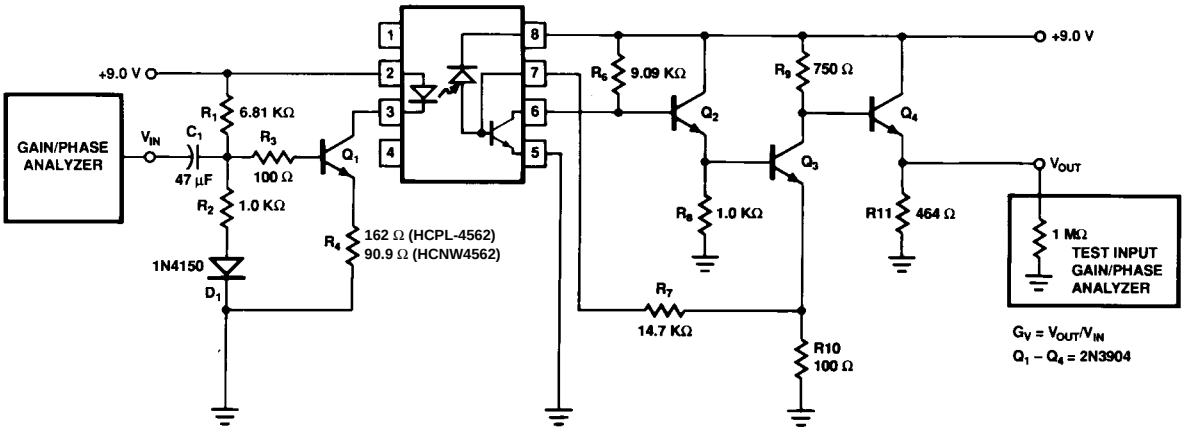
All Typicals at $T_A = 25°C$

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	HCPL-4562	2500			V rms	RH ≤ 50%, t = 1 min., $T_A = 25°C$		5, 12
		HCNW4562	5000						5, 13
		HCPL-4562 (Option 020)	5000						5, 13
Input-Output Resistance	R_{I-O}	HCPL-4562		10^{12}		Ω	V_{I-O} = 500 Vdc		5
		HCNW4562	10^{12}	10^{13}			$T_A = 25°C$		
			10^{11}				$T_A = 100°C$		
Input-Output Capacitance	C_{I-O}	HCPL-4562		0.6		pF	f = 1 MHz		5
		HCNW4562		0.5	0.6				

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. When used in the circuit of Figure 1 or Figure 4; $G_V = V_{OUT}/V_{IN}$; I_{FQ} = 6 mA (HCPL-4562), I_{FQ} = 10 mA (HCNW4562).
2. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C (HCPL-4562).
3. Maximum variation from the best fit line of I_{PB} vs. I_F expressed as a percentage of the peak-to-peak full scale output.
4. CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
5. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
6. Flat-band, small-signal voltage gain.
7. The frequency at which the gain is 3 dB below the flat-band gain.
8. Differential gain is the change in the small-signal gain of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
9. Differential phase is the change in the small-signal phase response of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
10. TOTAL HARMONIC DISTORTION (THD) is defined as the square root of the sum of the square of each harmonic distortion component. The THD of the isolated video circuit is measured using a 2.6 kΩ load in series with the 50 Ω input impedance of the spectrum analyzer.
11. ISOLATION MODE REJECTION RATIO (IMRR), a measure of the optocoupler's ability to reject signals or noise that may exist between input and output terminals, is defined by $20 \log_{10} [(V_{OUT}/V_{IN})/(V_{OUT}/V_{IM})]$, where V_{IM} is the isolation mode voltage signal.
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.



NOTE: ALL RESISTORS ARE 1% TOLERANCE

Figure 1. Gain and Bandwidth Test Circuit.

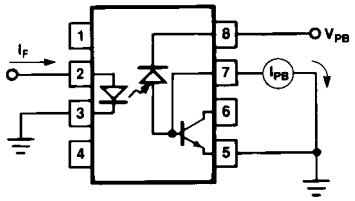


Figure 2. Base Photo Current Test Circuit.

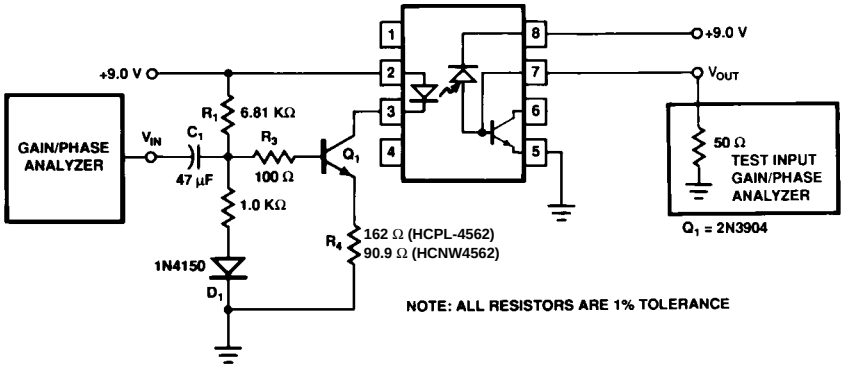


Figure 3. Base Photo Current Frequency Response Test Circuit.

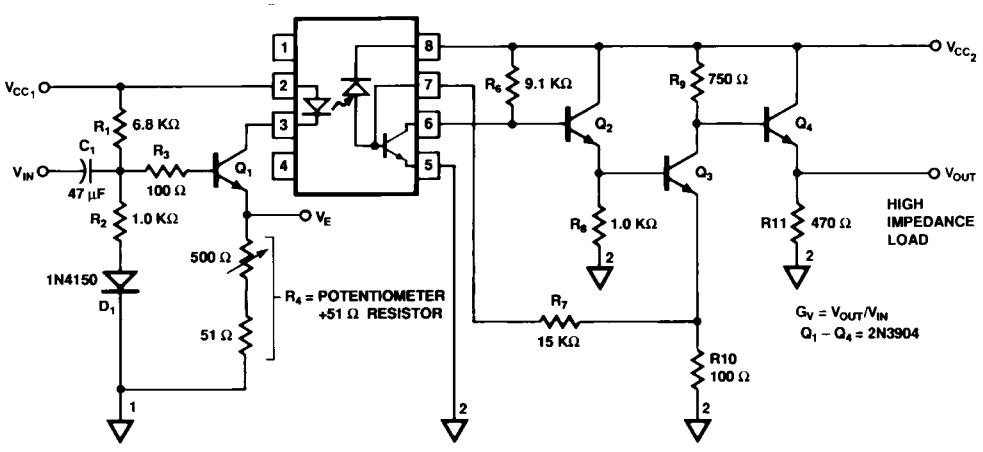


Figure 4. Recommended Isolated Video Interface Circuit.

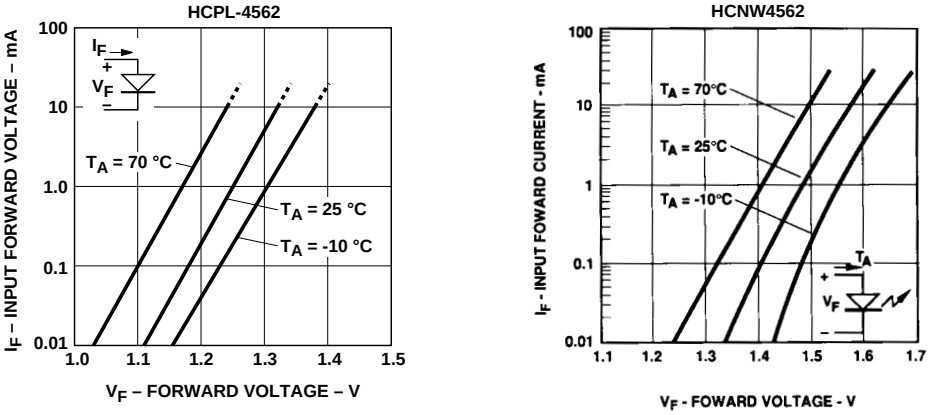


Figure 5. Input Current vs. Forward Voltage.

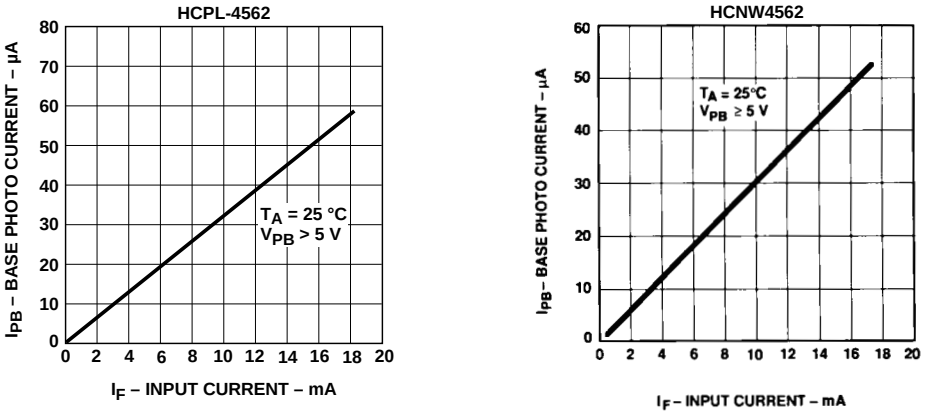


Figure 6. Base Photo Current vs. Input Current.

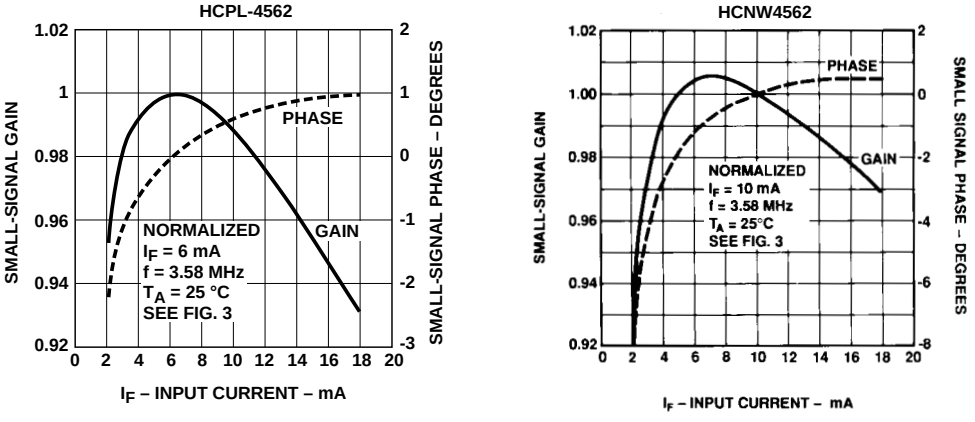


Figure 7. Small-Signal Response vs. Input Current.

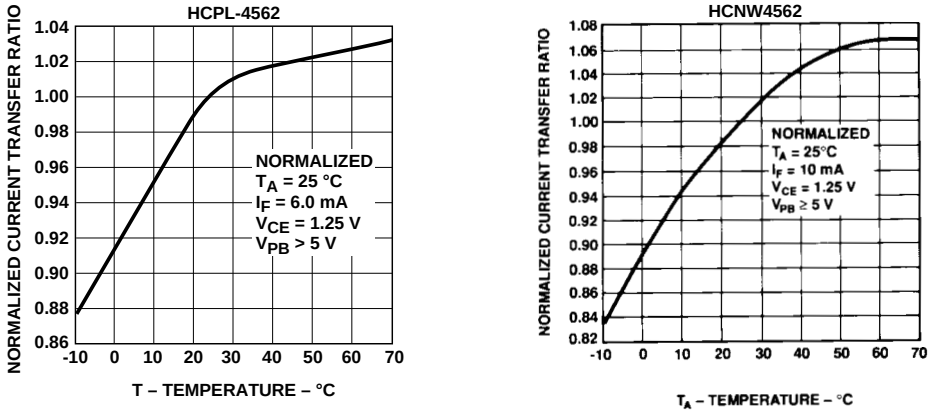


Figure 8. Current Transfer Ratio vs. Temperature.

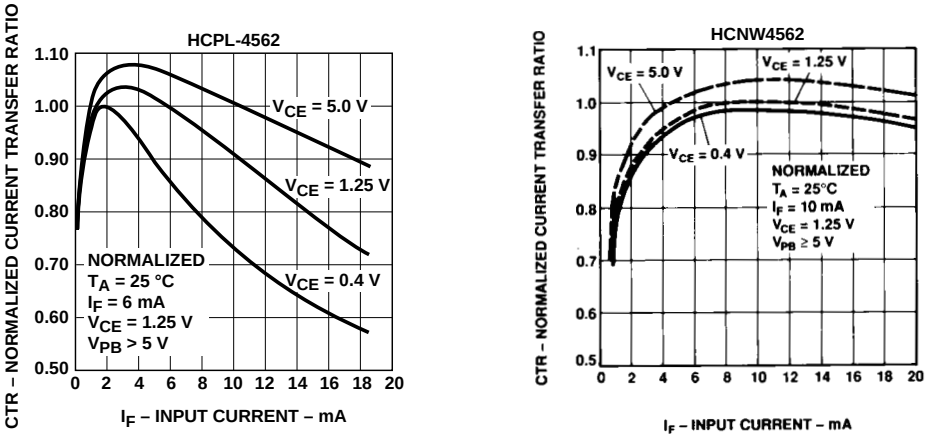


Figure 9. Current Transfer Ratio vs. Input Current.

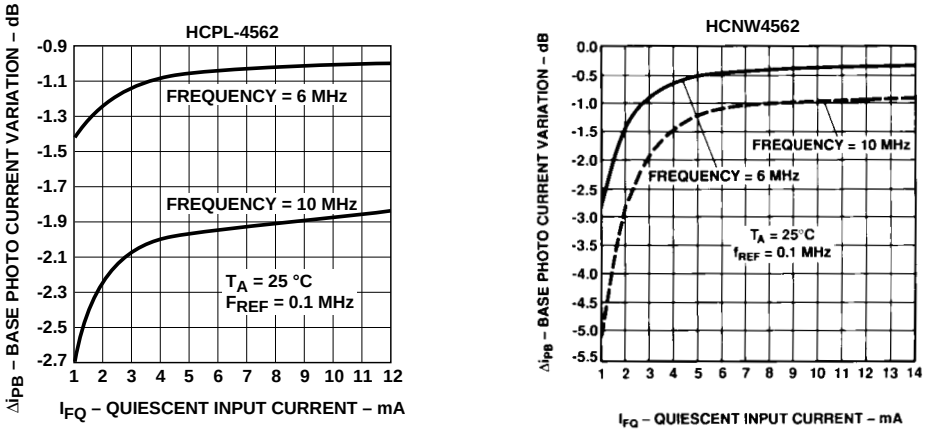


Figure 10. Base Photo Current Variation vs. Bias Conditions.

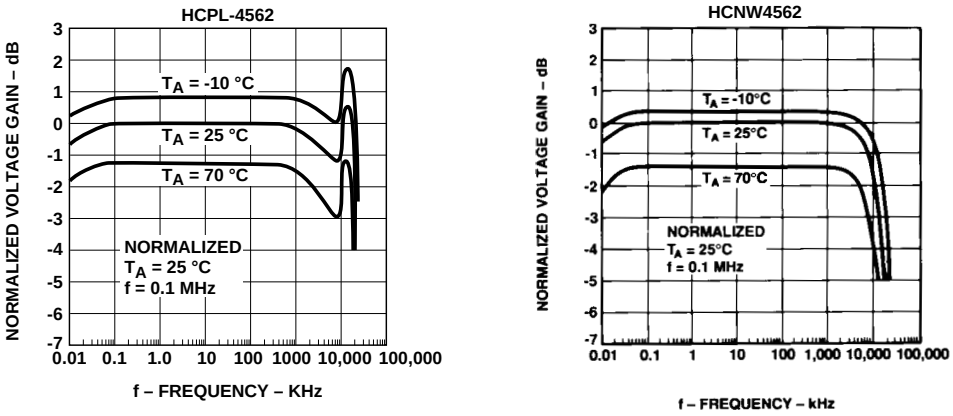


Figure 11. Normalized Voltage Gain vs. Frequency.

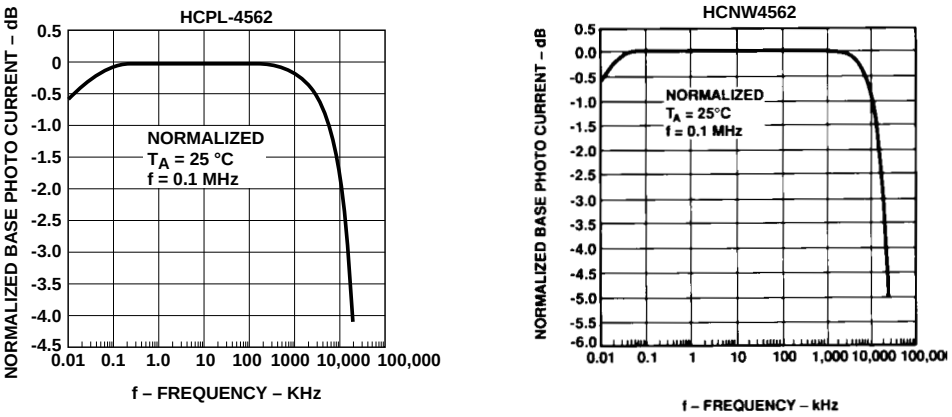


Figure 12. Normalized Base Photo Current vs. Frequency.

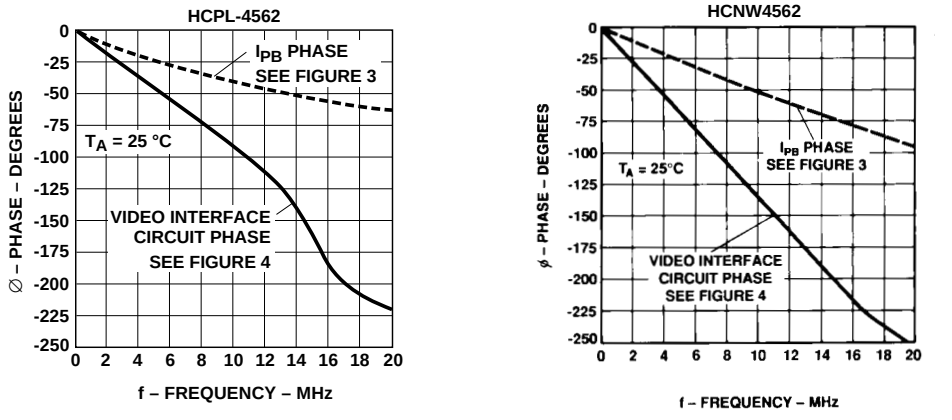


Figure 13. Phase vs. Frequency.

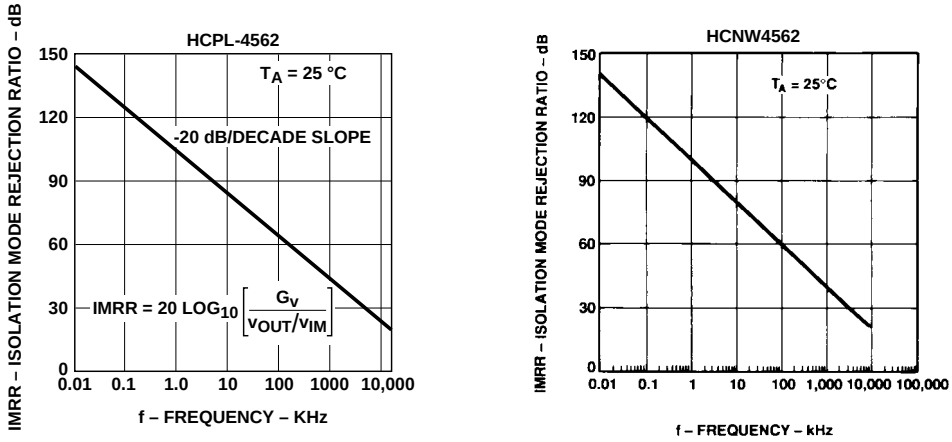


Figure 14. Isolation Mode Rejection Ratio vs. Frequency.

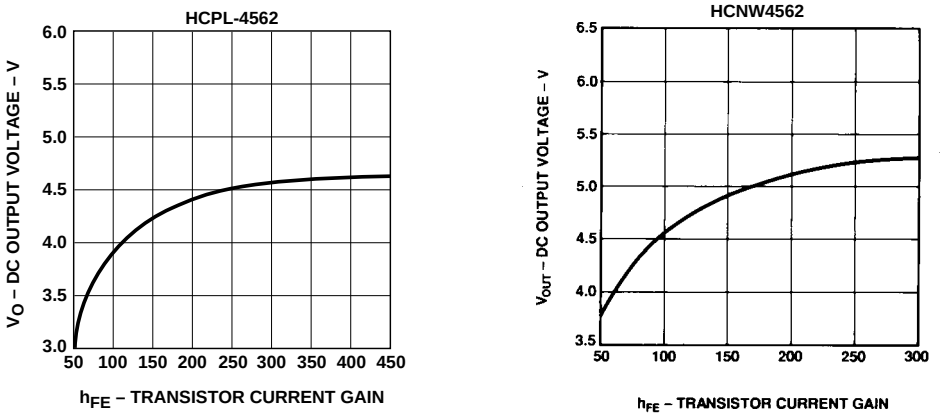


Figure 15. DC Output Voltage vs. Transistor Current Gain.

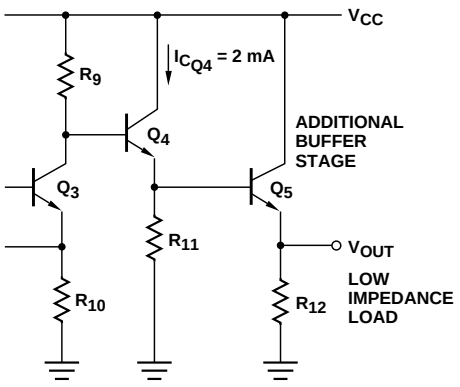


Figure 16. Output Buffer Stage for Low Impedance Loads.

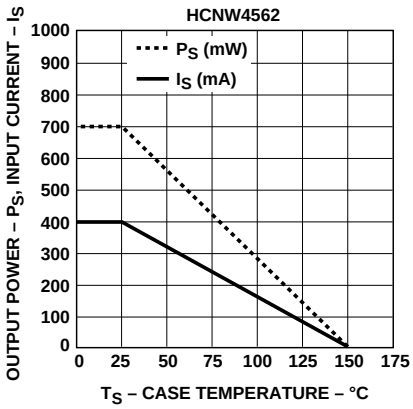


Figure 17. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

Conversion from HCPL-4562 to HCNW4562

In order to obtain similar circuit performance when converting from the HCPL-4562 to the HCNW4562, it is recommended to increase the Quiescent Input Current, I_{FQ}, from 6 mA to 10 mA. If the application circuit in Figure 4 is used, then potentiometer R4 should be adjusted appropriately.

Design Considerations of the Application Circuit

The application circuit in Figure 4 incorporates several features that help maximize the bandwidth performance of the HCPL-4562/HCNW4562. Most important of these features is peaked response of the detector circuit that helps extend the frequency range over which the voltage gain is relatively constant. The number of gain stages, the overall circuit topology, and the choice of DC bias points are all consequences of the desire to maximize bandwidth performance.

To use the circuit, first select R_1 to set V_E for the desired LED quiescent current by:

$$I_{FQ} = \frac{V_E}{R_4} \cong \frac{G_V\, V_E\, R_{10}}{(\partial I_{PB}/\partial I_F)\, R_7 R_9} \quad (1)$$

For a constant value $V_{INp\text{-}p}$, the circuit topology (adjusting the gain with R_4) preserves linearity by keeping the modulation factor (MF) dependent only on V_E.

$$i_{F_{p\text{-}p}} \cong V_{IN}/R_4 \quad (2)$$

$$\frac{i_{F\,p\text{-}p}}{I_{FQ}} \cong \frac{i_{PB\,p\text{-}p}}{I_{PBQ}} = \frac{V_{INp\text{-}p}}{V_E} \quad (3)$$

Modulation Factor (MF): $$\frac{i_{F\,(p\text{-}p)}}{2\, I_{FQ}} = \frac{V_{INp\text{-}p}}{2\, V_E} \quad (4)$$

For a given G_V, V_E, and V_{CC}, DC output voltage will vary only with h_{FEX}.

$$V_O = V_{CC} - V_{BE_4} - \frac{R_9}{R_{10}}\,[V_{BEX} - (I_{PBQ} - I_{BXQ})\, R_7] \quad (5)$$

Where:

$$I_{PBQ} \cong \frac{G_V\, V_E R_{10}}{R_7 R_9} \quad (6)$$

and,

$$I_{BXQ} \cong \frac{V_{CC} - 2\, V_{BE}}{R_6\, h_{FEX}} \quad (7)$$

Figure 15 shows the dependency of the DC output voltage on h_{FEX}.

For 9 V < V_{CC} < 12 V, select the value of R_{11} such that

$$I_{C_{Q4}} \cong \frac{V_O}{R_{11}} \leq \frac{4.25\ V}{470\ \Omega} \leq 9.0\ mA \quad (8)$$

The voltage gain of the second stage (Q_3) is approximately equal to:

$$\frac{R_9}{R_{10}} * \frac{1}{1 + s\, R_9 \left[C_{CQ_3} + \frac{1}{2\pi\, R'_{11}\, f_{T_4}}\right]} \quad (9)$$

Increasing R'_{11} (R'_{11} includes the parallel combination of R_{11} and the load impedance) or reducing R_9 (keeping R_9/R_{10} ratio constant) will improve the bandwidth.

If it is necessary to drive a low impedance load, bandwidth may also be preserved by adding an additional emitter following the buffer stage (Q_5 in Figure 16), in which case R_{11} can be increased to set $I_{CQ4} \cong 2$ mA.

Finally, adjust R_4 to achieve the desired voltage gain.

$$G_V \cong \frac{V_{OUT}}{V_{IN}} \cong \frac{\partial I_{PB}}{\partial I_F}\left[\frac{R_7 R_9}{R_4 R_{10}}\right] \quad (10)$$

where typically $\frac{\partial I_{PB}}{\partial I_F} = 0.0032$

Definition:

G_V = Voltage Gain
I_{FQ} = Quiescent LED forward current
$i_{Fp\text{-}p}$ = Peak-to-peak small signal LED forward current
$V_{INp\text{-}p}$ = Peak-to-peak small signal input voltage
$i_{PBp\text{-}p}$ = Peak-to-peak small signal base photo current
I_{PBQ} = Quiescent base photo current
V_{BEX} = Base-Emitter voltage of HCPL-4562/HCNW4562 transistor
I_{BXQ} = Quiescent base current of HCPL-4562/HCNW4562 transistor
h_{FEX} = Current Gain (I_C/I_B) of HCPL-4562/HCNW4562 transistor
V_E = Voltage across emitter degeneration resistor R_4
f_{T_4} = Unity gain frequency of Q_5
C_{CQ_3} = Effective capacitance from collector of Q_3 to ground