

## INTEGRATED CIRCUITS

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT652

Octal bus transceiver/register;  
3-state

Product specification  
File under Integrated Circuits, IC06

September 1993

## Octal bus transceiver/register; 3-state

## 74HC/HCT652

## FEATURES

- Multiplexed real-time and stored data
- Independent register for A and B buses
- Independent enables for A and B buses
- 3-state
- Output capability: Bus driver
- Low power consumption by CMOS technology
- I<sub>CC</sub> category: MSI.

## APPLICATIONS

- Bus interfaces.

## DESCRIPTION

The 74HC/HCT652 are high-speed SI-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in

compliance with Jedec standard no. 7A.

The 74HC/HCT652 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and central circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropriate clock pins (CP<sub>AB</sub> or CP<sub>BA</sub>) regardless of the select pins (S<sub>AB</sub> and S<sub>BA</sub>) or output enable (OE<sub>AB</sub> and OE<sub>BA</sub>) control pins. Depending on the select inputs S<sub>AB</sub> and S<sub>BA</sub> data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the output enable pins this operating mode permits. The output enable pins OE<sub>AB</sub> and OE<sub>BA</sub> determine the operation mode of the transceiver. When OE<sub>AB</sub> is LOW, no data transmission from A<sub>n</sub> to B<sub>n</sub> is

possible and when OE<sub>BA</sub> is HIGH, there is no data transmission from B<sub>n</sub> to A<sub>n</sub> possible. When S<sub>AB</sub> and S<sub>BA</sub> are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE<sub>AB</sub> and OE<sub>BA</sub>. In this configuration each output reinforces its input. Thus when all other data sources to the two sets of bus lines are at high-impedance, each set of the bus lines will remain at its last state. This type differs from the HC/HCT646 in one extra bus-management function. This is the possibility to transfer stored "A data to the "B" bus and transfer stored "B" data to the "A" bus at the same time. The examples at the application information demonstrate all bus management functions. Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25°C; t<sub>r</sub> = t<sub>f</sub> = 6 ns; V<sub>CC</sub> = 4.5 V; C<sub>L</sub> = 50 pF.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PLH</sub> /t <sub>PZL</sub>	propagation delay A <sub>n</sub> /B <sub>n</sub> to B <sub>n</sub> /A <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	13	13	ns
	propagation delay CP <sub>AB</sub> /CP <sub>BA</sub> to B <sub>n</sub> /A <sub>n</sub>		18	20	ns
	propagation delay S <sub>AB</sub> /S <sub>BA</sub> to B <sub>n</sub> /A <sub>n</sub>		20	23	ns
t <sub>PHZ</sub> /t <sub>PZL</sub>	3-state output enable time OE <sub>AB</sub> /OE <sub>BA</sub> to B <sub>n</sub> /A <sub>n</sub>		14	15	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE <sub>AB</sub> /OE <sub>BA</sub> to B <sub>n</sub> /A <sub>n</sub>		12	13	ns
f <sub>max</sub>	maximum clock frequency		92	92	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per channel	notes 1 and 2	26	28	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; C<sub>L</sub> = output load capacitance in pF;

f<sub>o</sub> = output frequency in MHz; V<sub>CC</sub> = supply voltage in V;

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

Octal bus transceiver/register; 3-state

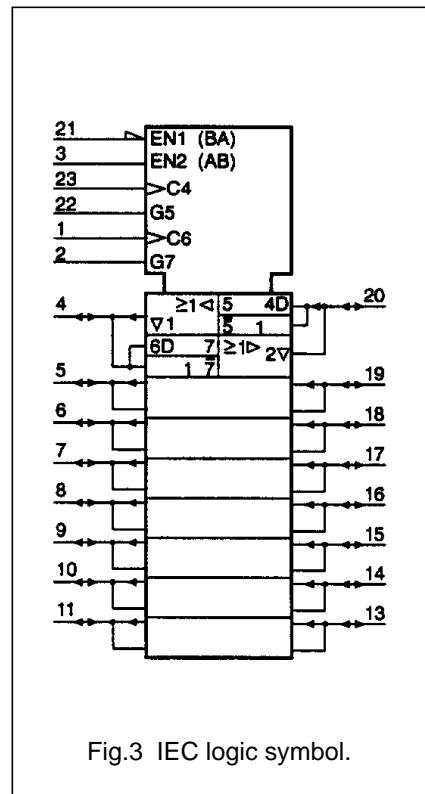
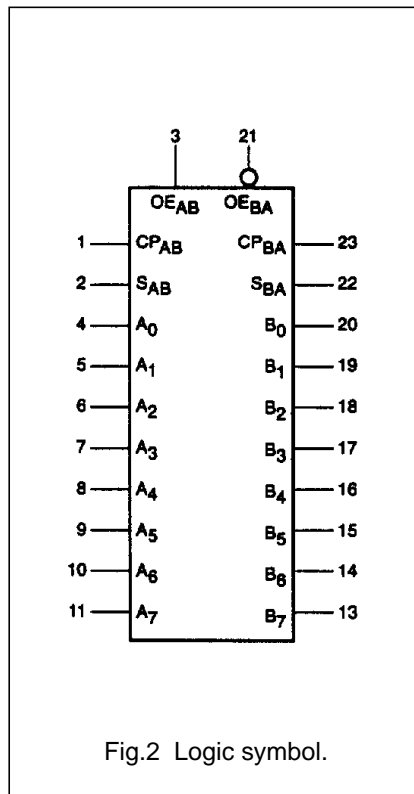
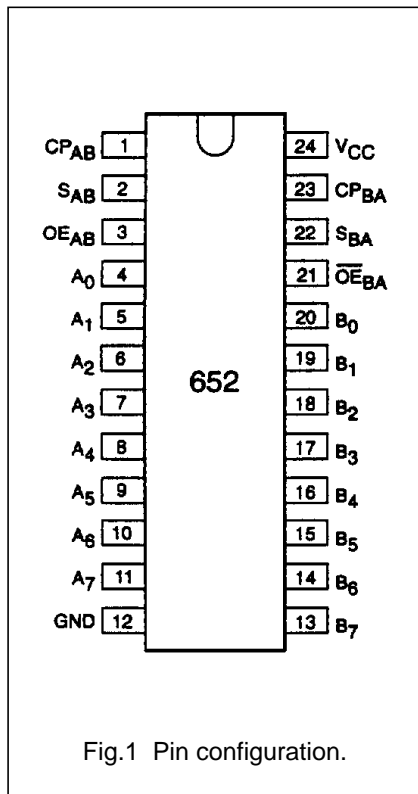
74HC/HCT652

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT652N	24	DIL	plastic	SOT101L
74HC/HCT652D	24	SO	plastic	SOT137A

PINNING

SYMBOL	PIN	DESCRIPTION
CP <sub>AB</sub>	1	A to B clock input
S <sub>AB</sub>	2	select A to B source input
OE <sub>AB</sub>	3	output enable A to B input
A <sub>0</sub> ..A <sub>7</sub>	4..11	A data inputs/outputs
GND	12	ground (0 V)
B <sub>7</sub> ..B <sub>0</sub>	13..20	B data inputs/outputs
OE <sub>BA</sub>	21	output enable B to A input
S <sub>BA</sub>	22	select B to A source input
CP <sub>BA</sub>	23	B to A clock input
V <sub>CC</sub>	24	positive supply voltage



Octal bus transceiver/register; 3-state

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FUNCTION TABLE

INPUTS <sup>(1)</sup>						DATA I/O <sup>(2)</sup>		OPERATION OR FUNCTION
OE <sub>AB</sub>	OE <sub>BA</sub>	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>	A <sub>1</sub> THRU A <sub>8</sub>	B <sub>1</sub> THRU B <sub>8</sub>	HC/HCT652
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B
L	L	↑	↑	X	L	Ouput	Input	Store B in both registers
L	L	X	X	X	L	Ouput	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H	Ouput	Input	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes

- H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH transition
- The data output functions may be enabled or disabled by various signals at OE<sub>AB</sub> and OE<sub>BA</sub> inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

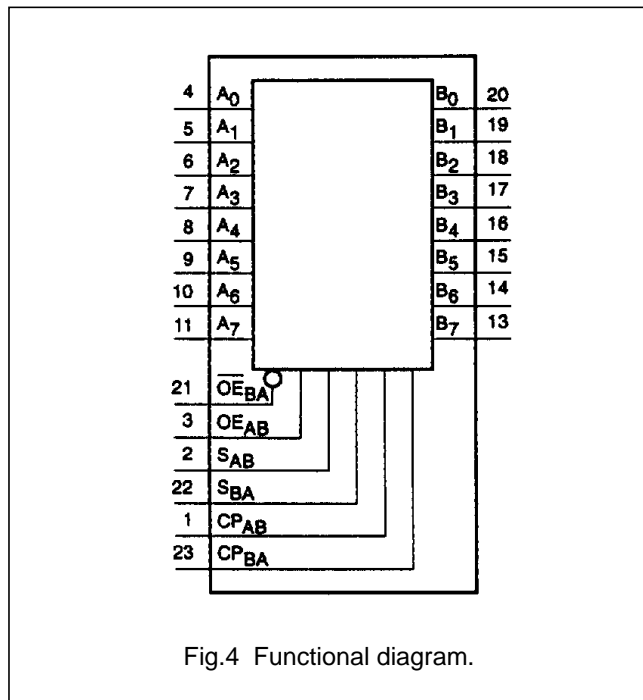


Fig.4 Functional diagram.

Octal bus transceiver/register; 3-state

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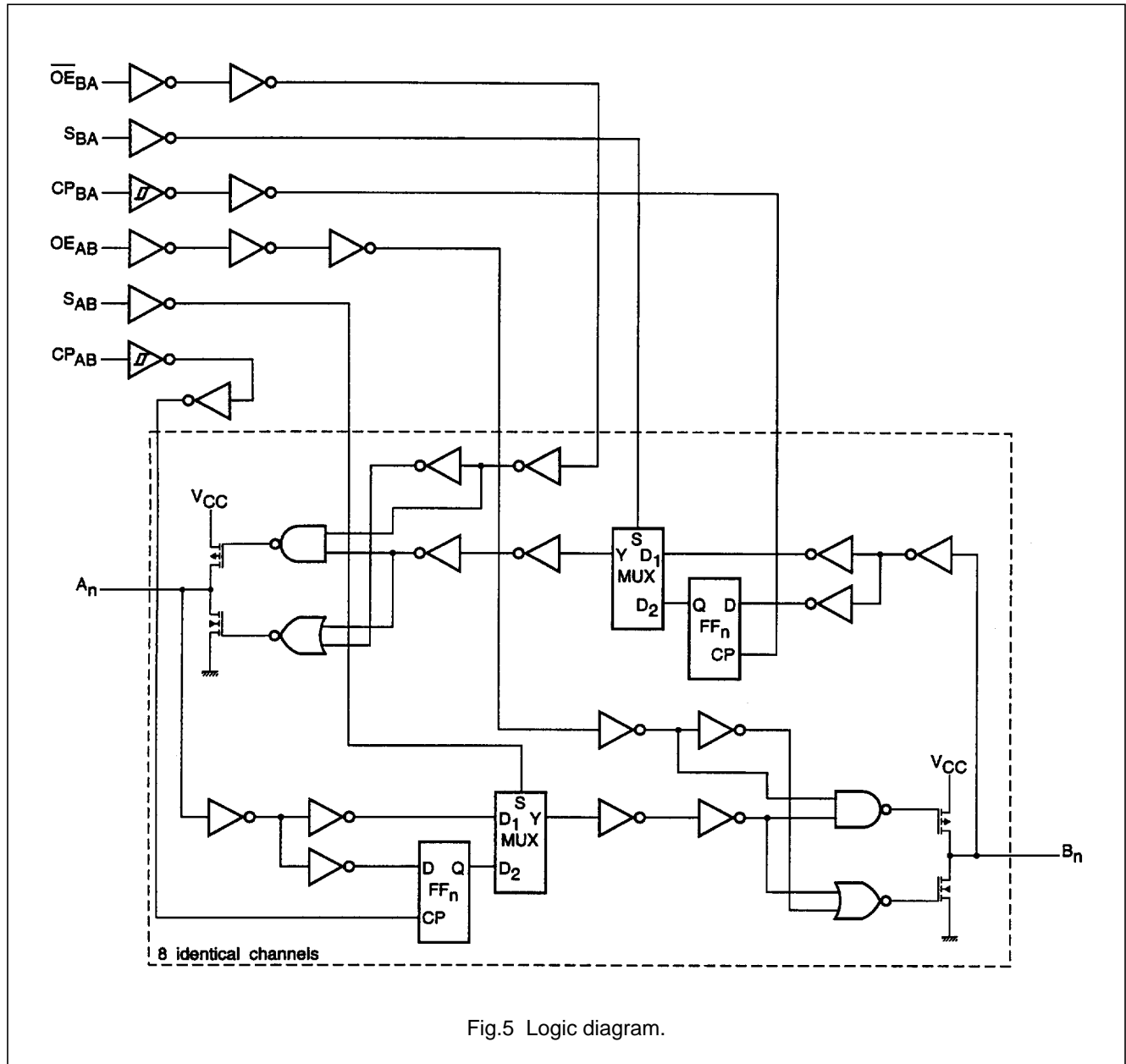


Fig.5 Logic diagram.

## Octal bus transceiver/register; 3-state

## 74HC/HCT652

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI.

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF.

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub>	–	44	135	–	170	–	205	ns	2.0	Fig.6	
		–	16	27	–	34	–	41	4.5			
		–	13	23	–	29	–	35	6.0			
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay CP <sub>AB</sub> , CP <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>	–	61	190	–	240	–	285	ns	2.0	Fig.7	
		–	22	38	–	48	–	57	4.5			
		–	18	32	–	41	–	48	6.0			
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay S <sub>AB</sub> , S <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>	–	63	195	–	245	–	295	ns	2.0	Fig.8	
		–	23	39	–	49	–	59	4.5			
		–	18	33	–	42	–	50	6.0			
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE <sub>AB</sub> , $\overline{\text{OE}}_{\text{BA}}$ to A <sub>n</sub> , B <sub>n</sub>	–	47	150	–	190	–	225	ns	2.0	Fig.9	
		–	17	30	–	38	–	45	4.5			
		–	14	26	–	33	–	38	6.0			
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE <sub>AB</sub> , $\overline{\text{OE}}_{\text{BA}}$ to A <sub>n</sub> , B <sub>n</sub>	–	41	150	–	190	–	225	ns	2.0	Fig.9	
		–	15	30	–	38	–	45	4.5			
		–	12	26	–	33	–	38	6.0			
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	–	14	60	–	75	–	90	ns	2.0	Figs 6, 8	
		–	5	12	–	15	–	18	4.5			
		–	4	10	–	13	–	15	6.0			
t <sub>W</sub>	clock pulse width HIGH or LOW CP <sub>AB</sub> or CP <sub>BA</sub>	80	17	–	100	–	120	–	ns	2.0	Fig.7	
		16	6	–	20	–	24	–	4.5			
		14	5	–	17	–	20	–	6.0			
t <sub>SU</sub>	set-up time A <sub>n</sub> , B <sub>n</sub> to CP <sub>AB</sub> , CP <sub>BA</sub>	100	17	–	125	–	150	–	ns	2.0	Fig.7	
		20	6	–	25	–	30	–	4.5			
		17	5	–	21	–	26	–	6.0			
t <sub>H</sub>	hold time A <sub>n</sub> , B <sub>n</sub> to CP <sub>AB</sub> , CP <sub>BA</sub>	25	–8	–	30	–	35	–	ns	2.0	Fig.7	
		5	–3	–	6	–	7	–	4.5			
		4	–2	–	5	–	6	–	6.0			
f <sub>max</sub>	maximum clock pulse frequency	6.0	16	–	4.8	–	4.0	–	MHz	2.0	Fig.7	
		30	83	–	24	–	20	–	4.5			
		35	98	–	28	–	24	–	6.0			

## Octal bus transceiver/register; 3-state

## 74HC/HCT652

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

$I_{CC}$  category: MSI.

**Note to the HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for unit a load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below

INPUT	UNIT LOAD COEFFICIENT
$S_{AB}, S_{BA}$	0.75
$A_0$ to $A_7$ and $B_0$ to $B_7$	0.75
$CP_{AB}, CP_{BA}$	1.50
$OE_{AB}$	1.50
$\overline{OE}_{BA}$	1.50

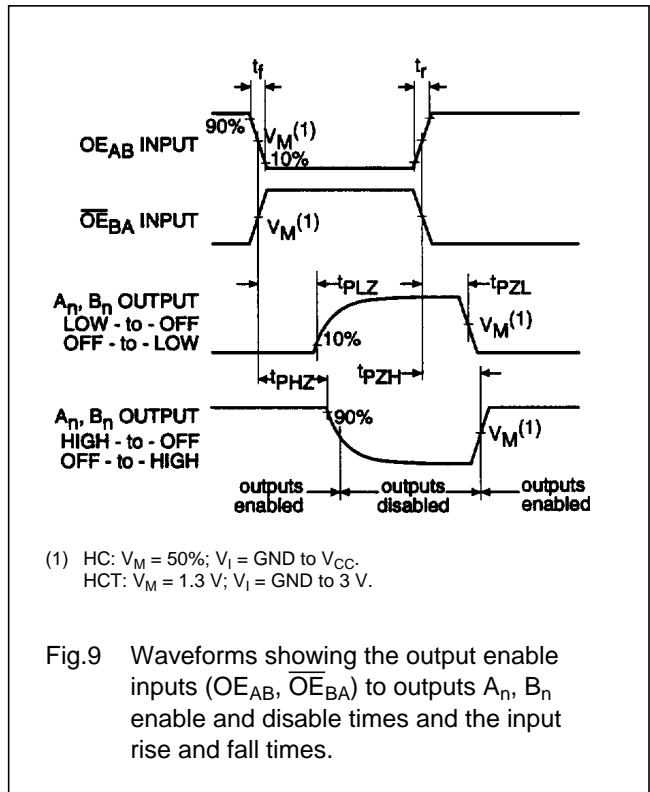
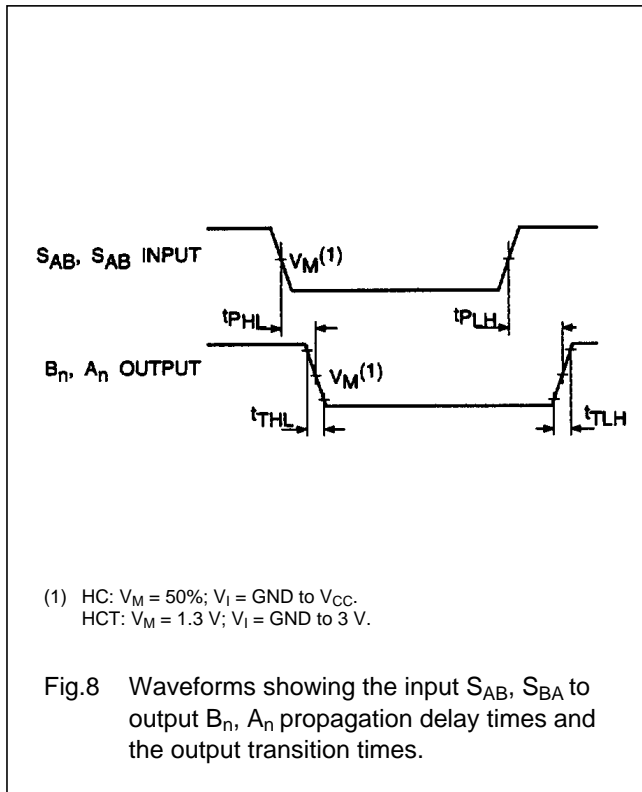
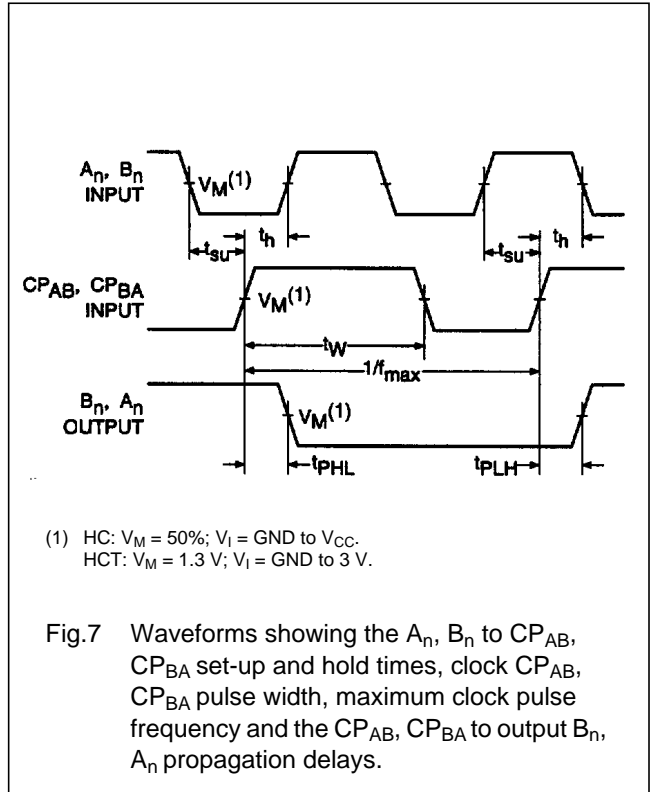
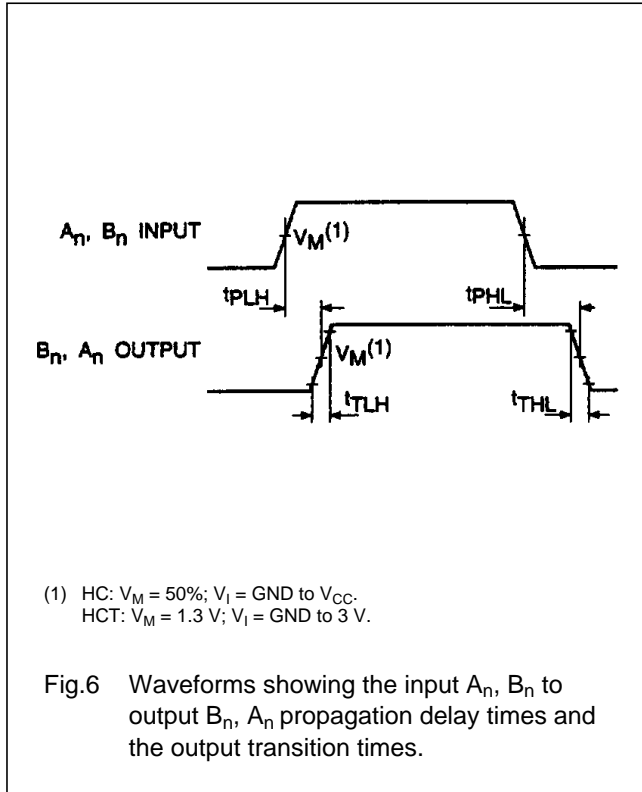
**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

INPUT	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125		$V_{CC}$ (V)		WAVEFORMS	
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
$t_{PHL}/t_{PLH}$	propagation delay $A_n, B_n$ to $B_n, A_n$	–	16	27	–	34	–	41	ns	4.5	Fig.6	
$t_{PHL}/t_{PLH}$	propagation delay $CP_{AB}, CP_{BA}$ to $B_n, A_n$	–	23	39	–	49	–	59	ns	4.5	Fig.7	
$t_{PHL}/t_{PLH}$	propagation delay $S_{AB}, S_{BA}$ to $B_n, A_n$	–	27	46	–	55	–	66	ns	4.5	Fig.8	
$t_{PZH}/t_{PZL}$	3-state output enable time $OE_{AB}, \overline{OE}_{BA}$ to $A_n, B_n$	–	18	33	–	41	–	50	ns	4.5	Fig.9	
$t_{PHZ}/t_{PLZ}$	3-state output disable time $OE_{AB}, \overline{OE}_{BA}$ to $A_n, B_n$	–	16	35	–	44	–	53	ns	4.5	Fig.9	
$t_{THL}/t_{TLH}$	output transition time	–	5	12	–	15	–	18	ns	4.5	Fig.6, 8	
$t_W$	clock pulse width HIGH or LOW $CP_{AB}$ or $CP_{BA}$	16	6	–	20	–	24	–	ns	4.5	Fig.7	
$t_{su}$	set-up time $A_n, B_n$ to $CP_{AB}, CP_{BA}$	10	5	–	13	–	15	–	ns	4.5	Fig.7	
$t_h$	hold time $A_n, B_n$ to $CP_{AB}, CP_{BA}$	5	–2	–	6	–	8	–	ns	4.5	Fig.7	
$f_{max}$	maximum clock pulse frequency	30	83	–	24	–	20	–	MHz	4.5	Fig.7	

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APPLICATION INFORMATION

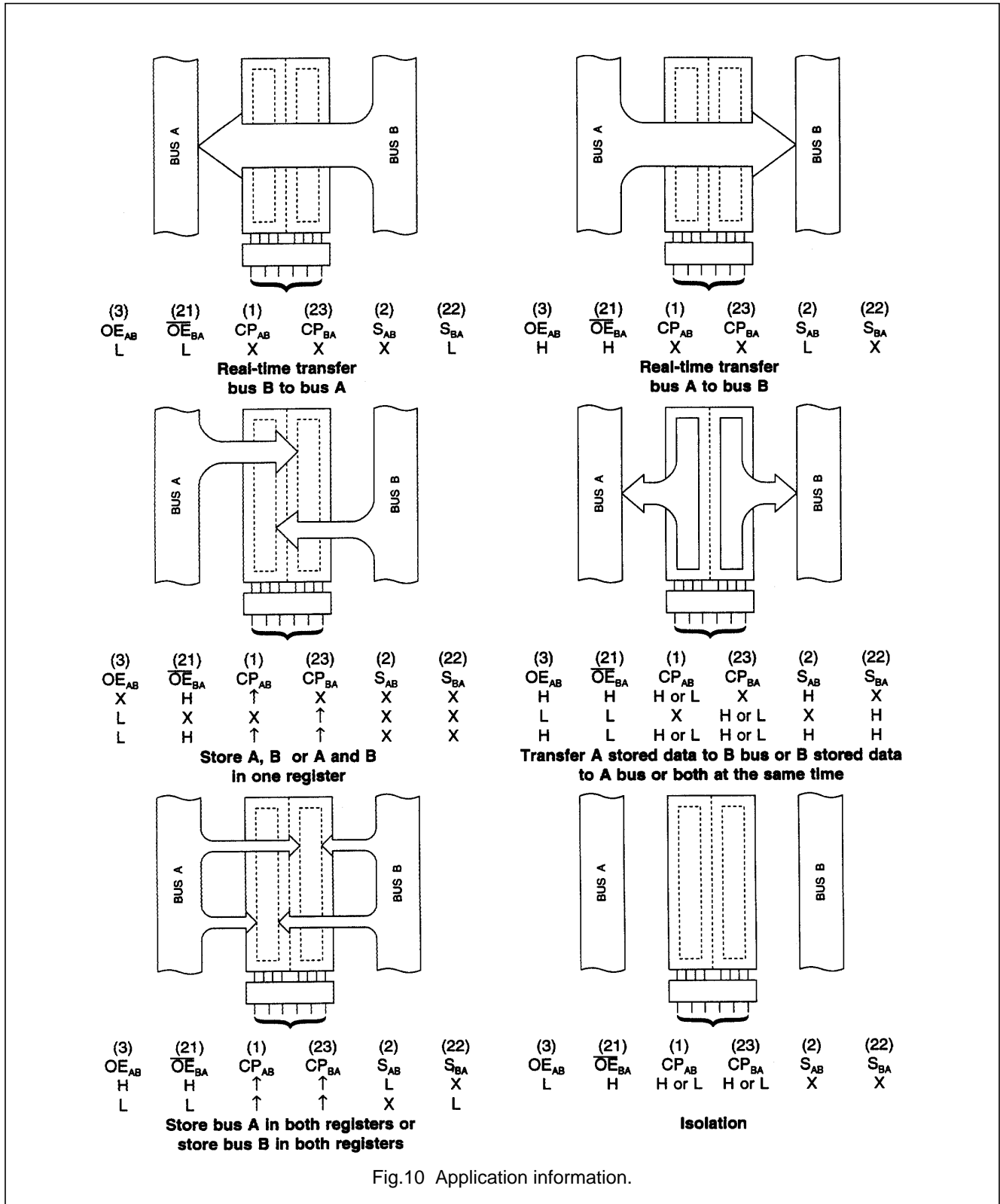


Fig.10 Application information.

Octal bus transceiver/register; 3-state

74HC/HCT652

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**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.