

August 1995

**Radiation Hardened
Quad 2-Input AND Gate****Features**

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD(Si)
- SEP Effective LET No Upsets: >100 MEV-cm 2 /mg
- Single Event Upset (SEU) Immunity $<2 \times 10^{-9}$ Errors/Bit-Day (Typ)
- Dose Rate Survivability: $>1 \times 10^{12}$ Rads (Si)/Sec
- Dose Rate Upset $>10^{10}$ RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
 - VIL = 0.8V
 - VIH = VCC/2
- Input Current Levels $I_i \leq 5\mu A$ at VOL, VOH

Description

The Intersil HCTS08MS is a Radiation Hardened Quad 2-Input AND Gate. A high on both inputs force the output to a High state.

The HCTS08MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

The HCTS08MS is supplied in a 14 lead Ceramic Flatpack Package (K suffix) or a 14 lead SBDIP Package (D suffix).

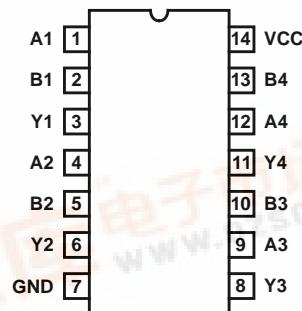
Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCTS08DMSR	-55°C to +125°C	Intersil Class S Equivalent	14 Lead SBDIP
HCTS08KMSR	-55°C to +125°C	Intersil Class S Equivalent	14 Lead Ceramic Flatpack
HCTS08D/ Sample	+25°C	Sample	14 Lead SBDIP
HCTS08K/ Sample	+25°C	Sample	14 Lead Ceramic Flatpack
HCTS08HMSR	+25°C	Die	Die

Pinouts

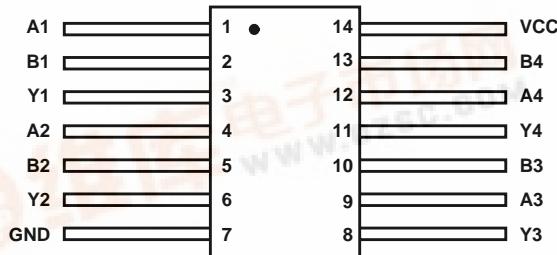
14 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T14

TOP VIEW



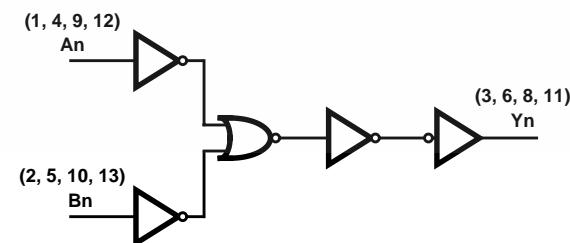
14 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP3-F14

TOP VIEW

**TRUTH TABLE**

INPUTS		OUTPUTS
An	Bn	Yn
L	L	L
L	H	L
H	L	L
H	H	H

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram

Specifications HCTS08MS

Absolute Maximum Ratings

Supply Voltage	-0.5V to +7.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	$\pm 10\text{mA}$
DC Drain Current, Any One Output	$\pm 25\text{mA}$
(All Voltage Reference to the VSS Terminal)	
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1

Reliability Information

	θ_{JA}	θ_{JC}
SBDIP Package	74°C/W	24°C/W
Ceramic Flatpack Package	116°C/W	30°C/W
Maximum Package Power Dissipation at +125°C		
SBDIP Package	0.66W	
Ceramic Flatpack Package	0.43W	
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:		
SBDIP Package	13.5mW/°C	
Ceramic Flatpack Package	8.6mW/°C	

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage	+4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF)	100ns/V Max
Operating Temperature Range (T _A)	-55°C to +125°C

Input Low Voltage (VIL)	0.0V to 0.8V
Input High Voltage (VIH)	VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	4.0	0.5	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO \geq 4.0V is recognized as a logic "1", and VO \leq 0.5V is recognized as a logic "0".

Specifications HCTS08MS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume $RL = 500\Omega$, $CL = 50\text{pF}$, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	-	45	pF
			1	+125°C, -55°C	-	80	pF
Input Capacitance	CIN	VCC = 5.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, IOL = 50µA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, IOH = -50µA	+25°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5.0	+5.0	µA

Specifications HCTS08MS

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, (Note 3)	+25°C	-	-	-
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	ns
	TPLH	VCC = 4.5V	+25°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume $RL = 500\Omega$, $CL = 50\text{pF}$, Input TR = TF = 3ns, $VIL = \text{GND}$, $VIH = 3\text{V}$.
3. For functional tests, $VO \geq 4.0\text{V}$ is recognized as a logic "1", and $VO \leq 0.5\text{V}$ is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3 μ A
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	
		TESTED	RECORDED
Initial Test	100% 5004	1, 7, 9	1 (Note 2)
Interim Test	100% 5004	1, 7, 9, Δ	1, Δ (Note 2)
PDA	100% 5004	1, 7, Δ	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	1, 2, 3, Δ (Note 2)
Subgroup B6	Sample 5005	1, 7, 9	
Group D	Sample 5005	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 Method 5005 may be exercised.
2. Table 5 parameters only.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

Specifications HCTS08MS

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V \pm 0.5V	VCC = 6V \pm 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

1. Each pin except VCC and GND will have a resistor of $10\text{K}\Omega \pm 5\%$ for static burn-in.
2. Each pin except VCC and GND will have a resistor of $1\text{K}\Omega \pm 5\%$ for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V \pm 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of $47\text{K}\Omega \pm 5\%$ for irradiation testing.
Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

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Intersil Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)	100% Interim Electrical Test 1 (T1)
GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects	100% Delta Calculation (T0-T1) 100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015
100% Nondestructive Bond Pull, Method 2023	100% Interim Electrical Test 2 (T2)
Sample - Wire Bond Pull Monitor, Method 2011	100% Delta Calculation (T0-T2)
Sample - Die Shear Monitor, Method 2019 or 2027	100% PDA 1, Method 5004 (Notes 1and 2)
100% Internal Visual Inspection, Method 2010, Condition A	100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015
100% Temperature Cycle, Method 1010, Condition C, 10 Cycles	100% Interim Electrical Test 3 (T3)
100% Constant Acceleration, Method 2001, Condition per Method 5004	100% Delta Calculation (T0-T3)
100% PIND, Method 2020, Condition A	100% PDA 2, Method 5004 (Note 2)
100% External Visual	100% Final Electrical Test
100% Serialization	100% Fine/Gross Leak, Method 1014
100% Initial Electrical Test (T0)	100% Radiographic, Method 2012 (Note 3)
100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015	100% External Visual, Method 2009 Sample - Group A, Method 5005 (Note 4) 100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.

5. Data Package Contents:

- Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
- Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
- GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
- X-Ray report and film. Includes penetrometer measurements.
- Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
- Lot Serial Number Sheet (Good units serial number and lot number).
- Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
- The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

HCTS08MS

AC Timing Diagrams

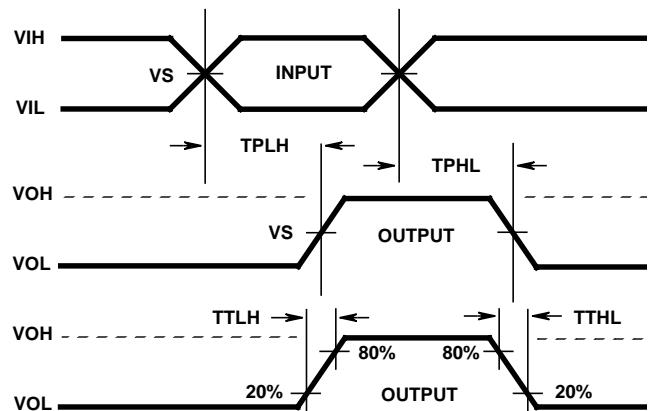


FIGURE 1

AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit

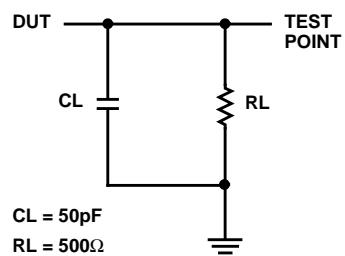


FIGURE 2

HCTS08MS

Die Characteristics

DIE DIMENSIONS:

87 x 88 mils
2.20 x 2.24mm

METALLIZATION:

Type: SiAl
Metal Thickness: $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: SiO_2
Thickness: $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:

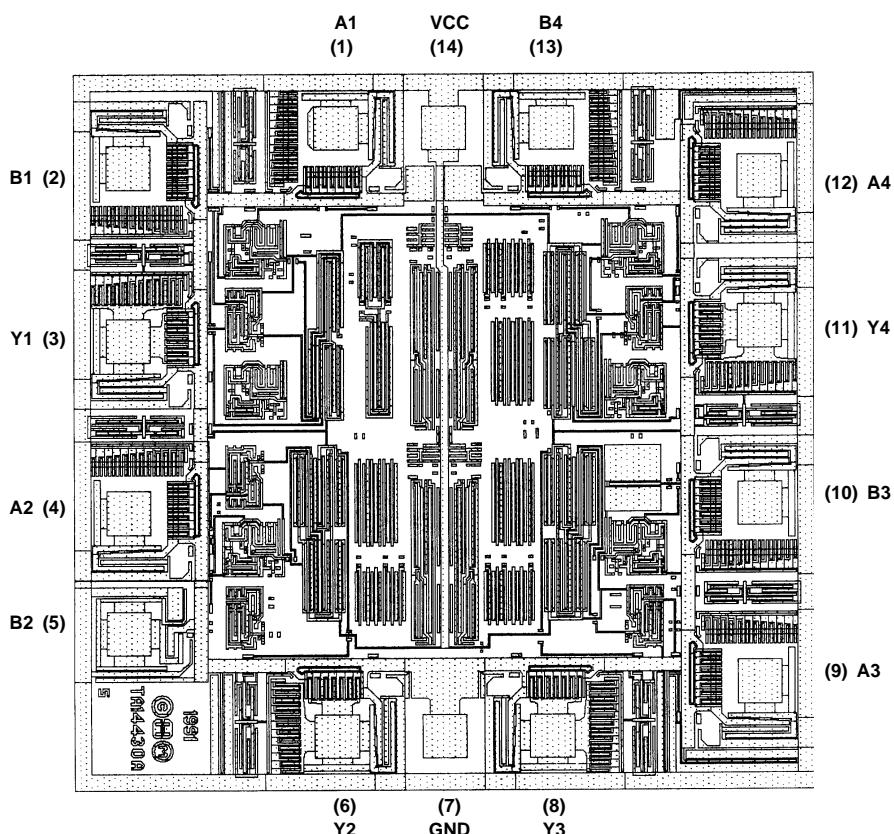
$<2.0 \times 10^5 \text{A/cm}^2$

BOND PAD SIZE:

$100\mu\text{m} \times 100\mu\text{m}$
4 mils x 4 mils

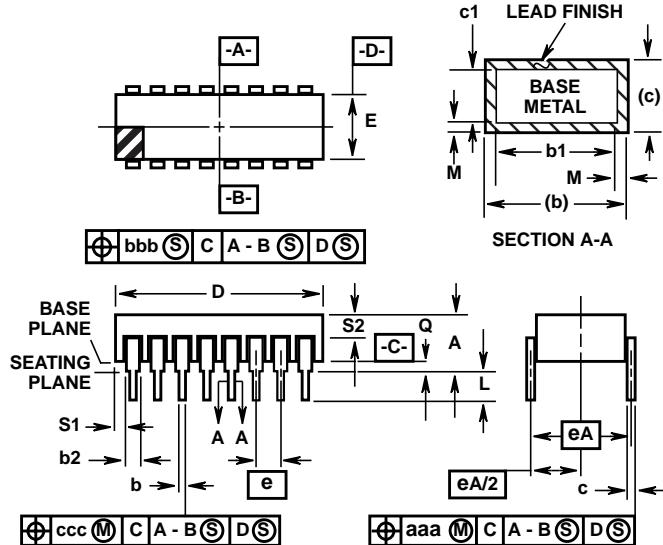
Metallization Mask Layout

HCTS08MS



HCTS08MS

Packaging



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

**D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

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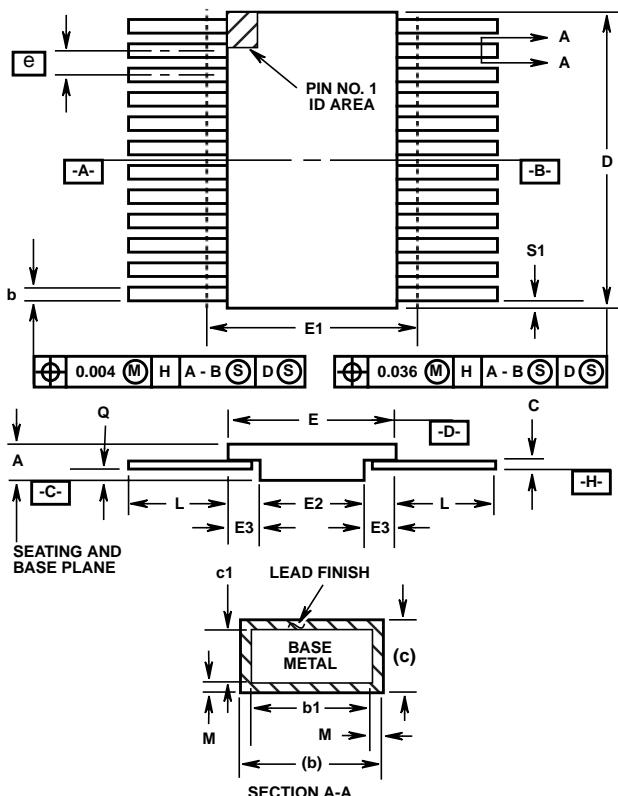
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Packaging (Continued)



K14.B

14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.003	0.009	0.08	0.23	-
c1	0.003	0.007	0.08	0.18	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.010	0.020	0.25	0.51	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension K) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH