

HD14013B

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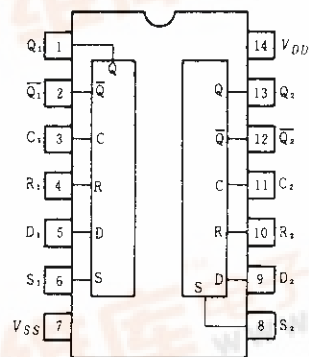
Dual D-type Flip Flop

The HD14013B dual type D flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\bar{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle Applications

FEATURES

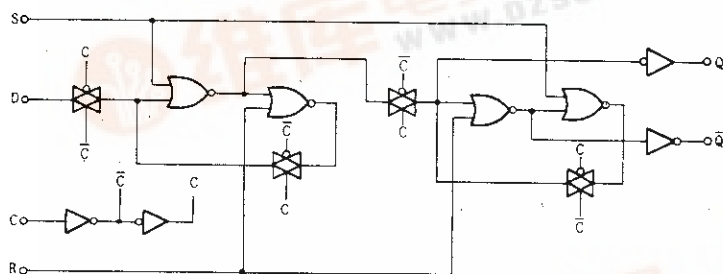
- Static Operation
- Quiescent Current = 2nA/pkg typ @5V
- Supply Voltage Range = 3 to 18V
- Toggle Rate = 4MHz typ @5V
- Logic Edge-clocked Flip-Flop Design ... Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Pin-for-pin Replacement for CD4013B and MC14013B

PIN ARRANGEMENT



(Top View)

LOGIC DIAGRAM (1/2)



TRUTH TABLE

Inputs				Outputs	
Clock*	Data	Reset	Set	Q	$\bar{Q}$
	0	0	0	0	1
	1	0	0	1	0
	x	0	0	Q	$\bar{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

x : Don't Care

* : Level Change

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	$V_{DD}(V)$	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	V_{OL}	5.0	$V_{in} = V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in} = 0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out} = 4.5$ or 0.5 V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out} = 9.0$ or 1.0 V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out} = 13.5$ or 1.5 V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out} = 0.5$ or 4.5 V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out} = 1.0$ or 9.0 V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out} = 1.5$ or 13.5 V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH} = 2.5$ V	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	$V_{OH} = 4.6$ V	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	$V_{OH} = 9.5$ V	-0.5	—	-0.4	-0.9	—	-0.3	—	
		15	$V_{OH} = 13.5$ V	-1.4	—	-1.2	-3.5	—	-1.0	—	
	I_{OL}	5.0	$V_{OL} = 0.4$ V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL} = 0.5$ V	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL} = 1.5$ V	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	± 0.1	—	± 0.00001	± 0.3	—	± 1.0	μA
Input Capacitance	C_{in}		$V_{in} = 0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	4.0	—	0.002	4.0	—	30	μA
		10		—	8.0	—	0.004	8.0	—	60	
		15		—	16	—	0.006	16	—	120	
Total Supply Current*	I_T	5.0	Dynamic + I_{DD} , per Gate, $C_L = 50$ pF, $f = 1$ kHz	—	—	—	0.75	—	—	—	μA
		10		—	—	—	1.5	—	—	—	
		15		—	—	—	2.3	—	—	—	

* To calculate total supply current at frequency other than 1kHz.

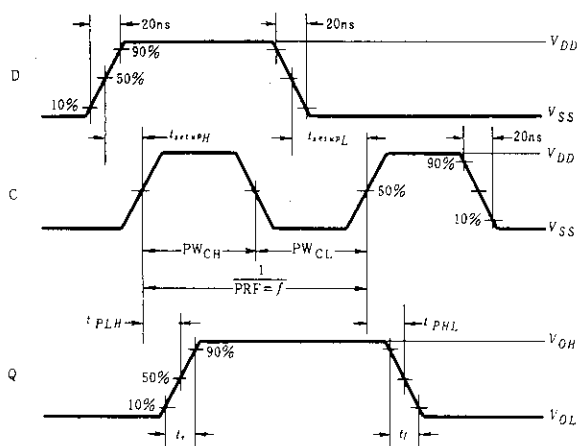
④ $V_{DD} = 5.0$ V $I_T = (0.75 \mu A/kHz) f + I_{DD}$ ⑤ $V_{DD} = 10$ V $I_T = (1.5 \mu A/kHz) f + I_{DD}$ ⑥ $V_{DD} = 15$ V $I_T = (2.3 \mu A/kHz) f + I_{DD}$

SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, $T_a=25^\circ\text{C}$)

Characteristic		Symbol	$V_{DD}(\text{V})$	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	360	ns
			10	—	90	180	
			15	—	65	130	
Output Fall Time		t_f	5.0	—	180	250	ns
			10	—	70	150	
			15	—	60	100	
Propagation Delay Time	Clock	$t_{PLH},$ t_{PHL}	5.0	—	175	350	ns
			10	—	80	200	
			15	—	70	150	
	Set		5.0	—	250	450	
			10	—	115	200	
			15	—	75	150	
	Reset		5.0	—	350	450	
			10	—	100	200	
			15	—	75	150	
Setup Time		$t_{\text{setup } H}$ $t_{\text{setup } L}$	5.0	40	20	—	ns
			10	20	10	—	
			15	15	7.5	—	
Clock Pulse Width		$PW_{CH},$ PW_{CL}	5.0	250	125	—	ns
			10	100	50	—	
			15	70	35	—	
Clock Pulse Frequency		PRF	5.0	—	4.0	2.0	MHz
			10	—	10	5.0	
			15	—	14	7.0	
Clock Pulse Rise and Fall Time		t_r, t_f	5.0	—	—	15	μs
			10	—	—	5.0	
			15	—	—	4.0	
Set and Reset Pulse Width		PW_S PW_R	5.0	250	125	—	ns
			10	100	50	—	
			15	70	35	—	

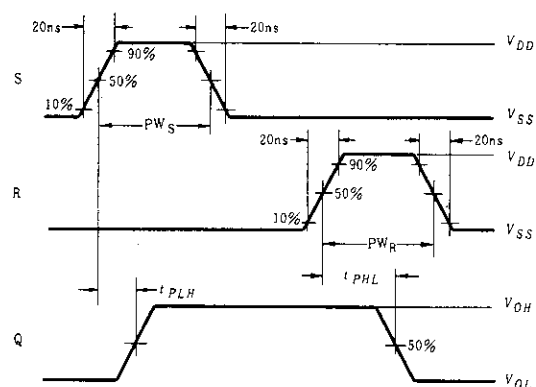
DYNAMIC SIGNAL WAVEFORMS

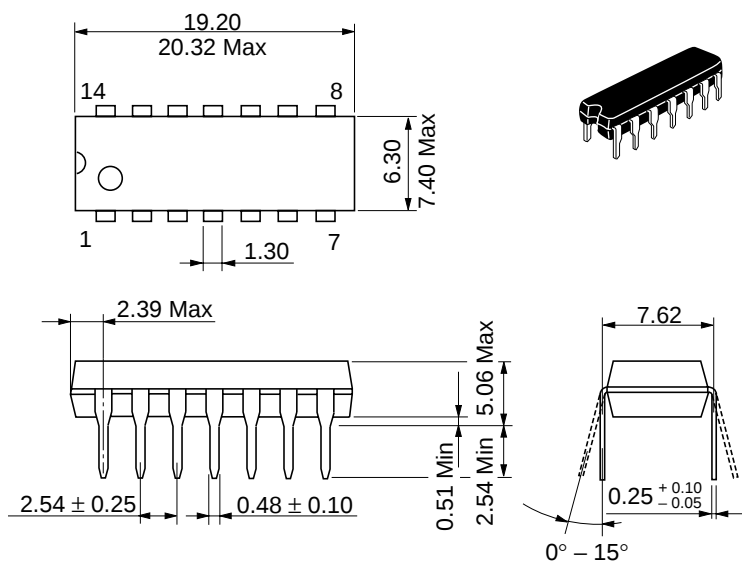
Data, Clock, and Output



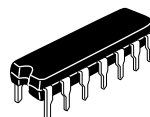
Note: Inputs R and S low.

Set, Reset, and Output

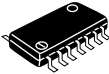
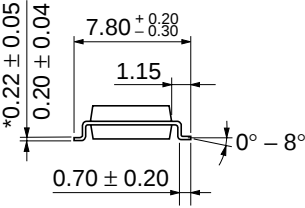
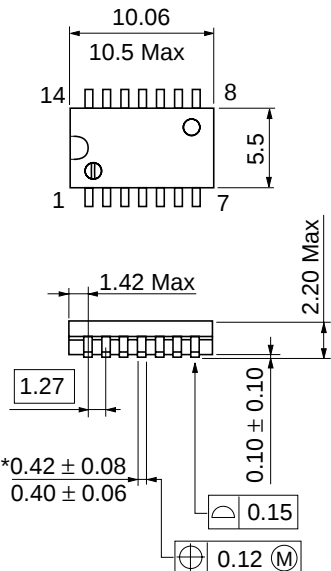




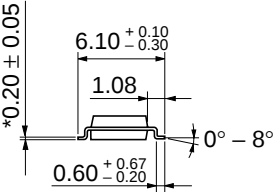
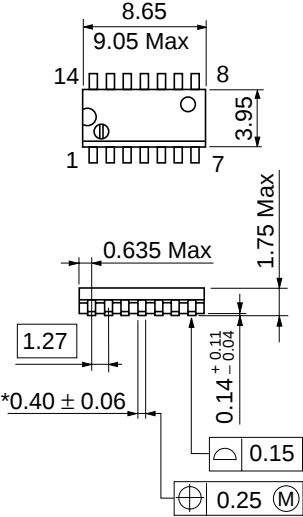
Unit: mm



Unit: mm



Unit: mm



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