# HD14014B

8-bit Static Shift Register

The HD14014B 8-bit shift register finds primary use in parallel-to-serial data conversion, synchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

■ FEATURES

Quiescent Current = 5nA/pkg typ @5V
Full Static Operation from DC to 7MHz
Supply Voltage Range = 3 to 18V
Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
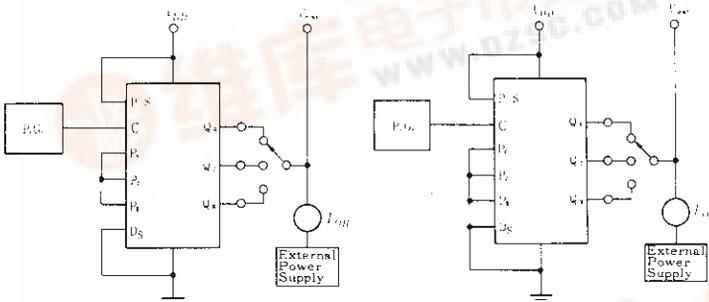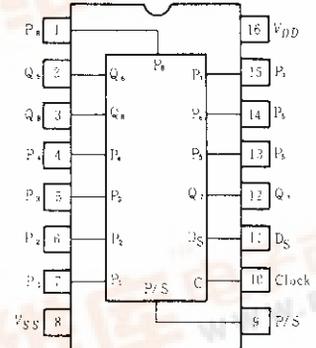Pin-for-Pin Replacement for CD4014B and MC14014B

■ LOGIC DIAGRAM
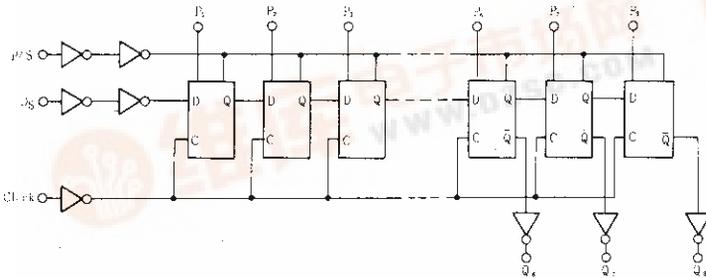
■ DC CHARACTERISTIC TEST CIRCUIT

● I$_{OH}$

● I$_{OL}$

■ PIN ARRANGEMENT

(Top View)

■ TRUTH TABLE

● Serial Operation

t	Clock	Ds	P/S
n	⤴	0	0
n+1	⤴	1	0
n+2	⤴	0	0
n+3	⤴	1	0
	⤵	×	0

Q$_6$ t=n+6	Q$_7$ t=n+7	Q$_8$ t=n+8
0	?	?
1	0	?
0	1	0
1	0	1
Q$_6$	Q$_7$	Q$_8$

● Parallel Operation

Clock	Ds	P/S	Dm	Qm*
⤴	×	1	0	0
⤴	×	1	1	1

* : Q$_6$, Q$_7$, & Q$_8$ are available externally
× : Don't Care

■ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40℃ min	−40℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or $0.5V$	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or $1.0V$	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or $1.5V$	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or $4.5V$	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or $9.0V$	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or $13.5V$	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5V$	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
		5.0	$V_{OH}=4.6V$	−0.2	—	−0.16	−0.36	—	−0.12	—	
		10	$V_{OH}=9.5V$	−0.5	—	−0.4	−0.9	—	−0.3	—	
		15	$V_{OH}=13.5V$	−1.4	—	−1.2	−3.5	—	−1.0	—	
	I_{OL}	5.0	$V_{OL}=0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5V$	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5V$	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}		$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I_T	5.0	Dynamic+I_{DD}, per Gate, $C_L=50pF, f=1$ kHz	—	—	—	0.76	—	—	—	μA
		10		—	—	—	1.51	—	—	—	
		15		—	—	—	2.27	—	—	—	

* To calculate total supply current at frequency other than 1kHz.
(@$V_{DD}=5.0V$ $I_T=(0.75μA/kHz)f+I_{DD}$. (@$V_{DD}=10V$ $I_T=(1.50μA/kHz)f+I_{DD}$, (@$V_{DD}=15V$ $I_T=(2.25μA/kHz)f+I_{DD}$

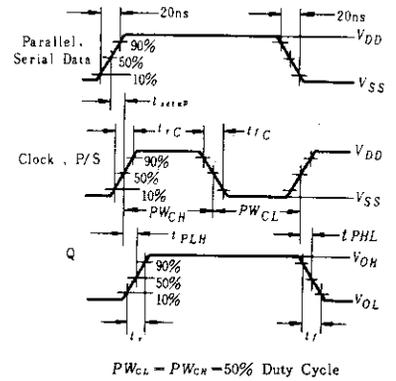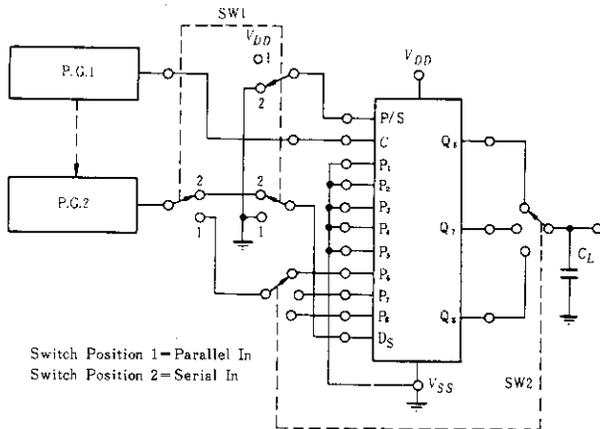# ■POWER DISSIPATION TEST CIRCUIT AND WAVEFORM
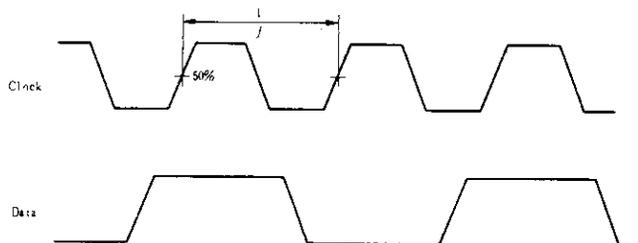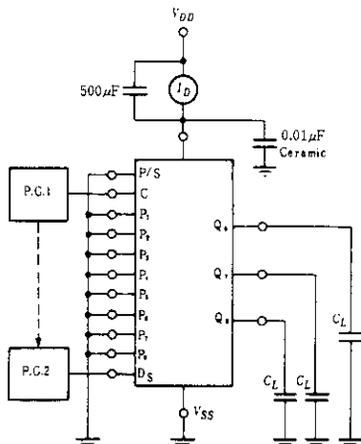
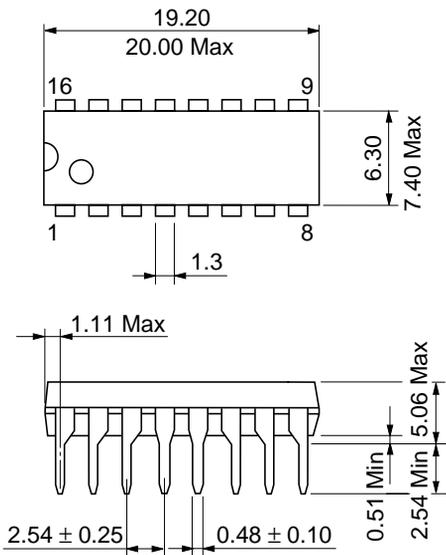## ■ SWITCHING CHARACTERISTICS $(C_L=50\text{pF}, Ta=25°\text{C})$

Characteristic	Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time	t_r	5.0	—	180	400	ns
		10	—	90	200	
		15	—	65	160	
Output Fall Time	t_f	5.0	—	100	200	ns
		10	—	50	100	
		15	—	37	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	—	400	1000	ns
		10	—	170	400	
		15	—	115	265	
Clock Pulse Width	PW_C	5.0	500	150	—	ns
		10	200	75	—	
		15	150	40	—	
Clock Frequency	f_C	5.0	—	3.0	1.0	MHz
		10	—	6.0	2.5	
		15	—	8.0	3.0	
Parallel/Serial Control Pulse Width	PW(P/S)	5.0	500	150	—	ns
		10	200	75	—	
		15	150	40	—	
Setup Time	t_{setup}	5.0	500	150	—	ns
		10	100	50	—	
		15	80	30	—	
Input Clock Rise Time	t_{rc}	5.0	—	—	15	μs
		10	—	—	15	
		15	—	—	15	

■ SWITCHING TIME TEST CIRCUIT

Switch Position 1─Parallel In
Switch Position 2─Serial In

$PW_{CL} - PW_{CH} - 50\%$ Duty Cycle

Unit: mm

19.20
20.00 Max

16   9

6.30
7.40 Max

1   8

1.3

1.11 Max

5.06 Max
0.51 Min
2.54 Min

2.54 ± 0.25   0.48 ± 0.10

7.62

0.25 $^{+0.13}_{-0.05}$

0° − 15°
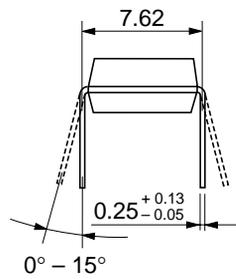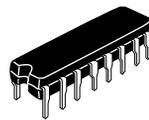
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