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■ PIN ARRANGEMENT

(Top View)

■ TRUTH TABLE

- | Clock | Reset | Outputs State |
|---|-------|-----------------------|
|  | 0 | No Change |
|  | 0 | Advance to next state |
| × | 1 | All Outputs are low |

× : Don't Care

The circuit diagram shows a synchronous counter implemented with D flip-flops. A common clock signal is connected to the clock input of every flip-flop. The first flip-flop has its Q output connected to its D input. Its R input is connected to the output of an AND gate, which takes the inverted Q outputs of all other flip-flops as inputs. This configuration ensures that the counter resets whenever it reaches a state where all bits are 1. The Q outputs of the flip-flops are labeled Q₀, Q₁, Q₂, ..., Q_{n-1}.



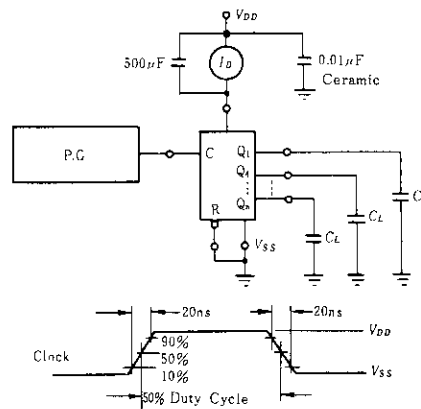
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit
			min	max	min	typ	max	min	max	
Output Voltage	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	-0.5	—	-0.4	-0.9	—	-0.3	—	
		15	-1.4	—	-1.2	-3.5	—	-1.0	—	
	I_{OL}	5.0	0.52	—	0.44	0.88	—	0.36	—	mA
		10	1.3	—	1.1	2.25	—	0.9	—	
		15	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}		—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	—	20	—	0.005	20	—	150	μA
		10	—	40	—	0.010	40	—	300	
		15	—	80	—	0.015	80	—	600	
Total Supply Current*	I_T	5.0	—	—	—	0.43	—	—	—	μA
		10	—	—	—	0.86	—	—	—	
		15	—	—	—	1.45	—	—	—	

* To calculate total supply current at frequency other than 1kHz.

@ $V_{DD}=5.0V$ $I_T=0.42\mu A/kHz \cdot f + I_{DD}$, @ $V_{DD}=10V$ $I_T=0.85\mu A/kHz \cdot f + I_{DD}$, @ $V_{DD}=15V$ $I_T=1.43\mu A/kHz \cdot f + I_{DD}$

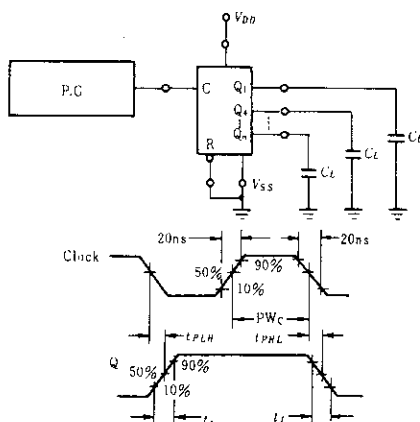
POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

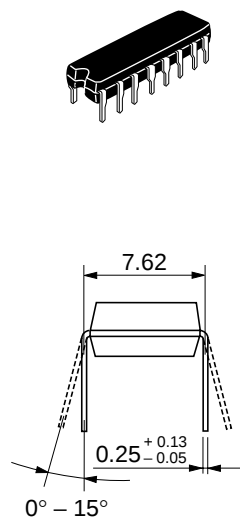
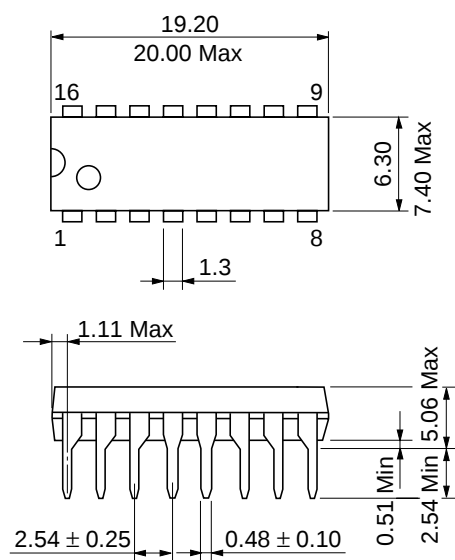


SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, $T_a=25^\circ\text{C}$)

Characteristic		Symbol	$V_{DD}(\text{V})$	min	typ	max	Unit
Output Rise Time	t_r		5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time	t_f		5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	Clock to Q_1	t_{PLH}	5.0	—	400	750	ns
			10	—	170	300	
			15	—	120	230	
	Clock to Q_{1+}	t_{PHL}	5.0	—	2.8	8.4	μs
			10	—	1.0	3.0	
			15	—	0.6	2.5	
	Reset to Q_+	t_{PHL}	5.0	—	595	3500	ns
			10	—	230	900	
			15	—	180	680	
Clock Pulse Width	PW_C		5.0	500	140	—	ns
			10	165	55	—	
			15	125	38	—	
Clock Pulse Frequency	PRF		5.0	—	3.5	1.0	MHz
			10	—	9.0	3.0	
			15	—	13	4.0	
Clock Pulse Rise and Fall Time	t_r, t_f		5.0	No Limit			
			10				
			15				
Reset Pulse Width	PW_R		5.0	3000	320	—	ns
			10	550	120	—	
			15	420	80	—	

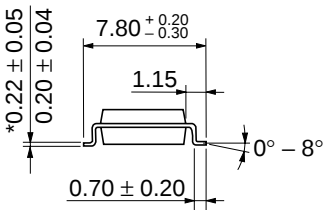
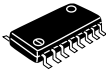
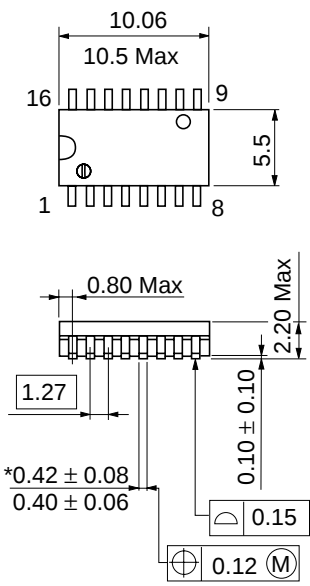
SWITCHING TIME TEST CIRCUIT



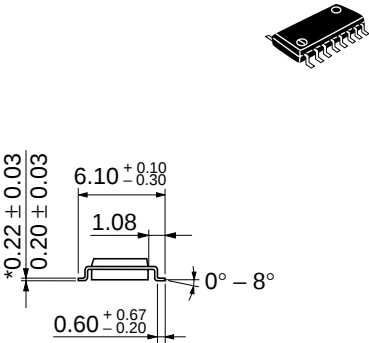
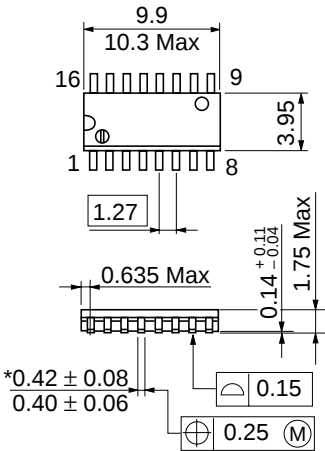


Unit: mm

Unit: mm



Unit: mm



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