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出货

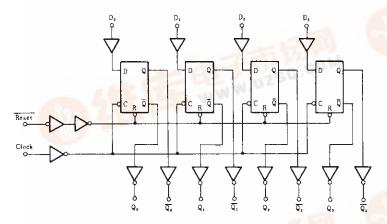
Quadruple D-type Flip Flop

HD141758

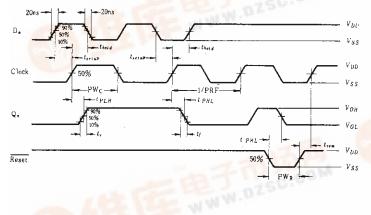
The HD14175B is quad type D flip-flop. Each of the four flipflops is positive-edge triggered by a common clock input (C). An active-low reset input (R) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and \overline{Q}). This device may be used as shift register elements or as type T flip-flops for counter and toggle applications.

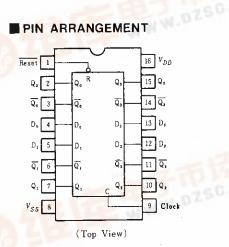
- FEATURES
- Supply Voltage Range = 3 to 18V •
- Output Compatible with One Low-power Schottky TTL Load
- Functional Equivalent to TTL74175

BLOCK DIAGRAM



DYNAMIC SIGNAL WAVEFORMS





TRUTH TABLE

Inputs			Output		
Clock	Data	Reset	Q	Q	
	0	1	0	1	
	1	1 ·	1	0	
<u> </u>	×	1	Q	Q	
×	×	0	0	1	

Don't Care



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol		Test Conditions	- 40°C			25°C		85°C			
Gnaracteristic (Sy		$V_{DD}(\mathbf{V})$	Test Conditions	min	max	min	typ	max	min	max	Unit	
Output Voltage		5.0			0.05		0	0.05	-	0.05	v	
	Vol	10	$V_{in} = V_{DD}$ or 0		0.05	_	0	0.05	_	0.05		
		15		-	0. 0 5	-	0	0.05	-	0.05		
		5.0		4.95	_	4.95	5.0	_	4.95	-	v	
	Von	10	$V_{in} = 0$ or V_{DD}	9.95	_	9.95	10		9.95	-		
		15		14.95		14.95	15	_	14.95	-		
		5.0	$V_{out} = 4.5 \text{ or } 0.5 \text{V}$		1.5	-	2.25	1.5	-	1.5	†	
14	VIL	10	$V_{out} = 9.0 \text{ or } 1.0 \text{V}$	-	3.0	-	4.50	3.0	-	3.0	v	
Input Voltage		15	Vout = 13.5 or 1.5V	-	4.0	_	6.75	4.0	-	4.0		
Input voltage		5.0	$V_{out} = 0.5 \text{ or } 4.5 \text{V}$	3.5	_	3.5	2.75	_	3.5	_	v	
	ViH	10	$V_{out} = 1.0 \text{ or } 9.0 \text{V}$	7.0		7.0	5.50	_	7.0	-		
		15	$V_{out} = 1.5 \text{ or } 13.5 \text{V}$	11.0	_	11.0	8.25		11.0	_		
		5.0	$V_{OH} = 2.5 \mathrm{V}$	-2.5		-2.1	-4.2	-	-1.7			
	Іон	5.0	$V_{OH} = 4.6 \text{ V}$	-0.52	-	-0.44	-0.88	-	-0.36	-		
Output Drive Current	10H	10	$V_{OH} = 9.5 V$	-1.3	_	-1.1	- 2.25		-0.9	_	mA	
		15	$V_{OH} = 13.5 \mathrm{V}$	-3.6	-	-3.0	-8.8		-2.4	-		
		5.0	$V_{OL} = 0.4 \text{V}$	0,52	_	0.44	0.88	_	0.36	-	mA	
	Ior	10	$V_{OL} = 0.5 V$	1.3	_	1.1	2.25		0.9	-		
		15	$V_{0L} = 1.5 V$	3.6		3.0	8.8	_	2.4			
Input Current	Iin	15		_	±0.3		±0.00001	±0.3	_	±1.0	μA	
Input Capacitance	Cin	—	$V_{in} = 0$	-	_	_	5.0	7.5	-		pF	
Quiescent Current		5.0	7 6:1	-	20	_	0.0005	20	-	150	μA	
	IDD	10	Zero Signal, per Package	-	40		0.0010	40	-	300		
		15	her rackaße	_	80	-	0.0015	80	_	600		
Total Supply Current*		5.0	Dynamic $+I_{DD}$, $C_L = 50 \text{pF}$	-	-		1.7	_	· _	_	μA	
	Iτ	10	$f=1\mathrm{kHz}$	-	-		3.4		-	_		
		15	per Gate	-	-	-	5.0		_	-		

* To calculate total supply current at frequency other than 1kHz.

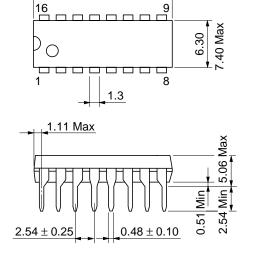
 $\Psi V_{DD} = 5.0 V \quad J_T = (1.7 \,\mu A/kH_2) f + I_{DD} \qquad \Psi V_{DD} = 10 V \quad J_T = (3.4 \,\mu A/kH_2) f + I_{DD} \qquad \Psi V_{DD} = 15 V \quad J_T = (5.0 \,\mu A/kH_2) f + I_{DD}$

HD14175B ------

SWITCHING CHARACTERICS ($C_L = 50 \text{ pF}, Ta = 25^{\circ}\text{C}$)

Characteristic		Symbol	$V_{DD}(\mathbf{V})$	min	typ	max	Unit	
Output Rise and Fall Time		tr,tj	5.0		100	200	ns	
			10	_	50	100		
			15		40	80		
Propagation Delay Time	Clock	tplh. tphl	5.0	-	220	420	ns	
			10		90	170		
			15	-	70	130		
		t phl	5.0	-	325	650		
	Reset		10		130	260		
* *			15	-	100	200		
Clock Pulse Width			5.0	250	110		ns	
		PWc	10	100	45	-		
			15	75	35	_		
Reset Pulse Width		PW _R	5.0	200	100	-	ns	
			10	80	40	—		
			15	60	30	-		
Clock Frequency		PRF	5.0	-	4.5	2.0	MHz	
			10	_	11	5.0		
			15	-	14	6.5	1	
Clock Pulse Rise and Fall Time		tr, tj	5.0	-	-	15		
			10	-	-	15	μs	
<u></u>			15 — — 1		15	7		
Setup Time			5.0	120	60	_	ns	
		tsetup	10	50	25	-		
			15	40	20]	
Hold Time		thatd	5.0	80	40		ns	
			10	40	20			
			15	30	15	_		
Reset Removal Time			5.0	250	125	_		
		trem	10	100	50	-	ns	
			15	80	40	-		

 $\boldsymbol{\ast}$ The reset signal must be high prior to a positive-going transition of the clock.



19.20 20.00 Max



7.62

 $0.25^{+0.13}_{-0.05}$

0° − 15°

Unit: mm

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