HD14194B

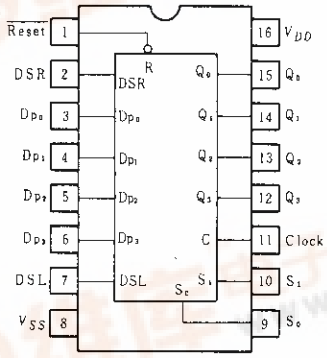
4-bit Bidirectional Universal Shift Register

The HD14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous $\overline{\text{Reset}}$ input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When $\overline{\text{Reset}}$ is at a logic 1 level, the two mode control inputs, S_0 and S_1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

■ FEATURES

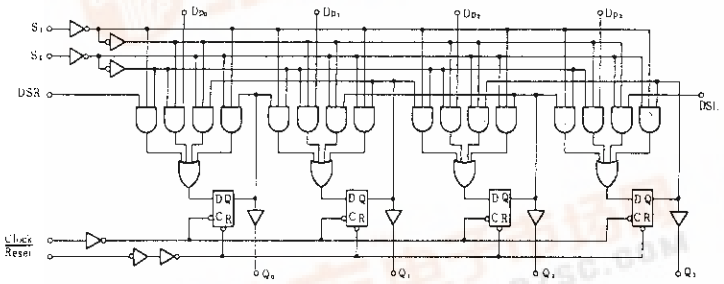
- Quiescent Current = 5nA/pkg typ. @5V
- Typical Shift Frequency = 9MHz @10V
- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode
- Functional Pin-for-Pin Equivalent of 74194

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Operating Mode	Inputs ($\overline{\text{Reset}}$ = 1)					Outputs (@ t_{n+1})			
	S_1	S_0	DSR	DSL	D_{P0-3}	Q_0	Q_1	Q_2	Q_3
Hold	0	0	×	×	×	Q_0	Q_1	Q_2	Q_3
Shift Left	1	0	×	0	×	Q_1	Q_2	Q_3	0
	1	0	×	1	×	Q_1	Q_2	Q_3	1
Shift Right	0	1	0	×	×	0	Q_0	Q_1	Q_2
	0	1	1	×	×	1	Q_0	Q_1	Q_2
Parallel	1	1	×	×	0	0	0	0	0
	1	1	×	×	1	1	1	1	1

× = Don't Care

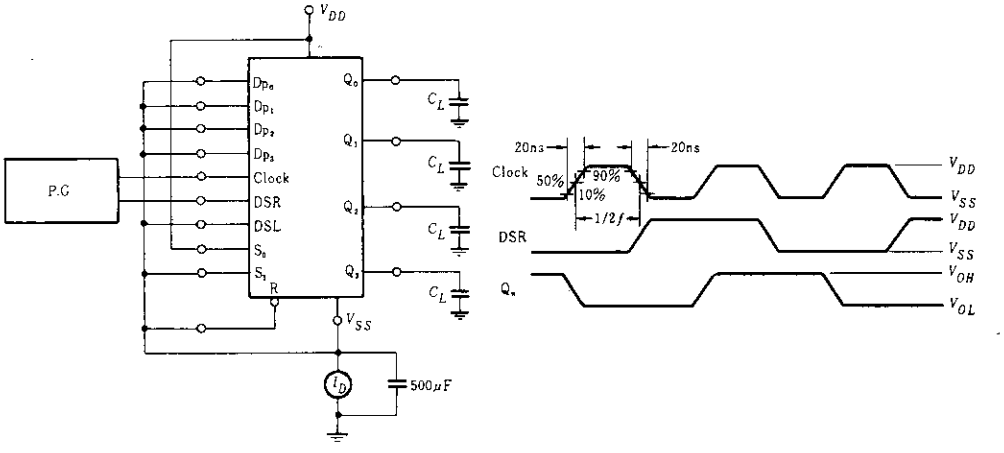
t_{n+1} = State after the next positive-going transition of the clock.

■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40℃ min	−40℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	−	0.05	−	0	0.05	−	0.05	V
		10		−	0.05	−	0	0.05	−	0.05	
		15		−	0.05	−	0	0.05	−	0.05	
	V_{OH}	5.0	V_{in}= 0 or V_{DD}	4.95	−	4.95	5.0	−	4.95	−	V
		10		9.95	−	9.95	10	−	9.95	−	
		15		14.95	−	14.95	15	−	14.95	−	
Input Voltage	V_{IL}	5.0	V_{out}= 4.5 or 0.5V	−	1.5	−	2.25	1.5	−	1.5	V
		10	V_{out}= 9.0 or 1.0V	−	3.0	−	4.50	3.0	−	3.0	
		15	V_{out}=13.5 or 1.5V	−	4.0	−	6.75	4.0	−	4.0	
	V_{IH}	5.0	V_{out}= 0.5 or 4.5V	3.5	−	3.5	2.75	−	3.5	−	V
		10	V_{out}= 1.0 or 9.0V	7.0	−	7.0	5.50	−	7.0	−	
		15	V_{out}= 1.5 or 13.5V	11.0	−	11.0	8.25	−	11.0	−	
Output Drive Current	I_{OH}	5.0	V_{OH}= 2.5V	−2.5	−	−2.1	−4.2	−	−1.7	−	mA
		5.0	V_{OH}= 4.6V	−0.52	−	−0.44	−0.88	−	−0.36	−	
		10	V_{OH}= 9.5V	−1.3	−	−1.1	−2.25	−	−0.9	−	
		15	V_{OH}=13.5V	−3.6	−	−3.0	−8.8	−	−2.4	−	
	I_{OL}	5.0	V_{OL}= 0.4V	0.52	−	0.44	0.88	−	0.36	−	mA
		10	V_{OL}= 0.5V	1.3	−	1.1	2.25	−	0.9	−	
		15	V_{OL}= 1.5V	3.6	−	3.0	8.8	−	2.4	−	
Input Current	I_{in}	15		−	±0.3	−	±0.00001	±0.3	−	±1.0	μA
Input Capacitance	C_{in}	−	V_{in}= 0	−	−	−	5.0	7.5	−	−	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	−	20	−	0.005	20	−	150	μA
		10		−	40	−	0.010	40	−	300	
		15		−	80	−	0.015	80	−	600	
Total Supply Current*	I_T	5.0	Dynamic + I_{DD}, C_L=50pF, f=1kHz per Gate	−	−	−	0.95	−	−	−	μA
		10		−	−	−	1.9	−	−	−	
		15		−	−	−	2.9	−	−	−	

* To calculate total supply current at frequency other than 1kHz.
@ V_{DD}=5.0V $I_T=(0.95\mu A/kHz)f+I_{DD}$ @ V_{DD}=10V $I_T=(1.9\mu A/kHz)f+I_{DD}$ @ V_{DD}=15V $I_T=(2.9\mu A/kHz)f+I_{DD}$

■ POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



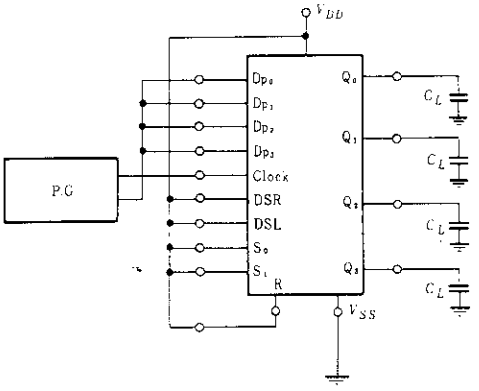
■ SWITCHING CHARACTERICS (C_L=50pF, Ta=25°C)

Characteristic		Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise and Fall Time		t_r, t_f	5.0	–	100	200	ns
			10	–	50	100	
			15	–	40	80	
Propagation Delay Time	Clock	t_{PLH}, t_{PHL}	5.0	–	275	550	ns
			10	–	110	220	
			15	–	85	170	
	Reset	t_{PHL}	5.0	–	350	700	ns
			10	–	140	280	
			15	–	110	220	
Clock Pulse Width		PW_C	5.0	280	140	–	ns
			10	110	55	–	
			15	85	40	–	
Reset Pulse Width		PW_R	5.0	180	90	–	ns
			10	70	35	–	
			15	50	26	–	
Clock Frequency		PRF	5.0	–	3.6	1.8	MHz
			10	–	9.0	4.5	
			15	–	12	6.0	
Clock Pulse Rise and Fall Time		t_r, t_f	5.0	No Limit			
			10				
			15				
Setup Time	Data-to-Clock	t_{setup}	5.0	10	−8.0	–	ns
			10	20	0	–	
			15	40	9.0	–	
	Mode Control -to-Clock		5.0	200	100	–	
			10	75	36	–	
			15	55	27	–	
Hold Time	Data-to-Clock	t_{hold}	5.0	180	90	–	ns
			10	50	25	–	
			15	35	10	–	
	Mode Control -to-Clock		5.0	0	− 40	–	
			10	0	− 27	–	
			15	0	− 20	–	
Reset Removal Time*		t_{rem}	5.0	300	150	–	ns
			10	110	55	–	
			15	80	40	–	

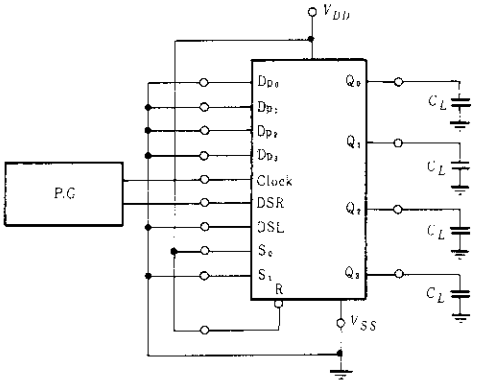
* The reset signal must be high prior to a positive-going transition of the clock.

■ DC CHARACTERISTIC TEST CIRCUIT

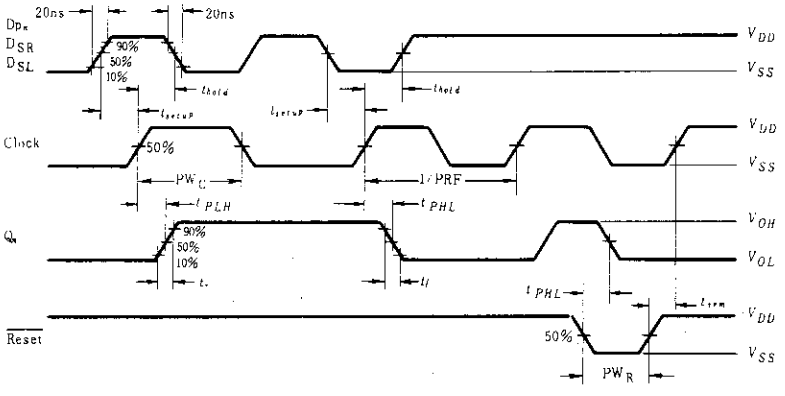
● Parallel Load



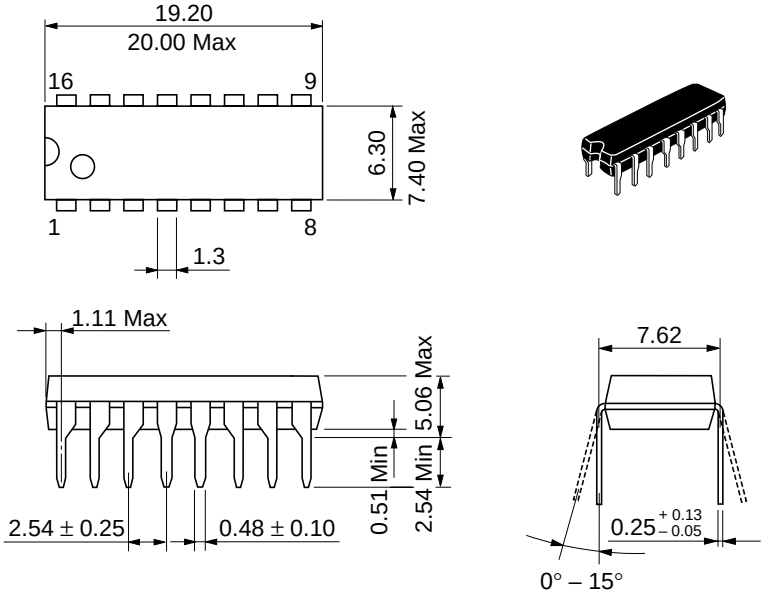
● Serial Load



Interchange DSR with DSL and S_0 with S_1 for testing shift left.



Unit: mm


19.20
20.00 Max
16
9
6.30
7.40 Max
1
8
1.3
1.11 Max
5.06 Max
0.51 Min
2.54 Min
2.54 ± 0.25
0.48 ± 0.10
7.62
0.25 + 0.13 − 0.05
0° – 15°

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