出货

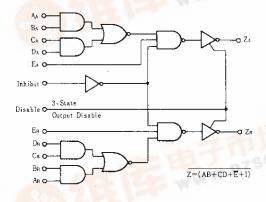
Dual 2-wide 2-input Expandable AND-OR-INVERT Gate

The HD14506B is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

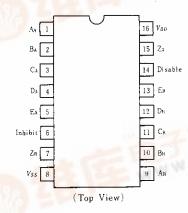
FEATURES

- Quiescent Current = 2nA/pkg typ. @5V
- 3-state Output
- · Separate Inhibit Line
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

LOGIC DIAGRAM



■ PIN ARRANGEMENT

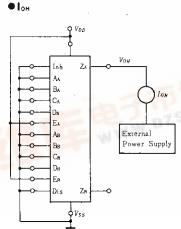


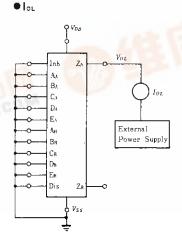
TRUTH TABLE

A	В	С	D	Е	Inhibit	Disable	Z
0	0	0	0	1	0	0	1
0	×	0	×	1	0	0	1
0	×	×	0	1	0	0	1
×	0	0	×	1	0	0	1
×	0	×	0	1	0	0	1
1	1	×	×	×	×	0	0
×	×	1	1	×	×	0	0
×	X	×	×	0	×	0	0
×	×	×	X	×	1	0	0
×	×	×	×	×	×	1	High Impedance

x=Don't Care

IDC CHARACTERISTIC TEST CIRCUIT





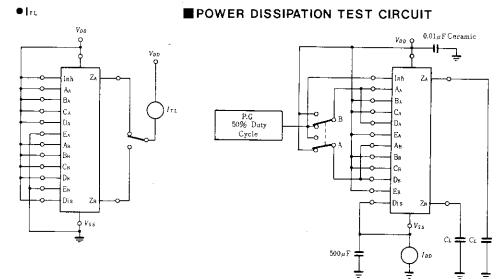


■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbo	Test Conditions	40°C			25°C			85° C		
	Symbol	$V_{DD}(\mathbf{V})$) rest conditions	min	max	mín	typ	max	min	max	Unit
	İ	5.0	$V_{in} = V_{DD}$ or 0		0.05		0	0.05	_	0.05	v
	Vol	10			0.05	-	0	0.05	_	0.05	
Output Voltage		15			0.05	_	0	0.05		0.05	
·		5.0		4.95	-	4.95	5.0		4.95	_	V
	V_{OH}	10	$V_{in} = 0$ or V_{DD}	9.95		9.95	10	_	9.95		
		15		14.95	_	14.95	15	-	14.95		
	:	5.0	$V_{out} = 4.5 \text{ or } 0.5 \text{V}$		1.5	_	2.25	1.5	_	1.5	v
15	V_{IL}	10	$V_{out} = 9.0 \text{ or } 1.0 \text{V}$	_	3.0	_	4.50	3.0	_	3.0	
Input Voltage		15	$V_{\rm out} = 13.5 \text{ or } 1.5 \text{ V}$		4.0	_	6.75	4.0		4.0	
Input voitage		5.0	$V_{out} = 0.5 \text{ or } 4.5 \text{V}$	3.5	_	3.5	2.75	_ <u>-</u>	3.5	_	v
	V_{IH}	10	$V_{out} = 1.0$ or $9.0\mathrm{V}$	7.0	_	7.0	5.50	_	7.0	_	
		15	$V_{\text{out}} = 1.5 \text{ or } 13.5 \text{V}$	11.0	i -	11.0	8.25	_	11.0	_	
		5.0	$V_{OH} = 2.5 \text{V}$	-1.0		-0.8	-1.7	_	-0.6	_	mA
	I_{OH}	5.0	$V_{OH} = 4.6 \text{V}$	-0.2		-0.16	-0.36	_	-0.12	_	
	10#	10	$V_{OH} = 9.5 \mathrm{V}$	-0.5	_	-0.4	-0.9	_	-0.3		
Output Drive Current		15	$V_{OH} = 13.5 \text{V}$	-1.4	_	-1.2	-3.5	_	-1.0	_	
		5.0	$V_{oL} = 0.4 \text{V}$	0.52	_	0.44	0.88	_	0.36	_	mA
	InL	10	$V_{OL} = 0.5 \text{V}$	1.3	_	1.1	2.25		0.9	_	
		15	$V_{oL} = 1.5 \text{V}$	3.6		3.0	8.8		2,4	_	
Input Current	I_{in}	15		-	±0.3	_	±0.00001	±0.3	_	±1.0	μΑ
Input Capacitance	C.,		$V_{in} = 0$	T -		_	5.0	7.5	_	_	pF
		5.0			4.0	_	0.002	4.0	- 1	30	μΑ
Quiescent Current	I_{DD}	10	Zero Signal, Per Package	_	8.0		0.004	8.0	_	60	
		15		_	16	_	0.006	16	_	120	
· -		5.0	Dynamic $+I_{DD}$,				0.6				μΑ
Total Supply Current*	I_T	10	Per Gate	_		_	1.1	_	_		
	Ì	15	$C_L = 50 \mathrm{pF}, f = 1 \mathrm{kHz}$	_			1.7	-	-		
Three-State Output Leakage Current	I_{TL}	15		! -	±1.0		±0.00001	±1.0		±7.5	μΑ

^{*} To calculate total supply current at frequency other than 1kHz. $@V_{DB} = 5.0 \text{V} \ I_T = (0.6 \mu \text{A/kHz}) \ f + I_{DB}, \ @V_{DB} = 10 \text{V} \ I_T = (1.1 \mu \text{A/kHz}) \ f + I_{DB}, \ @V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V} \ I_T = (1.7 \mu \text{A/kHz}) \ f + I_{DB}, \ eq V_{DB} = 15 \text{V}$

■DC CHARACTERISTIC TEST CIRCUIT

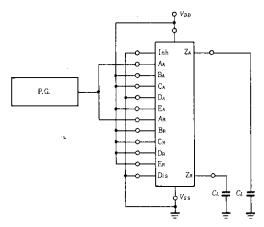


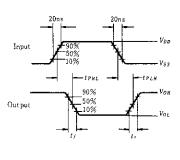
■SWITCHING CHARACTERISTICS (C_L =50pF, Ta=25°C)

Characteri	stic	Symbol	$V_{DD}(V)$	min	typ	max	Unit
			5.0	_	180	400	
Output Rise Time	•	t,	10	_	90	200	ns
		15	_	65	160	1	
			5.0	_	100	200	ns
Output Fall Time		<i>t,</i>	10		50	100	
			15	_	37	80	
		tplH	5.0		295	580	ns
<u>.</u>			10	_	110	225	
	Data		15	_	75	180	
	Data	t_{PHL}	5.0		270	480	ns
			10	-	95	175	
			15	_	65	140	
		t_{PLH}	5.0	_	180	430	ns
			10	-	75	160	
Propagation Delay Time	Expand		15	_	50	125	
Topagation Delay Time	Ехрани	tpHL	5.0		200	330	ns
			10	-	80	110	
			15		55	90	
		t _{PLH}	5.0	_	220	500	ns
			10	_	100	225	
	Tabibia		15	_	65	160	
	Inhibit	t _{PHL}	5.0		230	400	ns
			10	-	95	175	
			15		60	150	
			5.0	_	60	150	
		tuz	10	_	45	110	ns
Output Disable Time			15	_	35	90	
weker presents Time			5.0		90	225	
	tuz	10	_	55	140	ns	
		1	15		40	100	
			5.0	_	110	300	
		t_{ZH}	10	-	50	125	ns
Output Enable Time			15	_	40	100	
			5.0		170	425	
		t_{ZL}	10		70	175	ns
			15	_	50	125	

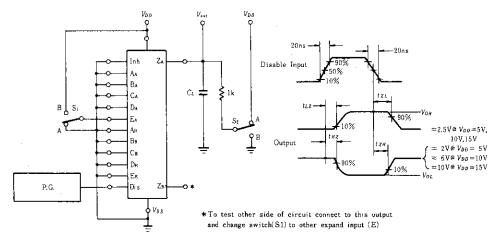
■ SWITCHING TIME TEST CIRCUIT

●telm, teml



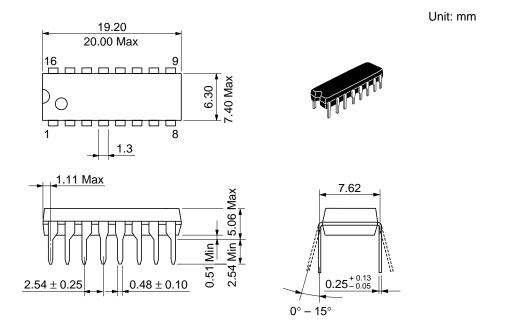


● tHz, tLz, tzH, tzL



Switch Positions

Test	S ₁	S2
tız	A	A
l H Z	В	8
121	A	A
4 Z H	8	В



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