HD145188, HD145

出货

Dual BCD Up Counter·······HD14518B Dual Binary Up Counter HD14520B

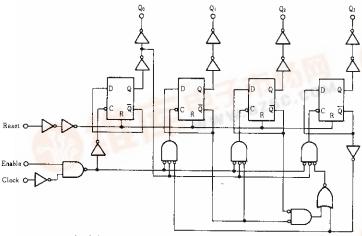
The HD14518B dual BCD counter and the HD14520B dual binary counter consist of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flipflops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the HD14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

■ FEATURES

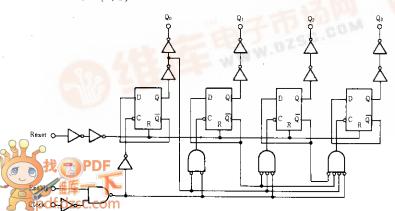
- Quiescent Current = 5nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-clocked Design ... Incremented on Positive Transition of Clock or Negative Transition of Enable
- 6MHz Counting Rate
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

LOGIC DIAGRAM

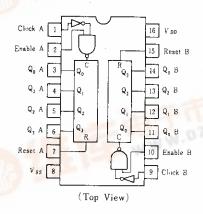
●HD14518B (1/2)



◆HD14520B (1/2)



PIN ARRANGEMENT



TRUTH TABLE

Clock	Enable	Reset	Action
	1	0	Increment Counter
0		0	Increment Counter
	×	0	No Change
×		0	No Change
	0	0	No Change
1		0	No Change
×	×	1	$Q_0 \sim Q_3 = 0$

x=Don't Care

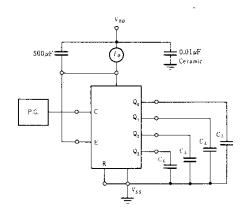
HD14518B, HD14520B-

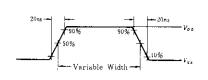
■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions		-40°C		25° C			85 °C		17_:4
Characteristic	Symbol	$V_{DD}(V_{\cdot})$	Test Committees	min	max	min	typ	max	min	max	Unit
Output Voltage 压		5.0			0.05	_	0	0.05		0.05	v
	. VoL	10	$V_{in} = V_{BD}$ or 0	_	0.05	_	0	0.05	_	0.05	
		15		_	0.05	_	0	0.05		0.05	
		5.0		4.95	_	4.95	5.0		4.95	_	v
	V _{OH}	10	$V_{\it in}\!=0$ or $V_{\it DD}$	9.95	-	9.95	10	-	9.95	-	
		15		14.95		14.95	15		14.95		
- 4	!	5.0	$V_{out} = 4.5 \text{ or } 0.5 \text{V}$	-	1.5	-	2.25	1.5	_	1.5	v
	V _{tL}	10	V _{out} = 9.0 or 1.0V		3.0	_	4.50	3.0	_	3.0	
1 1 17-1		15	5 V _{out} =13.5V or 1.5V		4.0	_	6.75	4.0	_	4.0	!
Input Voltage		5.0	$V_{out} = 0.5 \text{ or } 4.5 \text{V}$		_	3.5	2.75	-	3.5	_	
	V _{IH}	10	$V_{out} = 1.0 \text{ or } 9.0 \text{V}$	7.0	_	7.0	5.50	_	7.0	_	v
		15	V _{out} = 1.5 or 13.5V	11.0	-	11.0	8.25	-	11.0	_	
<u> </u>		5.0	$V_{OH} = 2.5 \text{V}$	-1.0	_	-0.8	-1.7	-	0.6	_	mA.
	,	5.0	V _{он} = 4.6V	-0.2		-0.16	-0.36		-0.12	_	
	Іон	10	V _{OH} = 9.5V	-0.5	-	-0.4	0.9	_	-0.3	_	
Output Drive Current		15	$V_{OH} = 13.5 \text{V}$	-1.4	_	-1.2	-3.5	_	-1.0		
	101	5.0	$V_{OL} = 0.4 \text{V}$	0.52	_	0.44	0.88		0.36	_	mA
		10	$V_{OL} = 0.5 \text{V}$	1.3	_	1.1	2.25	_	0.9	-	
		15	$V_{oi} = 1.5 \text{V}$		_	3.0	8.8	_	2.4		
Input Current	I_{in}	15	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	T -	±0.3	_	±0.00001	±0.3	_	±1.0	μА
Input Capacitance	Cin		$V_{in}=0$	-	-	_	5.0	7.5			рF
Quiescent Current		5.0	5 6 1	_	20	_	0.005	20	_	150	μA
	I_{DD}	10	Zero Signal,	_	40	-	0.010	40		300	
		15	per Package		80	-	0.015	80		600	
		5.0	Dynamic+Ina,	_	_	_	0.6	_	_		μΑ
Total Supply Current*	I_T	10	per Gate	_	_		1,2	-		_	
		15	$C_{L} = 50 \mathrm{pF}, f = 1 \mathrm{kHz}$	_	_		1.7	_			

^{*} To calculate total supply current at frequency other than 1kHz. $@V_{DO} = 5.0V$ $I_{\tau} = (0.6\,\mu\text{A/kHz}) f + I_{DO}$. $@V_{DO} = 10V$ $I_{\tau} = (1.2\,\mu\text{A/kHz}) f + I_{DO}$. $@V_{DO} = 15V$ $I_{\tau} = (1.7\,\mu\text{A/kHz}) f + I_{DO}$.

■POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



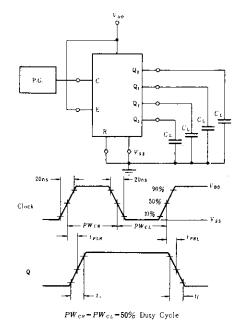


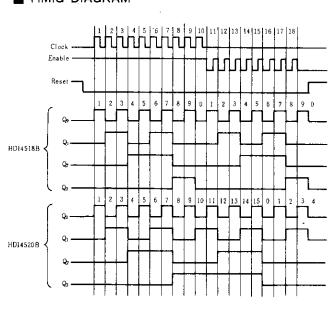
■SWITCHING CHARACTERISTICS ($C_L = 50 \text{pF}$, $Ta = 25 ^{\circ}\text{C}$)

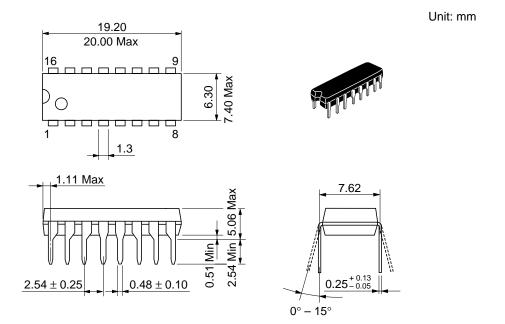
Characterist	ic	Symbol	$V_{DD}(V)$	min	typ	max	Unit	
Output Rise Time		t _r	5.0	_	180	360	<u> </u>	
			10	_	90	180	πs	
			15	_	65	130	7	
Output Fall Time.		tr	5.0	_ "	130	250	ns	
			10		50	100		
			15	_	40	80		
	Clock	t peh.	5.0		280	560	ns	
			10	_	115	230		
D			15		80	160		
Propagation Delay Time	Reset		5.0	_	440	800		
			10		160	300		
			15	_	110	220		
Clock Pulse Width		PW cn. PW cl.	5.0	200	100		ns	
			10	100	50	<u>-</u>		
			15	70	35			
Clock Frequency		PRF	5.0	_	5.0	2.5	MHz	
			10	_	10.0	5.0		
			15	_	15.0	7.5		
Clock Pulse or Enable Rise and Fall Time		tr, tr	5.0		_	15	μs	
			10		_	15		
			15		_	15		
Enable Pulse Width		$PW_{arepsilon}$	5.0	440	220		ns	
			10	200	100			
			15	140	70	_		
Reset Pulse Width		PW_R	5.0	250	125	-		
			10	110	55	_	ns	
			15	80	40	_		

■ SWITCHING TIME TEST CIRCUIT

TIMIG DIAGRAM







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