HD14527B

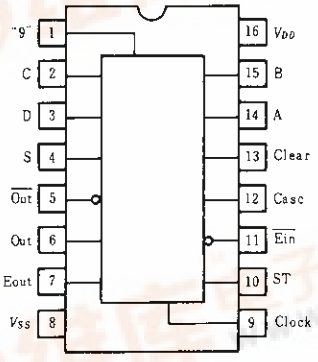
BCD Rate Multiplier

The HD14527B BCD rate multiplier(DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

■ FEATURES

- Quiescent Current=5nA/pkg typ. @5V
- Supply Voltage Range=3 to 18V
- Low Input Capacitance= 5pF typ.
- Internally Synchronous for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- " 9 " Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

■ PIN ARRANGEMENT



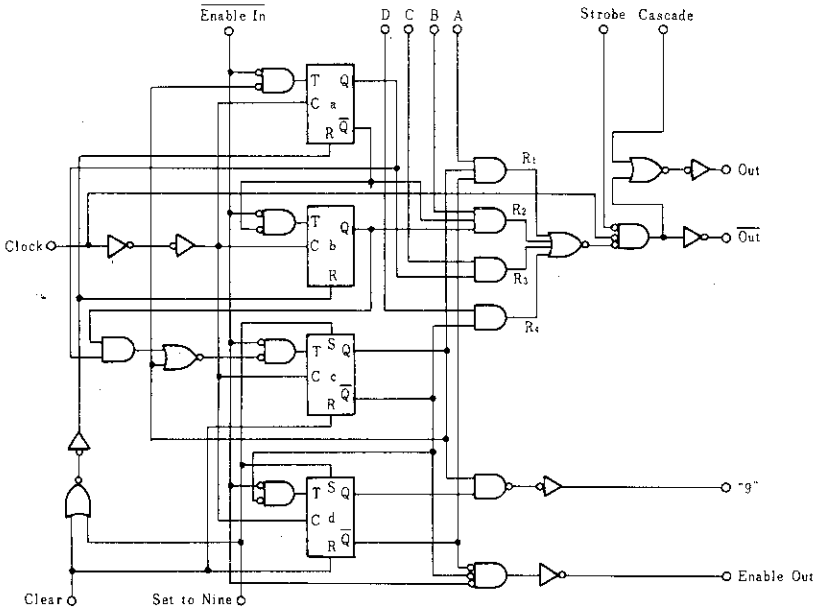
(Top View)

■ TRUTH TABLE

Inputs										Output			
										Logic Level			
										Number of Pulses			
D	C	B	A	Number of Clock Pulses	$\overline{Ein}$	Strobe	Cascade	Clear	Set	Out	$\overline{Out}$	Eout	"9"
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
×	×	×	×	10	1	0	0	0	0	—	—	—	—
×	×	×	×	10	0	1	0	0	0	0	1	1	1
×	×	×	×	10	0	0	1	0	0	1	0	1	1
1	×	×	×	10	0	0	0	1	0	10	10	1	0
0	×	×	×	10	0	0	0	1	0	0	1	1	0
×	×	×	×	10	0	0	0	0	1	0	1	0	1

x = Don't Care

■LOGIC DIAGRAM

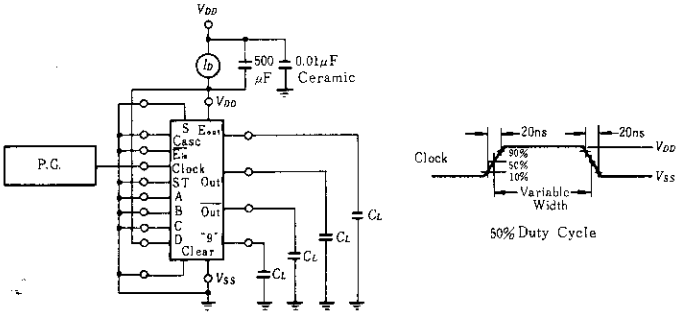


■ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40℃ min	−40℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5$V	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
		5.0	$V_{OH}=4.6$V	−0.2	—	−0.16	−0.36	—	−0.12	—	
		10	$V_{OH}=9.5$V	−0.5	—	−0.4	−0.9	—	−0.3	—	
		15	$V_{OH}=13.5$V	−1.4	—	−1.2	−3.5	—	−1.0	—	
	I_{OL}	5.0	$V_{OL}=0.4$V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5$V	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5$V	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}	—	$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I_T	5.0	Dynamic+I_{DD}, per Gate $C_L=50$ pF, $f=1$ kHz	—	—	—	0.85	—	—	—	μA
		10		—	—	—	1.75	—	—	—	
		15		—	—	—	2.6	—	—	—	

* To calculate total supply current at frequency other than 1kHz.
@V_{DD}=5.0V $I_T=(0.85\mu A/kHz)f+I_{DD}$, @$V_{DD}$=10V $I_T=(1.75\mu A/kHz)f+I_{DD}$, @$V_{DD}$=15V $I_T=(2.6\mu A/kHz)f+I_{DD}$

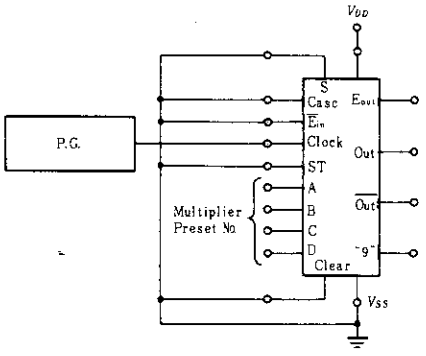
●POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

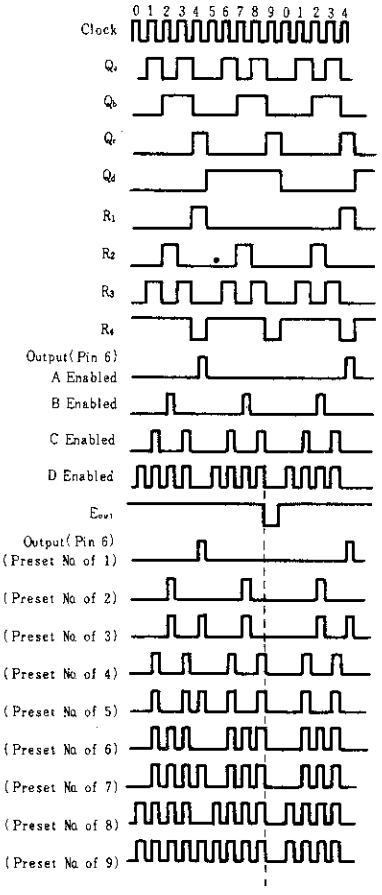


■SWITCHING CHARACTERISTICS (C_L=50pF, Ta=25°C)

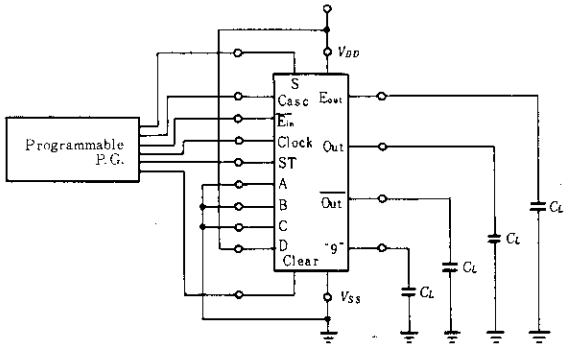
Characteristic		Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		t_f	5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	Clock to Out	t_{PHL}, t_{PLH}	5.0	—	200	500	ns
			10	—	100	250	
			15	—	70	175	
	Clock to $\overline{\text{Out}}$		5.0	—	125	315	
			10	—	65	150	
			15	—	45	115	
	Clock to Eout		5.0	—	295	900	
			10	—	130	325	
			15	—	85	230	
	Clock to "9"		5.0	—	400	1000	
			10	—	155	400	
			15	—	110	300	
	Set, Clear to Out	t_{PHL}	5.0	—	380	1000	ns
			10	—	165	400	
			15	—	110	300	
	Cascade to Out	t_{PLH}	5.0	—	125	315	ns
			10	—	65	150	
			15	—	45	115	
	Strobe to Out	t_{PLH}	5.0	—	230	700	ns
			10	—	105	265	
			15	—	70	190	
Clock Pulse Width		PW_C	5.0	500	250	—	ns
			10	200	110	—	
			15	150	80	—	
Clock Frequency		PRF	5.0	—	2.0	1.0	MHz
			10	—	4.5	2.5	
			15	—	6.0	3.3	
Clock Pulse Rise and Fall Time		t_r, t_f	5.0	—	—	15	μs
			10	—	—	15	
			15	—	—	15	
Set or Clear Pulse Width		PW_S PW_{clear}	5.0	240	80	—	ns
			10	100	35	—	
			15	75	30	—	
Set Removal Time		t_{rem}	5.0	0	−20	—	ns
			10	0	−10	—	
			15	0	−7.5	—	
Enable In Setup Time		t_{setup}	5.0	400	175	—	ns
			10	150	60	—	
			15	120	45	—	

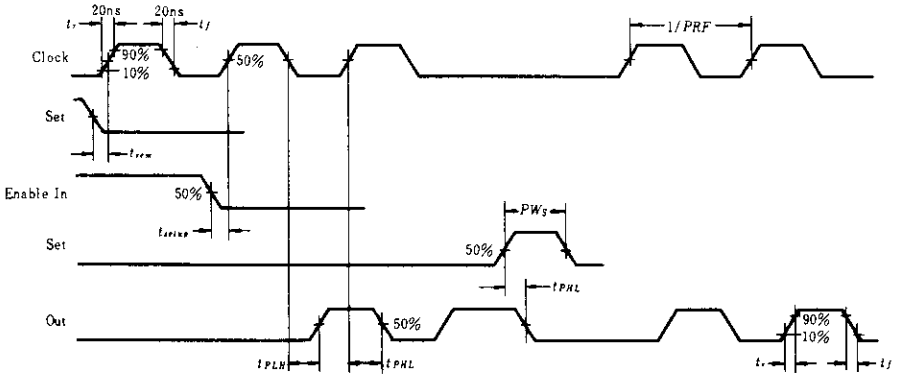
■ TIMING DIAGRAM



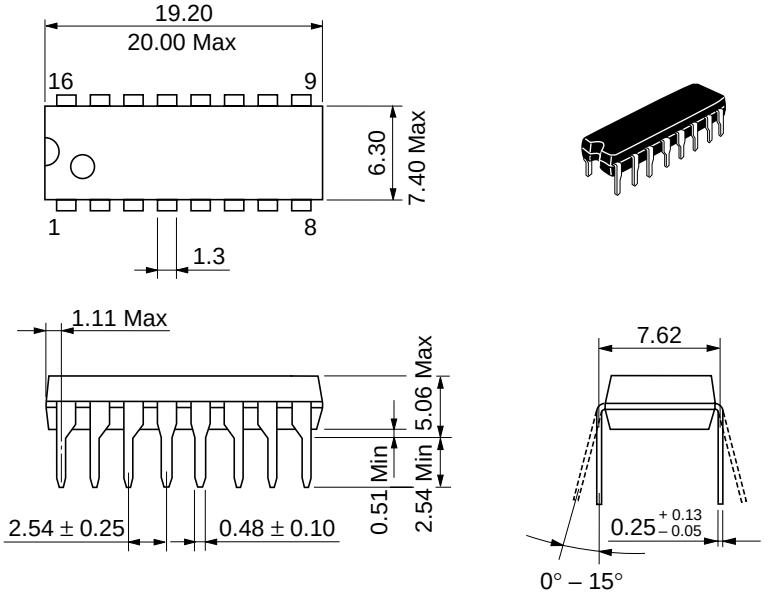


■ SWITCHING TIME TEST CIRCUIT





Unit: mm


19.20
20.00 Max
16
9
6.30
7.40 Max
1
8
1.3
1.11 Max
5.06 Max
0.51 Min
2.54 Min
2.54 ± 0.25
0.48 ± 0.10
7.62
0.25 + 0.13 − 0.05
0° – 15°

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