

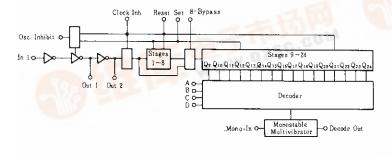
Programmable Timer

The HD14536B programmable timer is a flexible 24-stage ripple binary counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator, or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has also been included. By selecting the appropriate output in conjunction with the correct input clock frequency, a variety of timing can be achieved.

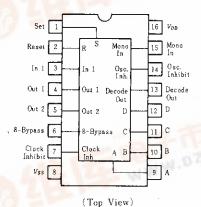
FEATURES

- 24 Flip-Flop Stages ... Will Count from 20 to 224
- Last 16 Stages Selectable by Four-Bit Select Code
- Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit Input
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation with Very Long Rise and Fall Times
- Clock Input f_{max} = 3MHz typ. @10V
- Counter Advances On Negative Going Edge of Clock
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

■BLOCK DIAGRAM



PIN ARRANGEMENT



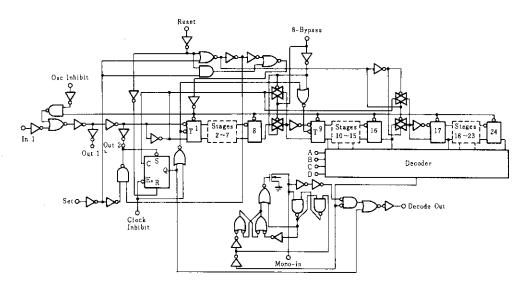
TRUTH TABLE

D	С	В	A	D. 10.	
			А	Decode Out	8-Bypass
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

In 1	Set	Reset	Clock Inhibit	Osc. Inhibit	Out 1	Out 2	Decode Out	
	0	0	0	0			No Change	
	0	0	0	0		_/_	Advance to next stage	
×	1	0	0	0	0	1	1	
×	0	1	0	0	0	1	0	
×	0	0	1	0			No Change	
0	0	0	0	×	0	1	No Change	
1	0	0	0	_/_			Advance to next stage	



LOGIC DIAGRAM

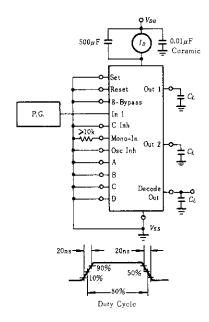


■ ELECTRICAL CHARACTERISTICS

C1	C	Test Conditions	−40 °C		25 °C			85° C		Unit	
Characteristic	Symbol	$V_{DD}(V)$	Test Conditions	min	max	min	typ	max	min	max	Unit
	Vol	5.0	$V_{in}=V_{DD}$ or 0	-	0.05	_	0	0.05		0.05	v
		10		_	0.05	_	0	0.05		0.05	
		15			0.05	_	0	0.05	-	0.05	
Output Voltage		5.0	$V_{i\pi}=0$ or V_{DD}	4.95	_	4.95	5.0		4.95	_	V
	Von	10		9.95	_	9.95	10	_	9.95	-	
		15		14.95	_	14.95	15		14.95	_	
		5.0	$V_{out} = 4.5 \text{ or } 0.5 \text{V}$	_	1.5	_	2.25	1.5	-	1.5	v
	VIL	10	$V_{out} = 9.0 \text{ or } 1.0 \text{V}$	-	3.0	_	4.50	3.0	-	3.0	
Input Voltage		15	$V_{out} = 13.5 \text{ or } 1.5 \text{V}$		4.0		6.75	4.0		4.0	
input voitage		5.0	$V_{\rm out} = 0.5$ or 4.5V	3.5	_	3.5	2.75		3.5		v
	VIH	10	V _{sut} =1.0 or 9.0V	7.0	_	7.0	5.50		7.0		
		15	$V_{\text{out}} = 1.5 \text{ or } 13.5 \text{V}$	11.0	_	11.0	8.25		11.0	_	
	Іон	5.0	$V_{OH}=2.5V$	-1.0	_	-0.8	-1.7	-	-0.6	_	mA
		5.0	V _{OH} =4.6V	-0.2	_	-0.16	-0.36	_	-0.12	_	
		10.	V _{он} =9.5V	-0.5		-0.4	-0.9		-0.3	-	
Output Drive Current		15	V _{OH} =13.5V	-1.4	_	-1.2	-3.5	_	-1.0	-	
	IoL	5.0	$V_{oL}=0.4V$	0.52	_	0.44	0.88		0.36	_	mA
		10	Vor-0.5V	1.3		1.1	2.25		0.9	_	
		15	VoL-1.5V	3.6	_	3.0	8.8	_	2.4	1	
Input Current	Iin.	15		_	±0.3	_	±0.00001	±0.3	1	±1.0	μA
Input Capacitance	Ci.	-	$V_{in}=0$	_	_	_	5.0	7.5	_	_	рF
	I_{DD}	5.0	Zero Signal, per Package		50	_	0.010	50	1	375	μA
Quiescent Current		19		_	100	_	0.020	100	_	750	
		15			200		0.030	200	_	1500	
-	I_{T}	5.0	Dynamic + IDD,	_	_	_	1.15	_	_		
Total Supply Current*		10	per Gate	_		_	2.3		_		μA
		15	$C_L = 50 \mathrm{pF}$, $f = 1 \mathrm{kHz}$	_	_	_	3.55		_	_	

^{*} To calculate total supply current at frequency other than 1kHz.

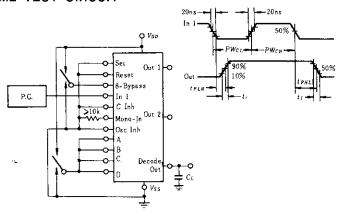
POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

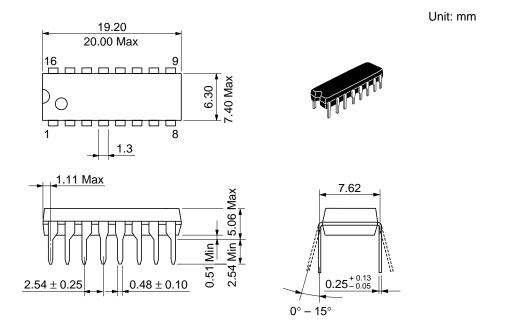


■ SWITCHING CHARACTERISTICS $(C_L = 50 \text{pF}, T_a = 25 ^{\circ}\text{C})$

Characteristic		Symbol	$V_{DD}(V)$	min	typ	max	Unit
	t.	5.0		180	400		
Output Rise Time		10	-	90	200	ns	
		15	_	65	160		
Output Fall Time		ŧ,	5.0	_	120	250	ns
			10	_	60	125	
•			15		40	100	1
	Cl. 1 O		5.0		1800	5400	ns μs
	Clock to Q	tpin,	10	_	650	2000	
	(Pin 6 High)		15	-	450	1500	
			5.0		3.8	12	
	Clock to Q		10	_	1.5	4.5	
Propagation Delay Time	(Pin 6 Low)		15	-	1.1	3.5	
Fropagation Delay Time	Clock to Q16		5.0	_	7.0	21	
			10	_	3.0	9.0	
	*		15		2.2	7.0	
		tpHL	5.0	_	1500	4500	ns
	Reset to Q.		10	_	600	1800	
			15	_	450	1400	
			5.0	900	300	_	
Clock Pulse Width		PW_c	10	300	100		ns
			15	255	85	_]
			5.0	_	1.2	0.4	
Clock Frequency	PRF	10		3.0	1.5	MHz	
		15		5.0	2.0	1	
	t_n t_f	5.0	No Limit		•		
Clock Pulse Rise and Fall Time		10			}		
		15					
			5.0	1500	500		
Reset Pulse Width	PW_R	10	600	200		ns	
			15	450	150		

■ SWITCHING TIME TEST CIRCUIT





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Semiconductor & Integrated Circuits. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1>(408) 433-0223 Hitachi Europe GmbH Electronic components Group Dornacher Stra§e 3 D-85622 Feldkirchen, Munich Germany

Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road

Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533

Hitachi Asia I td Taipei Branch Office

3F, Hung Kuo Building. No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Tsim Sha Tsu Kowloon, Hong Kong

Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281 Telex: 40815 HITEC HX

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