HD14541B

Programmable Oscillator/Timer

The HD14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic. Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

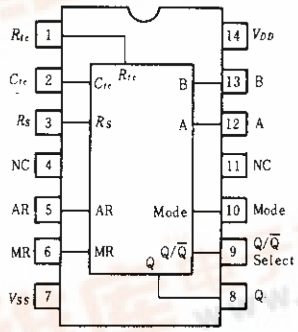
■ FEATURES

- Available Outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Low Symmetrical Output Resistance (typically 100Ω @15V)
- Built-in Low Power RC Oscillator (±2% accuracy over temperature range and ±10% supply and ±3% over processing @ < 10kHz)
- Oscillator Frequency Range = DC to 100kHz
- Oscillator May Be Bypassed if External Clock is Available (Apply external clock to Pin 3)
- Automatic Reset Initializes All Counters When Power Turns On (Limits-V_{DD} from 8.5V to 18V when enabled)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- Q/$\bar{Q}$ Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Supply Voltage Range = 3 to 18V

■ MAXIMUM RATINGS (Voltages referenced to V_{SS})

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5～+18	V
Input/Output Voltage	V_{in}, V_{out}	−0.5～V_{DD}+0.5	V
DC Current Drain per Input Pin	I_{in}	±10	mA
DC Current Drain per Output Pin	I_{OL}, I_{OH}	±45	mA
Operating Temperature Range	T_A	−40～+85	℃
Storage Temperature Range	T_{stg}	−65～+150	℃
Power Dissipation	P_D	300	mW

■ PIN ARRANGEMENT



(Top View)

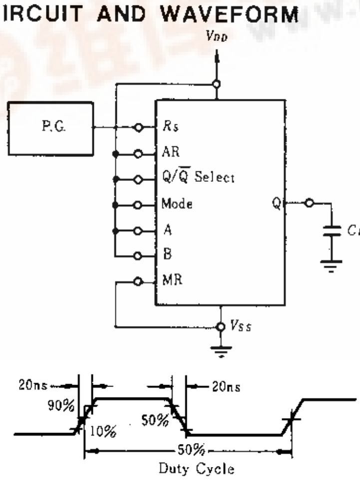
■ TRUTH TABLE

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset ON
9	Output Initially Low After Reset	Output Initially High After Reset
10	Single Cycle Mode	Recycle Mode

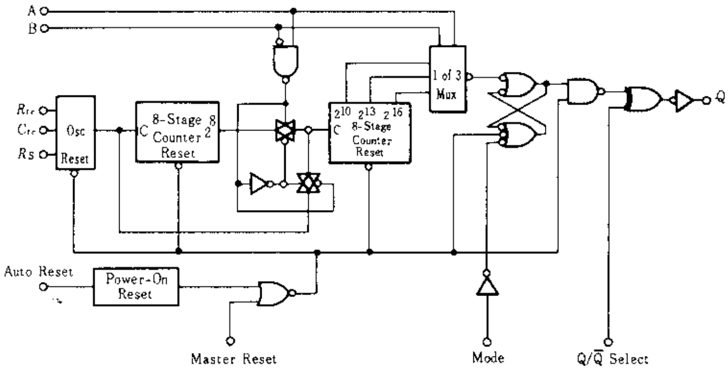
■ FREQUENCY SELECTTION TABLE

A	B	Number of Counter Stages	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

● POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



■BLOCK DIAGRAM

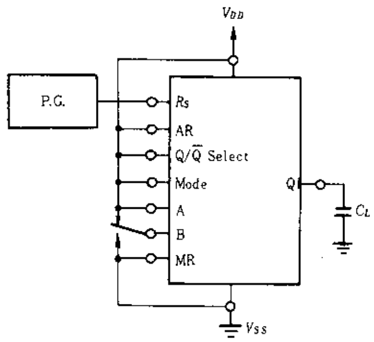


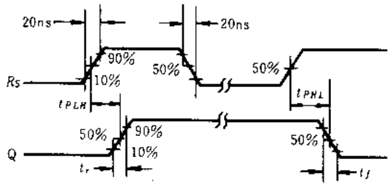
■ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40℃ min	−40℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5$V	−5.1	—	−4.27	−12.83	—	−3.5	—	mA
		10	$V_{OH}=9.5$V	−2.69	—	−2.25	−6.75	—	−1.85	—	
		15	$V_{OH}=13.5$V	−10.5	—	−8.8	−26.33	—	−7.22	—	
	I_{OL}	5.0	$V_{OL}=0.4$V	1.24	—	1.04	3.12	—	0.85	—	mA
		10	$V_{OL}=0.5$V	3.18	—	2.66	8.0	—	2.18	—	
		15	$V_{OL}=1.5$V	12.4	—	10.4	31.2	—	8.50	—	
Input Current	I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}		$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Auto Reset Quiescent Current	I_{DDR}	5.0	Pin 5 is low	—	200	—	7	200	—	1200	μA
		10		—	250	—	30	250	—	1500	
		15		—	500	—	82	500	—	2000	
Total Supply Current*	I_T	5.0	Dynamic $+I_{DD}$, per Gate $C_L=50$pF, $f=1$kHz	—	—	—	0.4	—	—	—	μA
		10		—	—	—	0.8	—	—	—	
		15		—	—	—	1.2	—	—	—	

* To calculate total supply current at frequency other than 1kHz.
@$V_{DD}=5.0$V $I_T=(0.4\mu A/kHz)f+I_{DD}$, @$V_{DD}=10$V $I_T=(0.8\mu A/kHz)f+I_{DD}$, @$V_{DD}=15$V $I_T=(1.2\mu A/kHz)f+I_{DD}$

■ SWITCHING TIME TEST CIRCUIT

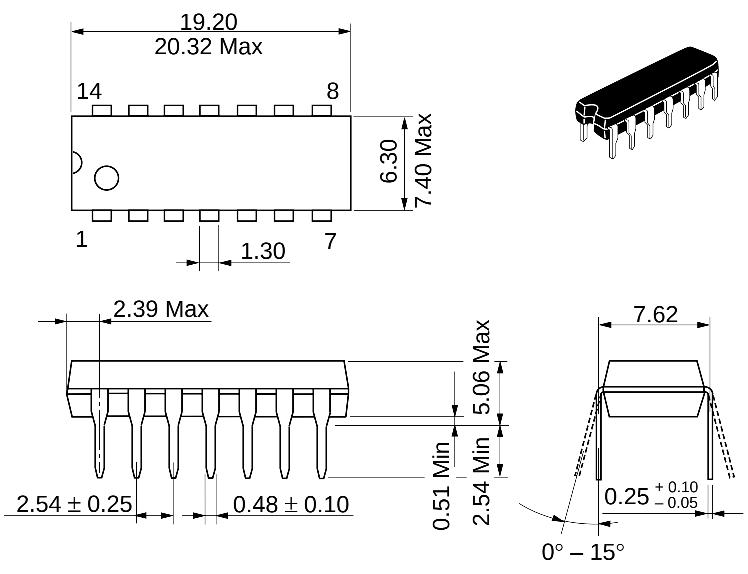




■ SWITCHING CHARACTERISTICS (C_L=50pF, Ta=25°C)

Characteristic		Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		t_f	5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	Clock to Q (2^8 Output)	t_{PLH}, t_{PHL}	5.0	—	3.5	10.5	μs
			10	—	1.25	3.8	
			15	—	0.9	2.9	
	Clock to Q (2^{16} Output)		5.0	—	6.0	18	
			10	—	3.5	10	
			15	—	2.5	7.5	
Clock Pulse Width		PW_C	5.0	900	300	—	ns
			10	300	100	—	
			15	225	85	—	
Clock Frequency		PRF	5.0	—	1.5	—	MHz
			10	—	4.0	—	
			15	—	6.0	—	
Minimum Master Reset Pulse Width		PW_{MR}	5.0	900	300	—	ns
			10	300	100	—	
			15	225	85	—	

Unit: mm


19.20
20.32 Max
14
8
6.30
7.40 Max
1
7
1.30
2.39 Max
5.06 Max
0.51 Min
2.54 Min
2.54 ± 0.25
0.48 ± 0.10
7.62
0.25 + 0.10 − 0.05
0° – 15°

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Stra§e 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX