HD14549B供应商 HD14549B, **HD1455**

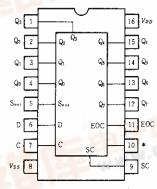
Successive Approximation Register

The HD14549B and the HD14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the HD14549B is required in the cascaded mode when greater than 8 bits are disired. The Feed Forward (FF) of the HD14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles. Applications for the HD14549B and HD14559B include analog-todigital conversion, with serial and parallel outputs

■ FEATURES

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the HA17408P 8-bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

■ PIN ARRANGEMENT



(Top View)

Note) *: HD14549B is MR input. HD14559B is FF input.

TRUTH TABLE

HD14549B

SC	SC (1=1)	MR	MR (t-1)	Clock	Action
×	×	×	×		
×	×	1	×		Reset
1	0	0	0	5	Start Conversion
1	×	0	1	5	Start Conversion
1	1	0	0		Continue Conversion
0	×	0	×		Continue Pre- vious Operation

HD14559B

SC	SC (1-1)	EOC	Clock	Action
×	×	×	Z	
1	0	0		Start Conversion
×	1	0		Continue Conversion
0	0	0		Continue Conversion
0	×	1		Retain Con- version Result
1	×	1		Start Conversion

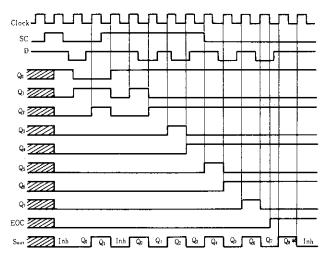
WWW.DZSC



^{× =} Don't Care

t-1 = State at Previous Clock

■ TIMING DIAGRAM



Note) | Don't care condition Inh; Indicates Serial Out is inhibited

> *; Q₈ is ninthbit of serial information available from 8-bit register.

Pin $10 - V_{ss}$

■ ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	T . C . I'm	-4	-40°C		25°C			85°C		
			$V_{DD}(V)$	Test Conditions	min	max	min	typ	max	min	max	Unit
Output Voltage		Vol	5.0	V _{in} - V _{DD} or 0	_	0.05	_	0	0.05		0.05	v
			10			0.05	_	0	0.05		0.05	
			15			0.05	-	0	0.05	-	0.05	
		Von	5.0		4.95	_	4.95	5.0	_	4.95	- [v
			10	$V_{is} = 0$ or V_{DD}	9.95	_	9.95	10	-	9.95		
			15		14.95		14.95	15	_	14.95	_	
			5.0	$V_{out} = 4.5$ or $0.5 \mathrm{V}$	_	1.5	_	2.25	1.5	_	1.5	v
		VIL	10	$V_{out} = 9.0 \text{ or } 1.0 \text{ V}$	_	3.0	-	4.50	3.0		3.0	
Input Voltage			15	$V_{\text{out}} = 13.5 \text{ or } 1.5 \text{ V}$		4.0		6.75	4.0		4.0	
input voitage			5.0	$V_{out} = 0.5 \text{ or } 4.5 \text{ V}$	3.5	_	3.5	2.75	_	3.5	_	v
		V_{IH}	10	V _{out} = 1.0 or 9.0 V	7.0	_	7.0	5.50	_	7.0	_	
			15	$V_{out} = 1.5 \text{ or } 13.5 \text{ V}$	11.0	_	11.0	8.25	_	11.0		
		-	5.0	$V_{OB} = 2.5 \mathrm{V}$	-1.0		-0.8	-1.7	_	-0.6	_	
		Іон	5.0	$V_{OH}=4.6\mathrm{V}$	-0.2	_	-0.16	-0.36		-0.12	1	mA
			10	$V_{OH} = 9.5 \text{ V}$	-0.5		-0.4	-0.9		-0.3		
			15	$V_{OH} = 13.5 \mathrm{V}$	-1.4	_	-1.2	-3.5	-	-1.0		
Output Drive			5.0	$V_{OL}=0.4\mathrm{V}$	1.04	-	0.88	1.76	ı	0.72		mA
Current	Q		10	$V_{0L} = 0.5 \text{ V}$	2.6	-	2.2	4.5	ı	1.8	_	
		J ,	15	$V_{OL} = 1.5 \mathrm{V}$	7.2	_	6.0	17.6	_	4.8		
		Pin 5, 11	5.0	$V_{OL} = 0.4 \mathrm{V}$	0.52		0.44	0.88	_	0.36	_	
	Pin 5,11		10	$V_{OL} = 0.5 \mathrm{V}$	1.3	_	1.1	2.25		0.9		
			15	$V_{OL} = 1.5 \mathrm{V}$	3.6	_	3.0	8.8	1	2.4		
Input Current		I.a	15			±0.3	_	±0.00001	±0.3		±1.0	μA
Input Capacitance		Cin		$V_{in} = 0$		-		5.0	7.5			pF
Quiescent Current		Ind	5.0	Zero Signal,		20	-	0.005	20		150	μΑ
			10	per Package		40	-	0.010	40		300	
			15	per I wenuge		80	_	0.015	80	-	600	
.'otal Supply Current*			5.0	Dynamic $+I_{DD}$,	-	_	_	0.8	_			μА
		I_T	10	per Gate				1.6	_		_	
			15	$C_L = 50 \mathrm{pF}, f = 1 \mathrm{kHz}$		_	-	2.4	_	_]

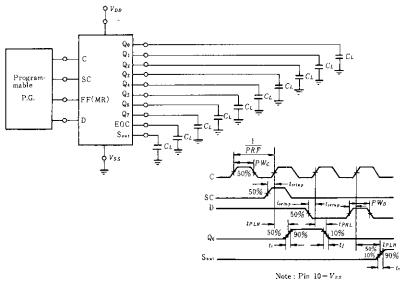
^{*} To calculate total supply current at frequency other than 1kHz. $@V_{DD} = 5.0 \text{V} \quad I_T = (0.8 \, \mu\text{A/kHz}) \\ f + I_{DD}, \quad @V_{DD} = 10 \text{V} \quad I_T = (1.6 \, \mu\text{A/kHz}) \\ f + I_{DD}, \quad @V_{DD} = 15 \text{V} \quad I_T = (2.4 \, \mu\text{A/kHz}) \\ f + I_{DD}, \quad &V_{DD} = 15 \text{V} \quad I_T = (2.4 \, \mu\text{A/kHz}) \\ f + I_{DD}, \quad &V_{DD} = 15 \text{V} \quad &V_{DD} = 15 \text{V} \quad &V_{DD} = 15 \text{V} \\ f = (2.4 \, \mu\text{A/kHz}) \\ f = (2.4 \, \mu\text{A/kHz}$

HD14549B, HD14559B---

SWITCHING CHARACTERISTICS ($C_L = 50 \,\mathrm{pF}, Ta = 25^{\circ}\mathrm{C}$)

Characterist	Symbol	$V_{DD}(V)$	min	typ	max	Unit	
	t,	5.0	_	180	400		
Output Rise Time		10		90	200	ns	
		15	_	65	160		
	t_f	5.0	_	120	250		
Output Fall Time		10	_	60	125	ns	
		15		40	190		
		t _{РL} н, t _Р нL	5.0		500	1200	
	Clock to Q		10	_	210	500	1
12			15		155	380	
			5.0	_	750	1800	
Propagation Delay Time	Clock to Sout		10	_	310	750	ns
			15		220	550	
			5.0	_	300	750	
	Clock to EOC		10		130	325	
			15		100	250	
	<u> </u>	tsetup	5.0	300	125	_	ns
SC, D, FF, MR Setup Time			10	150	50	_	
			15	115	40	_	
			5.0	600	350	_	
Clock Pulse Width	PW_c	10	300	135	_	ns	
		15	225	100	_	1	
			5.0	750	250		1
D, SC, FF, MR Pulse Wid	PW	10	300	100		ns	
			15	225	80]
	tr, tr	5.0	_	_	15		
Clock Pulse Rise and Fall Time		10			5.0	μs	
		15	_	_	4.0	1	
	PRF	5.0		1.5	0.8		
Clock Frequency		10		3.0	1.5	MHz	
		15		4.0	2.0		

■ SWITCHING TIME TEST CIRCUIT



■ OPERATING CHARACTERISTICS

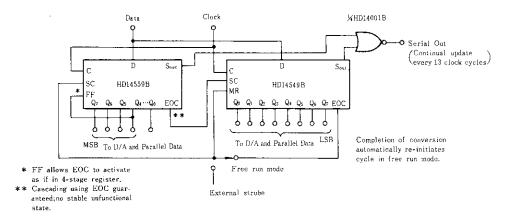
Both the HD14549B and HD14559B can be operated in either the "free run" or "strobed operation" mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for HD14549B but either 1 or 0 for HD14559B) no stable state exists under continual clocked operation. The HD14559B will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1. All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse. Operation of the various terminals is as follows:

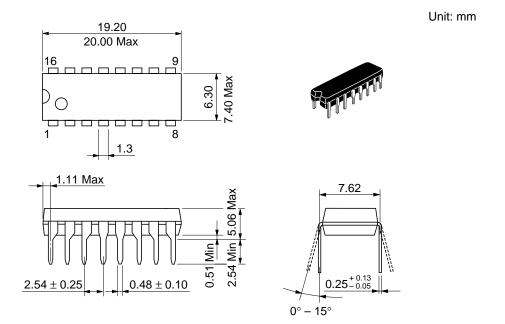
- C = Clock ... A Positive-going transition of the Clock is required for data on any input to be strobed into the circuit.
- SC = Start Convert ... A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.
- D = Data In ... Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.
- MR = Master Reset (HD14549B only) ... Resets all output to 0 on positive-going transitions of the clock, if removed while SC = 0, the circuit will remain reset until SC = 1. This allow easy cascading of circuits.
- FF = Feed Forward (HD14559B only) ... Provides register shortening by removing unwanted bits from a system. For operation with less than 8 bits, tie the output following the least significant bit of the circuits to EOC. E. G., for a 6-bit conversion,

tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Not that Q1 and Q0 will still operate and must be disregarded. For 8-bit operation, FF is tied to VSS. For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the HD14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the HD14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the HD14559B to the HD14549B. The Serial Out (Sout) inhibit structure of the HD14559B remains inactive one cycle after EOC goes high, while Sout of the HD14549B remains inhibited until the second clock cycle of its operation

- Qn = Data Outputs ... After a conversion is initiated the Q's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.
- EOC = End of Convert ... This output goes high on the negative-going transition of the clock following FF = 1 (for the HD14559B) or the conditional reset of Q0. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.
- Sout = Serial Out ... Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.

•12-bit Conversion Scheme





Cautions

- 1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
- 2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
- 3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
- 4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as failsafes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
- 5. This product is not designed to be radiation resistant.
- 6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
- 7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor

HITACH

Semiconductor & Integrated Circuits. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica http:semiconductor.hitachi.com/ Europe http://www.hitachi-eu.com/hel/ecg

Asia (Singapore) http://www.has.hitachi.com.sg/grp3/sicd/index.htm http://www.hitachi.com.tw/E/Product/SICD_Frame.htm Asia (Taiwan) Asia (HongKóng) http://www.hitachi.com.hk/eng/bo/grp3/index.htm

Japan http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1>(408) 433-0223 Hitachi Europe GmbH Electronic components Group Dornacher Stra§e 3 D-85622 Feldkirchen, Munich Germany

Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road

Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533

Hitachi Asia I td Taipei Branch Office

3F, Hung Kuo Building. No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Tsim Sha Tsu Kowloon, Hong Kong

Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281 Telex: 40815 HITEC HX

Copyright ' Hitachi, Ltd., 1999. All rights reserved. Printed in Japan.