HD151TS302RP

Spread Spectrum Clock for EMI Solution

HITACHI

ADE-205-655A (Z)

Preliminary
Rev. 1
Sep. 2001

Description

The HD151TS302 is a high-performance Spread Spectrum Clock modulator. It is suitable for low EMI solution.

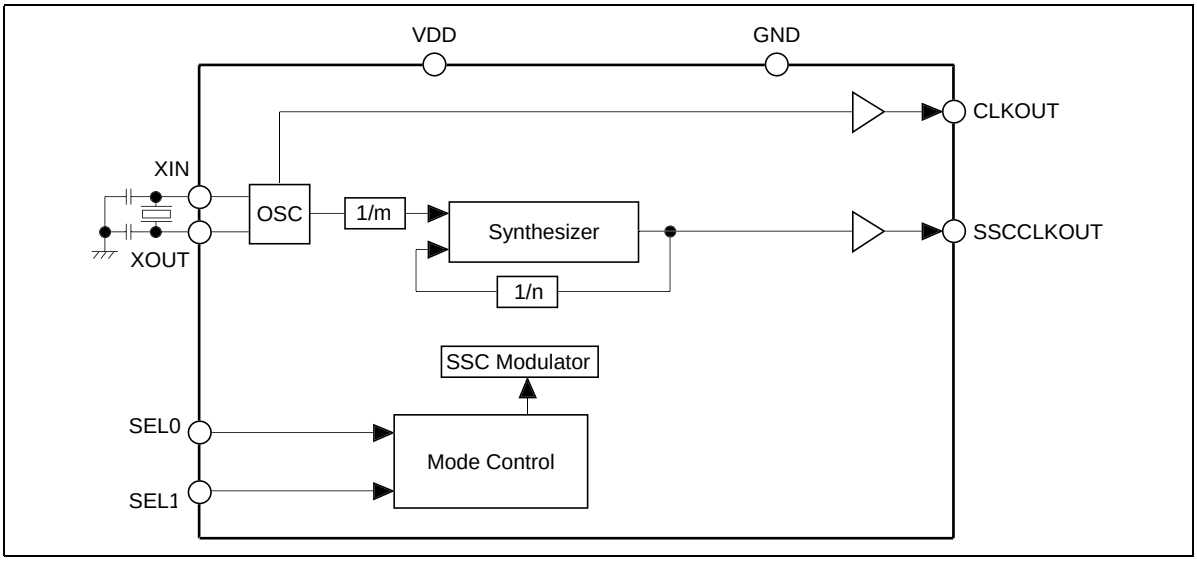
Features

- Supports 10 MHz to 60 MHz operation. (Designed for XIN = 24 MHz and 48 MHz)
- 1 copy of clock out with spread spectrum modulation @3.3 V
- 1 copy of reference clock @3.3 V
- Programmable spread spectrum modulation (–0.5%, –1.0%, –3.0% down spread modulation and spread spectrum disable mode.)
- SOP–8pin
- Pin to pin compatible with HD151TS301RP

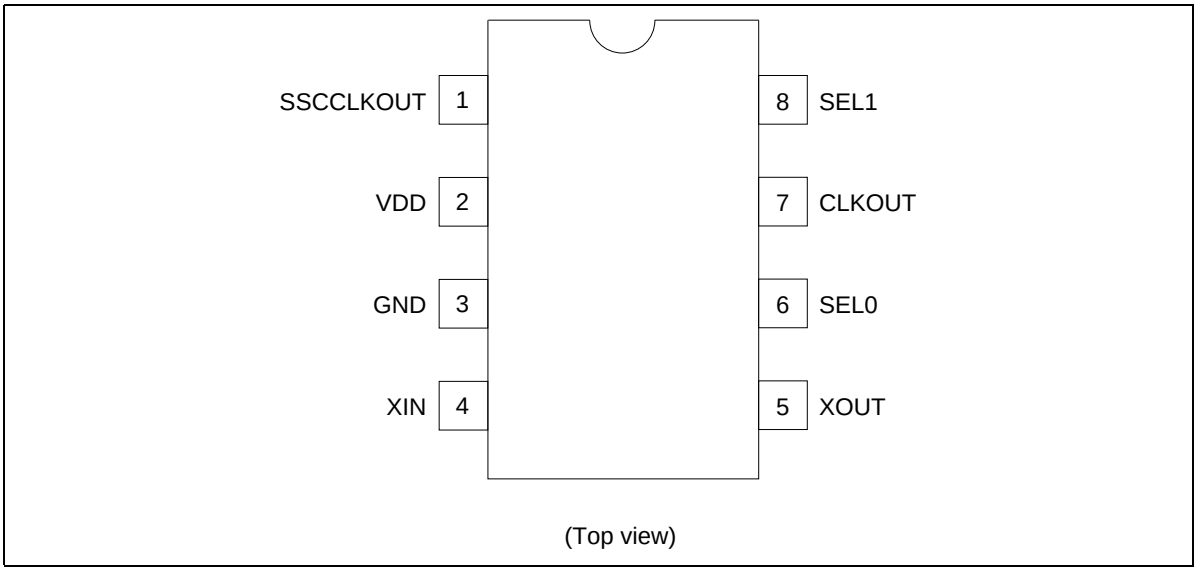
Key Specifications

- Supply voltages : VDD = 3.3 V±0.165 V
- Ta = 0 to 70°C operating range
- Clock output duty cycle = 50±5%
- Cycle to cycle jitter = ±250 ps typ.

Block Diagram



Pin Arrangement



SSC Function Table

SEL1 :0	Spread Percentage
0 0	–1.0%
0 1	–3.0%
1 0	SSC OFF
1 1	–0.5%

Note: –3.0% SSC is selected for default by internal pull-up & down resistors.

Clock Frequency Table

XIN(MHz)	SSCCLKOUT(MHz)	CLKOUT(MHz)
48	48[*1]	48[*2]
24	24[*1]	24[*2]

Notes: 1. With spread spectrum modulation.
2. Without spread spectrum modulation.

Pin Descriptions

Pin name	No.	Type	Description
GND	3	Ground	GND pin
VDD	2	Power	Power supplies pin. Normally 3.3 V.
CLKOUT	7	Output	Normally 3.3 V reference clock output.
SSCCLKOUT	1	Output	Spread spectrum modulated clock output.
XIN	4	Input	Oscillator input.
XOUT	5	Output	Oscillator output.
SEL0	6	Input	SSC mode select pin. LVCMOS level input. Pull-up by internal resistor. (100 kΩ).
SEL1	8	Input	SSC mode select pin. LVCMOS level input. Pull–down by internal resistor (100 kΩ).

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	VDD	–0.5 to 4.6	V	
Input voltage	V_I	–0.5 to 4.6	V	
Output voltage [*1]	V_O	–0.5 to VDD+0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	–50	mA	$V_O < 0$
Continuous output current	I_O	±50	mA	V_O = 0 to VDD
Maximum power dissipation at Ta = 55°C (in still air)		0.7	W	
Storage temperature	T_{stg}	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	VDD	3.135	3.3	3.465	V	
DC input signal voltage		–0.3	—	VDD+0.3	V	
High level input voltage	V_{IH}	2.0	—	VDD+0.3	V	
Low level input voltage	V_{IL}	–0.3	—	0.8	V	
Operating temperature	T_a	0	—	70	°C	
Input clock duty cycle		45	50	55	%	

DC Electrical Characteristics

Ta = 0 to 70°C, VDD = 3.3 V±5%

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	—	—	0.8	V	
Input high voltage	V_{IH}	2.0	—	—	V	
Input current	I_I	—	—	±10	µA	V_I = 0 V or 3.465 V, VDD = 3.465 V, XIN pin
		—	—	±100		V_I = 0 V or 3.465 V, VDD = 3.465 V, SEL0, SEL1 pins
Input slew rate		1	—	4	V / ns	20% – 80%
Input capacitance	C_I	—	—	4	pF	SEL0, SEL1
Operating current		—	7	—	mA	XIN = 24 MHz, C_L = 0 pF, VDD = 3.3 V

DC Electrical Characteristics / Clock Output & SSC Clock Output

Ta = 0 to 70°C, VDD = 3.3 V±5%

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage	V_{OH}	3.1	—	—	V	I_{OH} = –1 mA, VDD = 3.3 V
	V_{OL}	—	—	50	mV	I_{OL} = 1 mA, VDD = 3.3 V

AC Electrical Characteristics / Clock Output & SSC Clock Output

Ta = 25°C, VDD = 3.3 V, C_L = 30 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter [*1, 2]	t_{CCS}	—	| 250 |	| 300 |	ps	SSCCLKOUT, Fig1, 24 MHz	SSC = –0.5% SEL1:0 = 11
		—	| 250 |	| 300 |		SSCCLKOUT, Fig1, 48 MHz	
		—	| 250 |	| 300 |		SSCCLKOUT, Fig1, 24 MHz	SSC = –3.0% SEL1:0 = 01
		—	| 250 |	| 300 |		SSCCLKOUT, Fig1, 48 MHz	
		—	| 250 |	| 300 |		CLKOUT, Fig1, 24 MHz & 48 MHz	
Output frequency [*1, 2]		23.7	—	24.2	MHz	SSCCLKOUT, XIN = 24 MHz	SSC = –0.5% SEL1:0 = 11
		47.0	—	48.7		SSCCLKOUT, XIN = 48 MHz	
		23.1	—	24.2		SSCCLKOUT, XIN = 24 MHz	SSC = –3.0% SEL1:0 = 01
		45.9	—	48.7		SSCCLKOUT, XIN = 48 MHz	
		23.8	—	24.2		CLKOUT, 24 MHz	
		47.3	—	48.7		CLKOUT, 48 MHz	
Slew rate [*1]	t_{SL}	1.0	—	—	V/ns	@48 MHz CLKOUT	0.4 V to 2.4 V
Clock duty cycle [*1]		45	50	55	%		
Output impedance [*1]		—	30	—	Ω		
Spread spectrum modulation frequency [*1]		—	33	—	KHz	@48 MHz SSCCLKOUT	
Input clock frequency		10	—	60	MHz		
Stabilization time [*1,3]		—	—	2	ms		

Notes: 1. Parameters are guaranteed by design and characterization. Not 100% tested in production.
2. Cycle to cycle jitter and output frequency are included spread spectrum modulation.
3. Stabilization time is the time required for the integrated circuit to obtain phase lock of its input signal after power up.

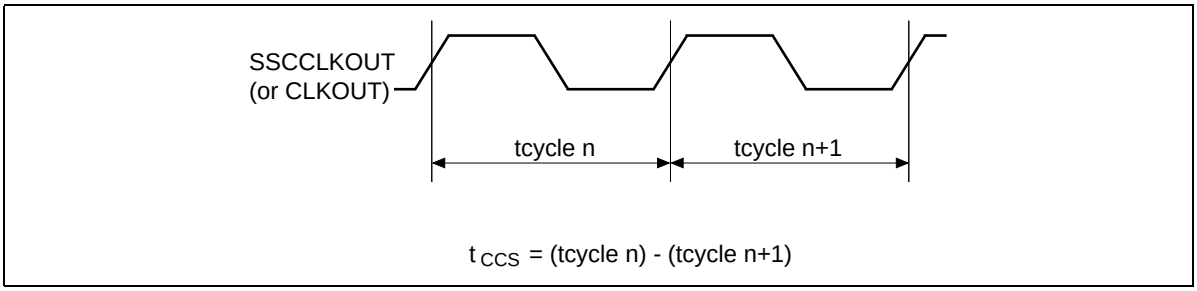
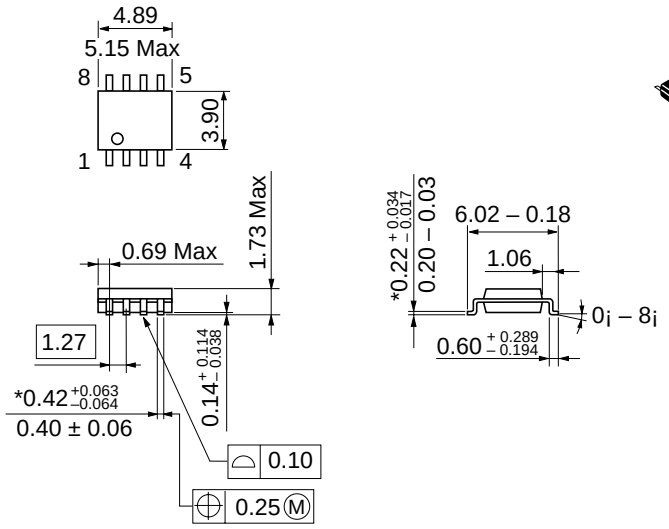


Figure 1 Cycle to cycle jitter

Package Dimensions

Unit: mm



Hitachi Code	FP-8DC
JEDEC	—
EIAJ	—
Mass (reference value)	0.08 g

*Dimension including the plating thickness
Base material dimension

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