HD404328, HD4074329
4-Bit Single-Chip Microcomputer

HITACHI®

Description

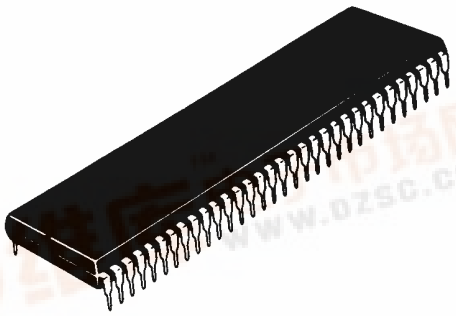
The HD404328 and HD4074329 are HMCS400-series microcomputers designed to increase program productivity and also incorporate large-capacity memory. Each microcomputer has an LCD driver/controller, A/D converter, zero-crossing detection circuit, and 32-kHz oscillator for clock.

The HD4074329, which includes PROM, is a ZTAT microcomputer that can dramatically shorten system development periods and smooth the process from debugging to mass production.

Features

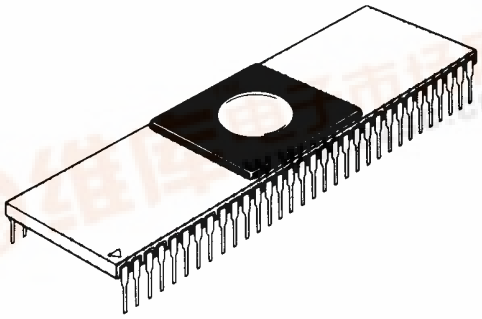
- 8,192-word × 10-bit ROM (HD404328)
  16,384-word × 10-bit PROM (HD4074329)
  (ZTAT versions are 27256-compatible)
- 256-digit × 4-bit RAM (HD404328)
  512-digit × 4-bit RAM (HD4074329)
- 35 I/O pins
  — 2 input pins
  — 33 input/output pins, including 8 large-current pins (15 mA, max) and 16 pins multiplexed with LCD segment pins
- Three timer/counters
- Clock-synchronous 8-bit serial interface
- A/D converter (8-bit × 4-channel)
- 12-digit LCD driver
  — Static, 1/4, 1/2, 1/3 Duty Cycle
- Zero-crossing detection circuit (optional)
- Eight interrupt sources
  — Two external sources, including one double-edge function
  — Six internal sources
- Subroutine stack
  — Up to 16 levels, including interrupts
- Four low-power dissipation modes
  — Subactive mode (optional)
  — Standby mode
  — Watch mode
- Built-in oscillator
  — Crystal or ceramic filter (external clock also enabled)

HD404328S, HD4074329S



DP-64S

HD404328FS, HD4074329FS



FP-64B

HD4074329C

DC-64S

- Instruction cycle time: 2 μs (f_{OSC}=4 MHz)
- Two operating modes
  — MCU mode
  — PROM mode (HD4074329 only)

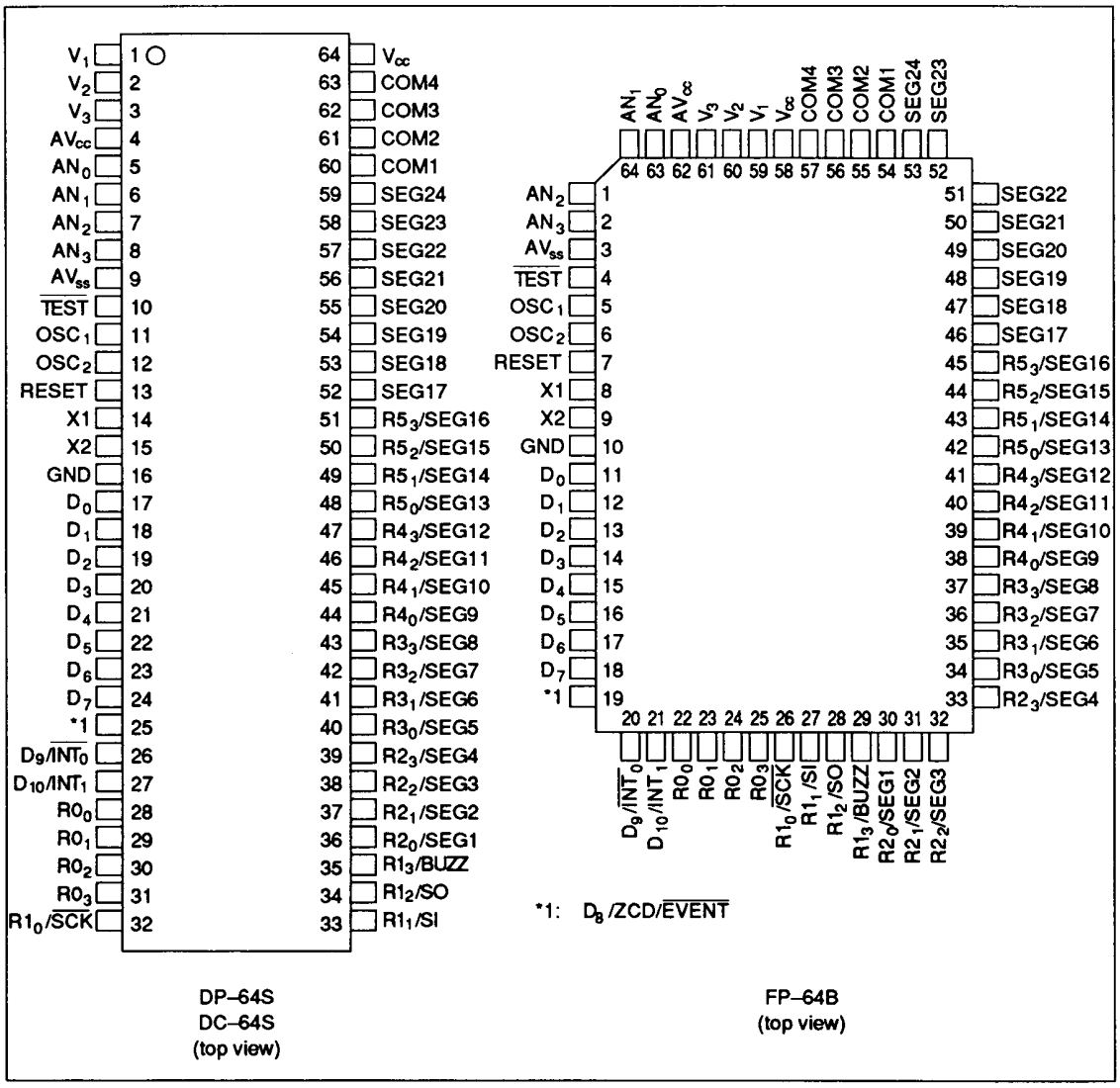
Support Tools

- Macro assembler for H68/H680SD series
- Emulator for AS microcomputers (with realtime trace function)
  — An emulator unit, target probe, and user cable are not included. Any emulator unit designed for the

Ordering Information

Type	Product Name	ROM (Words)	Package	Comment
Mask ROM	HD404328S	8,192	DP–64S	
	HD404328FS		FP–64B	
ZTAT	HD4074329S	16,384	DP–64S	
	HD4074329FS		FP–64B	
	HD4074329C		DC–64S	**Window**

Pin Arrangement

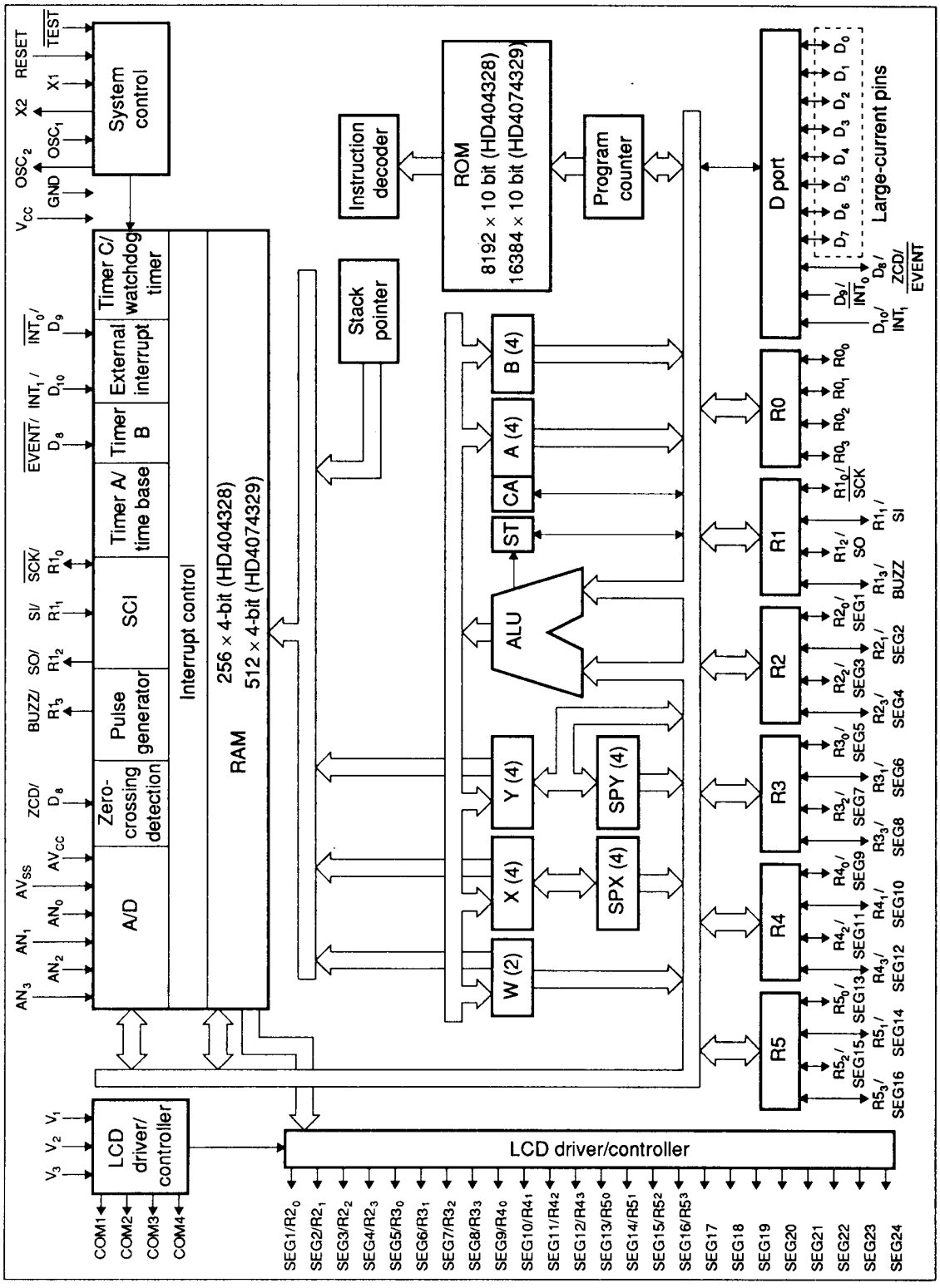


Note: For packaging details, see page 87.

Pin Description

Item	Symbol	Pin Number DP-64S DC-64S	Pin Number FP-64B	I/O	Function
Power supply	V_{CC}	64	58		Applies power voltage
	GND	16	10		Connected to ground
Test	$\overline{TEST}$	10	4	I	Used for factory testing only: connect this pin to V_{CC}
Reset	RESET	13	7	I	Resets the MCU
Oscillator	OSC_1	11	5	I	Input/output pins for the internal oscillator circuit: connect them to a crystal, ceramic filter, or external oscillator circuit
	OSC_2	12	6	O	
	X1	14	8	I	Used for a 32.768-kHz crystal for clock purposes: if not used, fix X1 to V_{CC} and leave X2 open
	X2	15	9	O	
Port	D_0–D_8	17–25	11–19	I/O	Input/output ports addressed by individual bits; pins D_0–D_7 are large-current pins that can each supply up to 15 mA
	D_9, D_{10}	26, 27	20, 21	I	Input ports addressable by individual bits
	$R0_0$–$R5_3$	28–51	22–45	I/O	Input/output ports addressable in 4-bit units
Interrupt	$\overline{INT_0}$, INT_1	26, 27	20, 21	I	Input pins for external interrupts
Serial	$\overline{SCK}$	32	26	I/O	SCI clock input/output pin
	SI	33	27	I	SCI receive data input pin
	SO	34	28	O	SCI transmit data output pin
Buzzer	BUZZ	35	29	O	Buzzer signal output pin
LCD	V_1, V_2, V_3	1–3	59–61		Power pins for LCD driver; can be left open in operation because they are connected by internal voltage division resistors Voltage conditions are: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$
	COM1–COM4	60–63	54–57	O	Common signal pins for LCD
	SEG1–SEG24	36–59	30–53	O	Segment signal pins for LCD
A/D converter	AV_{CC}	4	62		Power pin for A/D converter: connect it to the same potential as V_{CC}, as close physically as possible to the power source
	AV_{SS}	9	3		Ground for AV_{CC}: connect it to the same potential as GND, as close physically as possible to the power source
	AN_0–AN_3	5–8	63, 64, 1, 2	I	Analog input pins for 4-channel A/D converter
Zero-crossing detection	ZCD	25	19	I	Zero-crossing detection input pin
Counter	$\overline{EVENT}$	25	19	I	Event count input pin

Block Diagram



Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1 and described below.

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt service routines. After MCU reset or an interrupt routine is serviced, program execution continues from the vector address.

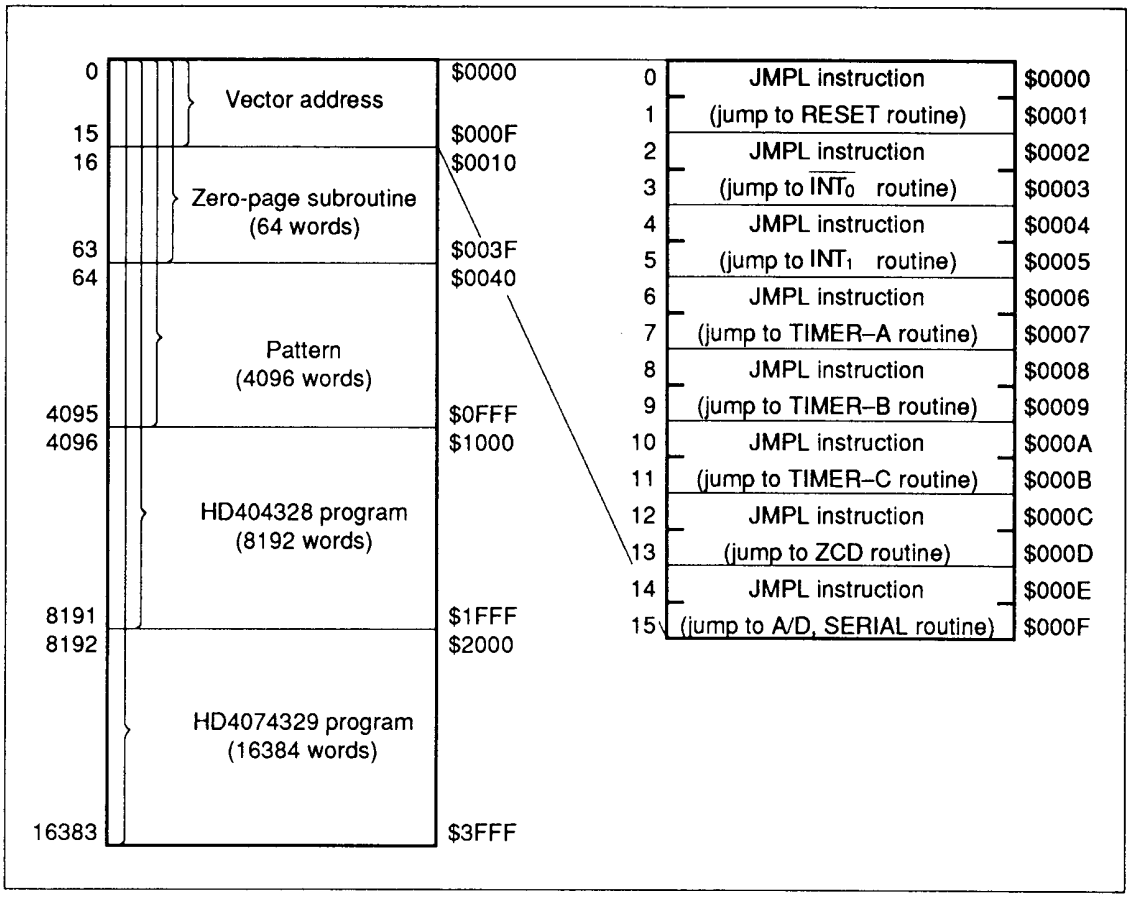
Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area (HD404328: $0000–$1FFF, HD4074329: $0000–$3FFF): Used for program coding.

RAM Memory Map

The MCU contains a 256-digit × 4-bit (HD404328) or 512-digit × 4-bit (HD4074329) RAM area consisting of a data area and a stack area. In addition, interrupt control bits and special registers are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figure 2 and described below.



Interrupt Control Bit Area and Register Flag Area ($000–$003, $020–$023): Used for interrupt control bits and the bit register (figure 3). This area can be accessed only by RAM bit manipulation instructions. In addition, note that the interrupt request flag cannot be set by software, the RSP bit is used only to reset the stack pointer, and the WDON flag can be set only by the SEM and SEMD instructions.

Special Function Register Area ($004–$01F, $024–$03F): Used as mode registers for external interrupts, serial interface, and timer/counters, and as data registers and as data control registers for I/O ports. As shown in figure 2, these registers can be classified into three types: write-only, read-only, and read/write. The SEM, SEMD, REM, and REMD instructions can be used for the LCD control register (LCR), but RAM bit manipulation instructions cannot be used for other registers.

LCD Data Area ($050–$067): Used for storing LCD data which is automatically output to LCD segments as display data. Data 1 lights the corresponding LCD segment; data 0 extinguishes it.

Data Area (HD404328: $040–$04F and $070–$11F, HD4074329: $070–$21F): The memory register (MR), which is 16 digits ($040–$04F) long, can be accessed by the LAMR and XMRA instructions. Its structure is shown in figure 4.

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status (ST), and carry (CA) at subroutine call (CAL, CALL) and interrupt servicing. This area can be used as a 16-nesting-level subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 4.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

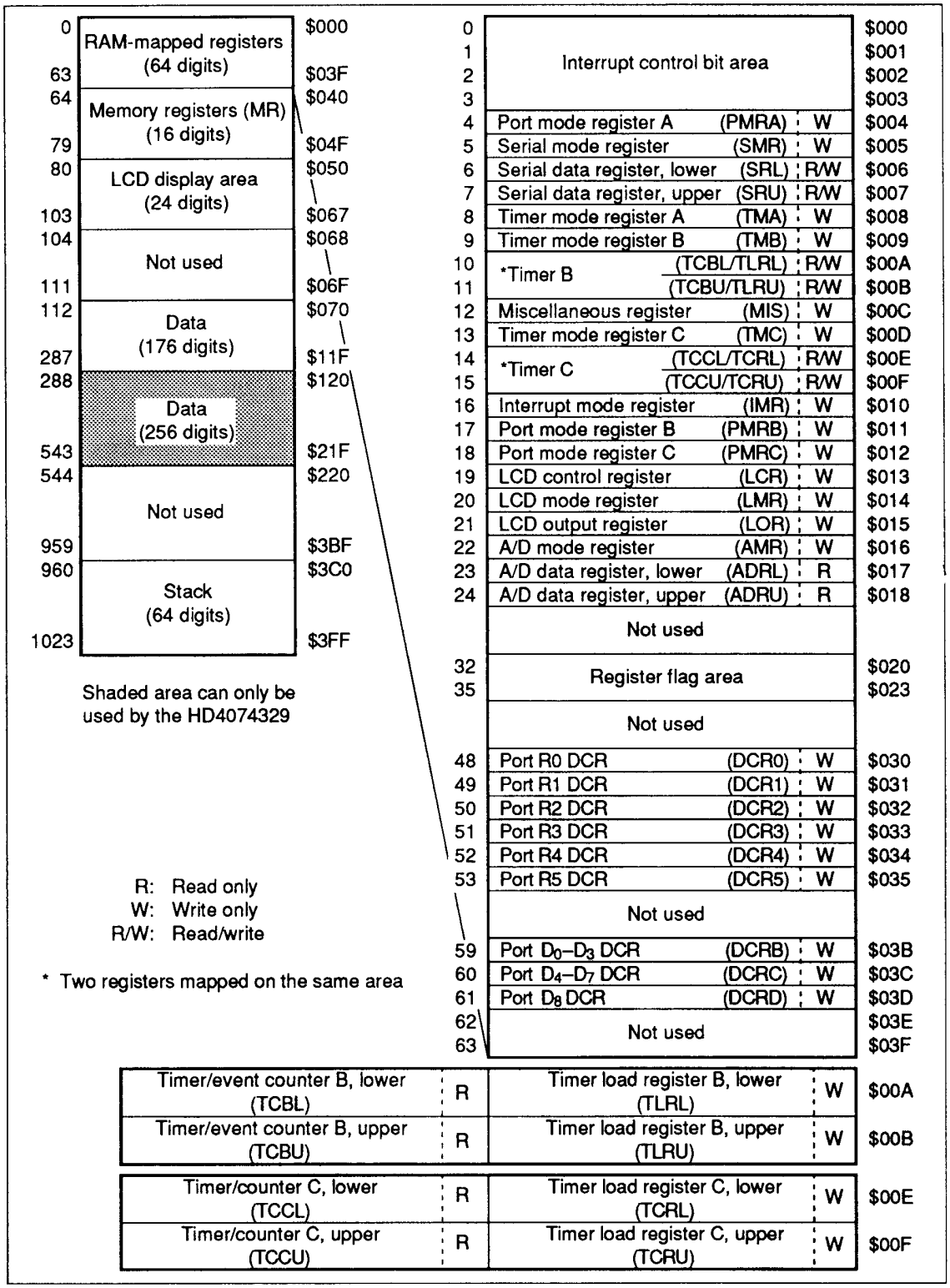


Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	I/E (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of INT_1)	IF1 (IF of INT_1)	$001
2	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	IMAD (IM of A/D)	IFAD (IF of A/D)	IMZC (IM of ZCD)	IFZC (IF of ZCD)	$003
32	DTON (Direct transfer on flag)	ADSF (A/D start flag)	WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
33	Reserved				$021
34					$022
35	IMS (IM of serial interface)	IFS (IF of serial interface)			$023

IF: Interrupt request flag
IM: Interrupt mask
I/E: Interrupt enable flag
SP: Stack pointer

Note: Bits in the interrupt control bit area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM or TMD instruction. Other instructions have no effect.
However, note that the IF cannot be set by the SEM or SEMD instruction. If the RSP bit or a non-existent bit is tested by the TM or TMD instruction, its status is undefined.
The WDON flag can only be used by the SEM or SEMD instruction (it is reset only by MCU reset).

Figure 3 Configuration of Interrupt Control Bit and Register Flag Area

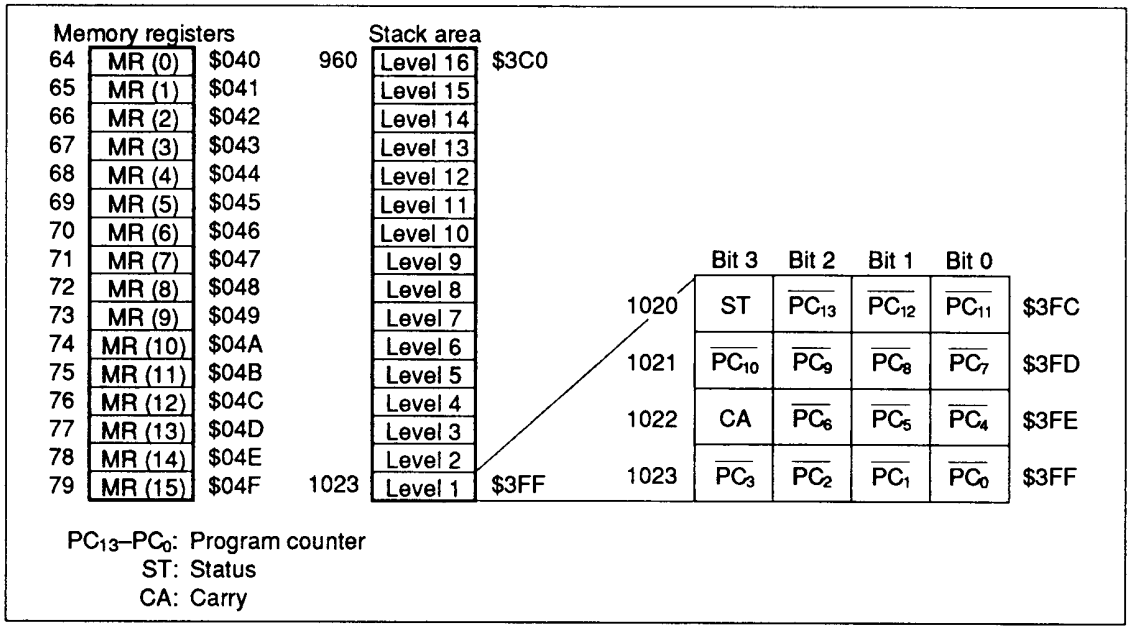


Figure 4 Configuration of Memory Register and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 5 and described below.

Accumulator (A), B Register (B): Four-bit registers used to hold results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during interrupt servicing and popped from the stack by the RTNI instruction—but not by the RTN instruction.

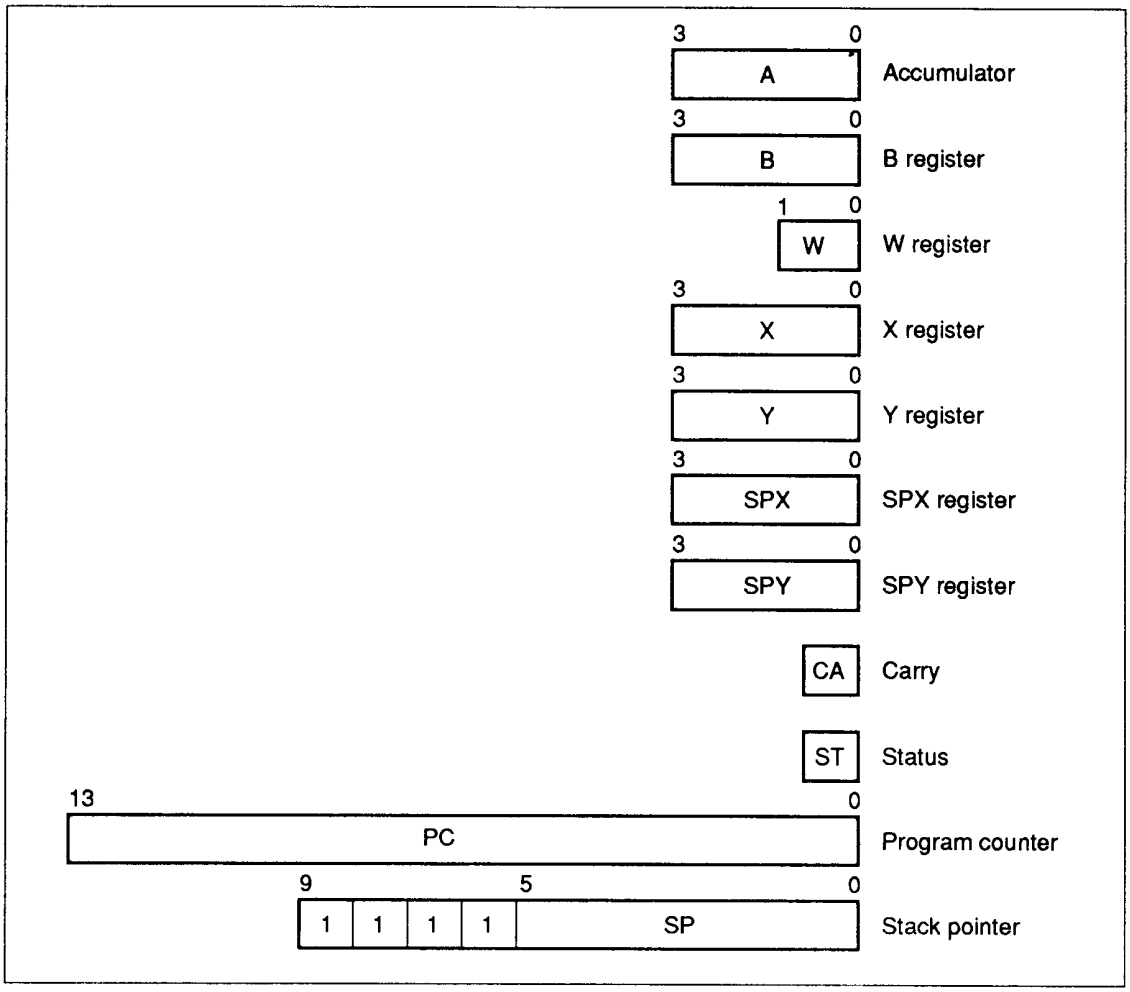


Figure 5 Registers and Flags

Status (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after a BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during interrupt servicing and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): 14-bit counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top four bits of the SP are fixed at 1111, a stack of up to 16 levels can be used.

The SP can be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a high-level voltage to the RESET pin. At power-on and when stop mode is canceled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize. During operation, RESET must be high for at least two instruction cycles.

Initial values after MCU reset are shown in table 1.

Interrupts

The MCU has eight interrupt sources: two external signals ($\overline{INT_0}$ and INT_1), three timer/counters (timer A, timer B, and timer C), serial interface (SERIAL), zero-crossing detection, and A/D converter.

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (I/E) controls the entire interrupt process.

Vector addresses are shared by serial interface and A/D converter interrupt causes, so software must first check which type of request has occurred.

Interrupt Control Bits and Interrupt Servicing: Locations $000 to $003 and $020 to $023 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (I/E) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 6, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the eight interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the I/E is 1 at that point, the interrupt is serviced. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 7 and an interrupt processing flowchart is shown in figure 8. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The I/E is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program a JMPL instruction at each vector address, to branch the program to the start address of the interrupt service program, and reset the IF by a software instruction within the interrupt service program.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(I/E)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCR)	All bits 0	Turns output buffer off (to high impedance)
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B	(PMRB)	0000	Refer to description of port mode register B
	Port mode register C	(PMRC)	0000	Refer to description of port mode register C
	Interrupt mode register	(IMR)	0000	Refer to description of interrupt mode register
Timer/ counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B	(TMB)	0000	Refer to description of timer mode register B
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Serial mode register	(SMR)	0000	Refer to description of serial mode register
	Prescaler S		$000	—
	Prescaler W		$00	—
	Timer/counter A	(TCA)	$00	—
	Timer/counter B	(TCB)	$00	—
	Timer/counter C	(TCC)	$00	—
	Timer load register B	(TLR)	$00	—
	Timer load register C	(TCR)	$00	—
	Octal counter		000	—
A/D	A/D mode register	(AMR)	0000	Refer to description of A/D mode register
LCD	LCD control register	(LCR)	000	Refer to description of LCD control register
	LCD mode register	(LMR)	0000	Refer to description of LCD duty cycle/clock control register
	LCD output register	(LOR)	0000	Refer to description of LCD output register
Bit register	Low speed on flag	(LSON)	0	Refer to description of low-power dissipation modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	A/D start flag	(ADSF)	0	Refer to description of A/D converter
	Direct transfer on flag	(DTON)	0	Refer to description of low-power dissipation modes
Miscellaneous register		(MIS)	0000	Refer to description of miscellaneous register

Note: The statuses of other registers and flags after MCU reset are as follows:

Item	Abbr.	Status After Cancellation of Stop Mode by MCU Reset	Status After all Other Types of Reset
Carry	(CA)	Pre-MCU-reset values are not guaranteed: values must be initialized by program	Pre-MCU-reset values are not guaranteed: values must be initialized by program
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data register	(SR)		
A/D data register	(ADRL, ADRU)		
RAM		Pre-MCU-reset (pre-STOP-instruction) values are retained	

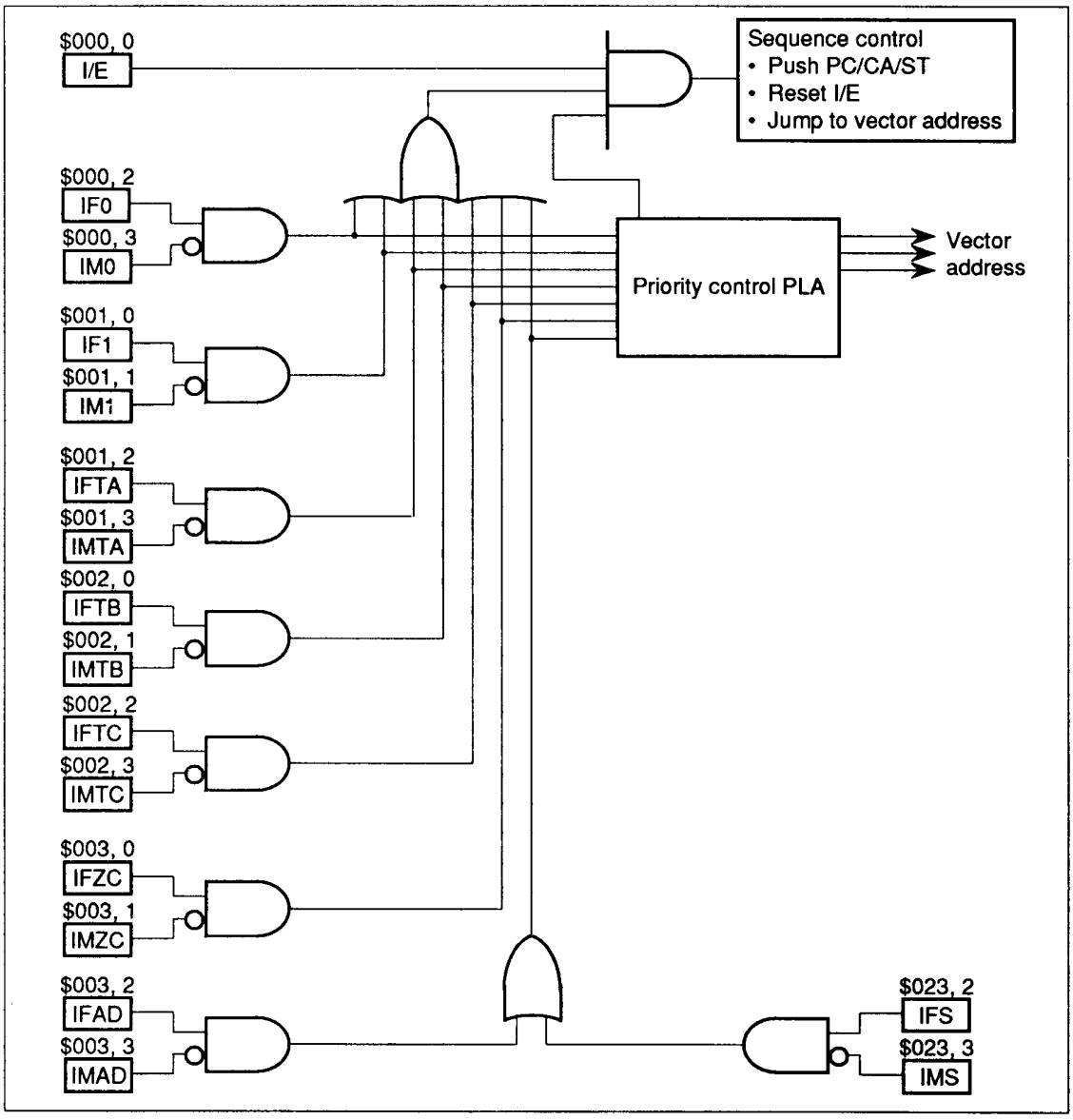


Figure 6 Block Diagram of Interrupt Control Circuit

Table 2 Vector Addresses and Interrupt Priorities

Reset, Interrupt	Priority	Vector Address
RESET		$0000
$\overline{INT_0}$	1	$0002
INT_1	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
ZCD	6	$000C
A/D, Serial	7	$000E

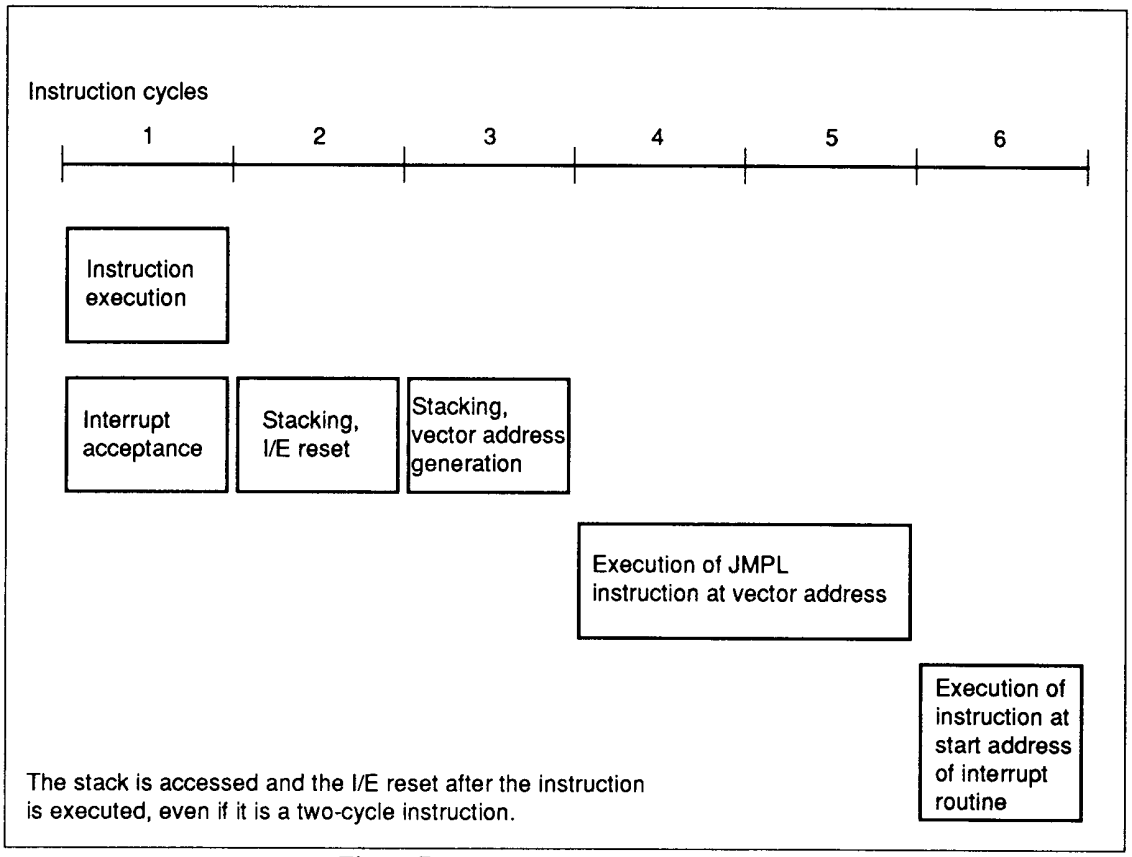


Figure 7 Interrupt Processing Sequence

Table 3 Interrupt Processing and Activation Conditions

Interrupt Control Bit	Interrupt Cause						
	$\overline{INT_0}$	INT_1	Timer A	Timer B	Timer C	ZCD	A/D, Serial
I/E	1	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0	0	0
IFTC · $\overline{IMTC}$	*	*	*	*	1	0	0
IFZC · $\overline{IMZC}$	*	*	*	*	*	1	0
IFAD · $\overline{IMAD}$ + IFS · $\overline{IMS}$	*	*	*	*	*	*	1

Note: Bits marked * can be either 0 or 1. Their values have no effect on operation.

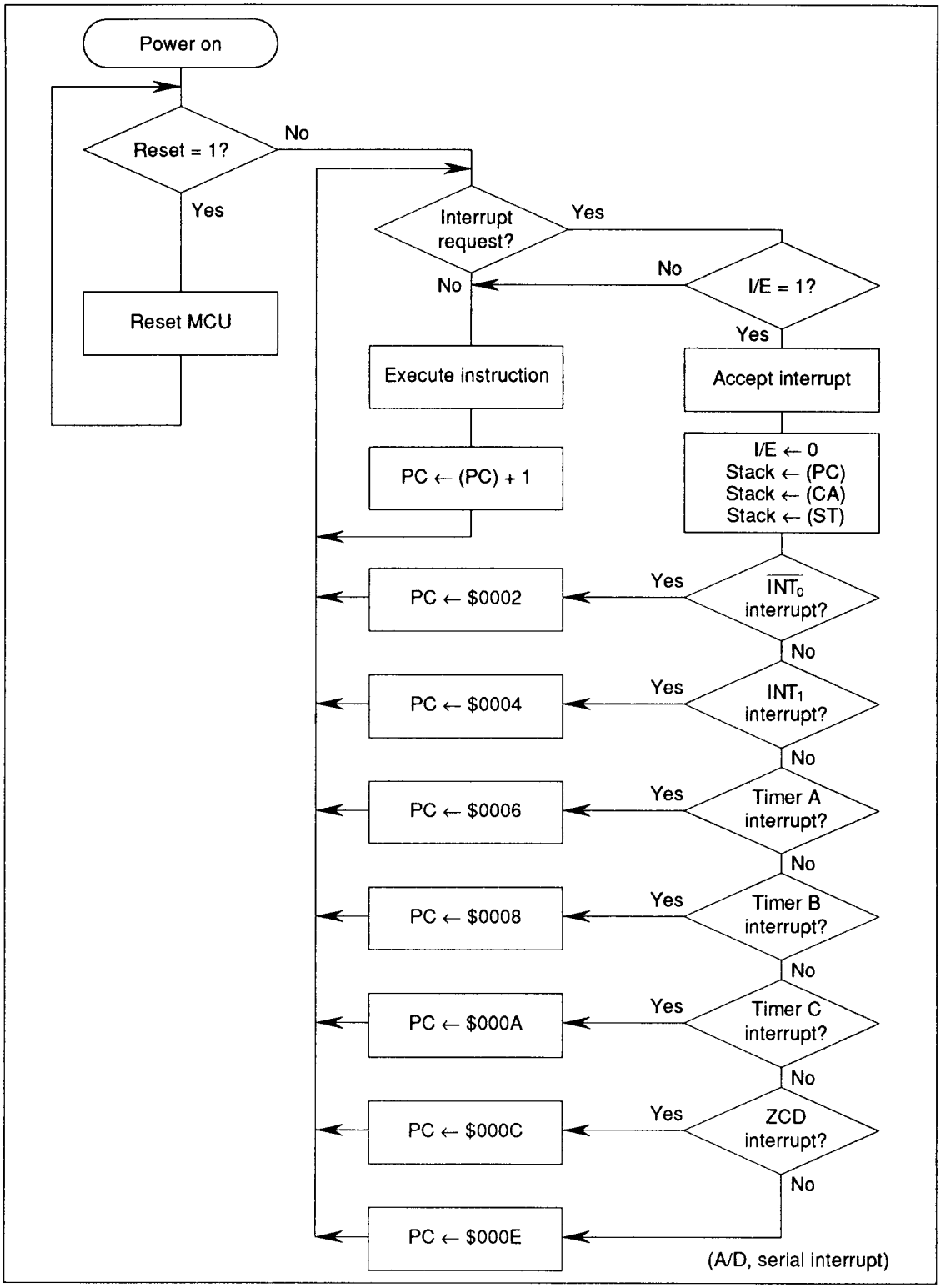


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (I/E: $000, 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as shown in table 4.

External Interrupts ($\overline{INT_0}$, INT_1): Specified by port mode register A (PMRA: $004).

External Interrupt Request Flags (IF0: $000, 2; IF1: $001, 0): Set at the rising or falling edges of the $\overline{INT_0}$ and INT_1 inputs, as shown in table 5.

IF0 is set at the falling edge of signals input to $\overline{INT_0}$, and IF1 is set at the rising and falling edges of signals input to INT_1. The INT_1 interrupt edge is selected by the interrupt mode register (IMR: $010), as shown in figure 9.

External Interrupt Masks (IM0: $000, 3; IM1: $001, 1): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as shown in table 6.

Table 4 Interrupt Enable Flag

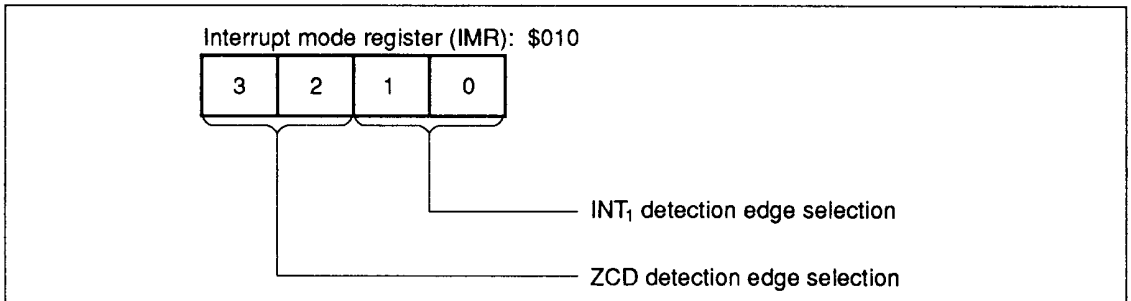
Interrupt Enable Flag (I/E)	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

Table 5 External Interrupt Request Flags

External Interrupt Request Flag (IF0, IF1)	Interrupt Request
0	No
1	Yes

Table 6 External Interrupt Masks

External Interrupt Mask (IM0, IM1)	Interrupt Request
0	Enabled
1	Disabled (masked)



IMR		ZCD Detection Edge
Bit 3	Bit 2	
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

IMR		INT_1 Detection Edge
Bit 1	Bit 0	
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

Figure 9 Interrupt Mode Register

Timer A Interrupt Request Flag (IFTA: $001, 2): Set by overflow output from timer A, as shown in table 7.

Timer A Interrupt Mask (IMTA: $001, 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as shown in table 8.

Timer B Interrupt Request Flag (IFTB: $002, 0): Set by overflow output from timer B, as shown in table 9.

Timer B Interrupt Mask (IMTB: $002, 1): Prevents (masks) an interrupt request caused by the timer B interrupt request flag, as shown in table 10.

Timer C Interrupt Request Flag (IFTC: $002, 2): Set by overflow output from timer C, as shown in table 11.

Timer C Interrupt Mask (IMTC: $002, 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as shown in table 12.

Zero-Crossing Interrupt Request Flag (IFZC: $003, 0): Set by a zero crossing of an AC input signal, as shown in table 13. The interrupt edge is selected by the interrupt mode register (IMR: $010), as shown in figure 9.

Zero-Crossing Interrupt Mask (IMZC: $003, 1): Prevents (masks) an interrupt request caused by the zero-crossing interrupt request flag, as shown in table 14.

Table 7 Timer A Interrupt Request Flag

Timer A Interrupt Request Flag (IFTA)	Interrupt Request
0	No
1	Yes

Table 8 Timer A Interrupt Mask

Timer A Interrupt Mask (IMTA)	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 9 Timer B Interrupt Request Flag

Timer B Interrupt Request Flag (IFTB)	Interrupt Request
0	No
1	Yes

Table 10 Timer B Interrupt Mask

Timer B Interrupt Mask (IMTB)	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 11 Timer C Interrupt Request Flag

Timer C Interrupt Request Flag (IFTC)	Interrupt Request
0	No
1	Yes

Table 12 Timer C Interrupt Mask

Timer C Interrupt Mask (IMTC)	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 13 Zero-Crossing Interrupt Request Flag

Zero-Crossing Interrupt Request Flag (IFZC)	Interrupt Request
0	No
1	Yes

Table 14 Zero-Crossing Interrupt Mask

Zero-Crossing Interrupt Mask (IMZC)	Interrupt Request
0	Enabled
1	Disabled (masked)

A/D Interrupt Request Flag (IFAD: $003, 2): Set at the completion of A/D conversion, as shown in table 15.

A/D Interrupt Mask (IMAD: $003, 3): Prevents (masks) an interrupt request caused by the A/D interrupt request flag, as shown in table 16.

Serial Interrupt Request Flag (IFS: $023, 2): Set when the octal counter counts the eighth transfer clock signal or when data transfer is discontinued by resetting the octal counter (table 17).

Serial Interrupt Mask (IMS: $023, 3): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as shown in table 18.

Table 15 A/D Interrupt Request Flag

A/D Interrupt Request Flag (IFAD)	Interrupt Request
0	No
1	Yes

Table 16 A/D Interrupt Mask

A/D Interrupt Mask (IMAD)	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 17 Serial Interrupt Request Flag

Serial Interrupt Request Flag (IFS)	Interrupt Request
0	No
1	Yes

Table 18 Serial Interrupt Mask

Serial Interrupt Mask (IMS)	Interrupt Request
0	Enabled
1	Disabled (masked)

Operating Modes

The MCU has five operating modes that are specified by how the clock is used. The functions available in each mode are listed in table 19, and operations are shown in table 20. Transitions between operating modes are shown in figure 10.

Active Mode: The MCU operates according to the clock generated by the system oscillators OSC_1 and OSC_2.

Table 19 Functions Available in Each Operating Mode

		Mode Name				
		Active	**Standby**	**Stop**	**Watch**	**Subactive[4]**
Activation method		RESET cancellation, interrupt request	SBY instruction	STOP instruction	TMA3 = 1 STOP instruction	$\overline{INT_0}$ or timer A interrupt request from watch mode
Status	System oscillator	Operating	Operating	Stopped	Stopped	Stopped
	Subsystem oscillator	Operating	Operating	Operating[1]	Operating	Operating
	Instruction execution (Φ_{CPU})	Operating	Stopped	Stopped	Stopped	Operating
	Interrupt function interrupt (Φ_{PER})	Operating	Operating	Stopped	Stopped	Operating[5]
	Clock function interrupt (Φ_{CLK})	Operating	Operating	Stopped	Operating[2]	Operating[2]
	RAM	Operating	Retained	Retained	Retained	Operating
	Registers/flags	Operating	Retained	Reset[6]	Retained	Retained/ operating
	I/O	Operating	Retained	Reset[3]	Retained	Operating
Cancellation method		RESET input, STOP/SBY instruction	RESET input, interrupt request	RESET input	RESET input, $\overline{INT_0}$ or timer A interrupt request	RESET input, STOP/SBY instruction

Notes:
1. To reduce current dissipation, stop all oscillation in external circuits.
2. Refer to the Interrupt Frame section for details.
3. Output pins are at high impedance.
4. Subactive mode is an optional function: specify it on the function option list.
5. The A/D converter does not operate.
6. Port mode register B retains the contents it had in active mode.

		System Clock (Φ_{CPU})	
		Operating	**Stopped**
Non-Timebase Peripheral Function Clock (Φ_{PER})	**Operating**	Active mode	Standby mode
		Subactive mode	
	Stopped	—	Watch mode (TMA3 = 1)
			Watch mode (TMA3 = 0)

Standby Mode: The MCU enters standby mode when a SBY instruction is executed from active mode. In this mode, the oscillators, interrupts, timer/counters, and serial interface continue to operate, but all instruction execution-related clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

Standby mode is terminated by a RESET input or an interrupt request. If it is terminated by RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and resumes, executing the next instruction after the SBY instruction. If the interrupt enable flag is 1, that interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 11.

Stop Mode: The MCU enters stop mode if a STOP instruction is executed in active mode when TMA3 = 0. In this mode, the system oscillator stops, which stops all MCU functions as well.

Stop mode is terminated by a RESET input as shown in figure 12. RESET must be high for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is canceled, all RAM contents are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

Watch Mode: The MCU enters watch mode if a STOP instruction is executed in active mode when TMA3 = 1, or if a STOP or SBY instruction is executed in subactive mode.

Watch mode is terminated by a RESET input or a timer A/$\overline{INT_0}$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer A/$\overline{INT_0}$ interrupt request, the MCU enters active mode if LSON is 0, or subactive mode if LSON is 1. Any interrupt request generated during the transition to active mode is delayed for half the interrupt frame period (t_{RC}), to give the oscillation time to stabilize, as shown in figure 13.

Table 20 Operations in Low-Power Dissipation Modes

Function	Stop Mode	Watch Mode	Standby Mode	Subactive Mode[3]
CPU	Reset	Retained	Retained	
RAM	Retained	Retained	Retained	
Timer A	Reset			
Timer B	Reset	Stopped		
Timer C	Reset	Stopped		
Serial interface	Reset	Stopped[4]		
LCD	Reset			
I/O	Reset[1]	Retained	Retained	
A/D	Reset	Stopped		Stopped
Zero-crossing detection	Stopped[5]	Stopped[5]		

Notes: 1. Output pins are at high impedance.
2. Shading means operating.
3. Subactive mode is an optional function specified on the function option list.
4. Transmission/reception is activated if a clock is input in external clock mode. (However, interrupts stop.)
5. The bias circuits still operate when the D8/ZCD/$\overline{EVENT}$ pin is set to ZCD.

Operation during mode transition is the same as that at standby mode cancellation (figure 11).

Subactive Mode: The CPU operates with a clock generated by the X1 and X2 oscillation circuits. Functions that can operate in subactive mode are listed in table 21. When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of LSON and DTON. The DTON flag can only be set in subactive mode; it is automatically reset after a transition to active mode.

Subactive mode is an optional function that the user must specify on the function option list.

Interrupt Frame: In watch and subactive modes, timer A and $\overline{INT_0}$ interrupts are generated in synchronism with the interrupt frame. Three interrupt frame lengths (T) can be selected by settings of the miscellaneous register, as shown in figure 14. The time from an interrupt strobe to interrupt request generation is the oscillation stabilization period (t_{RC}), as shown in figure 13.

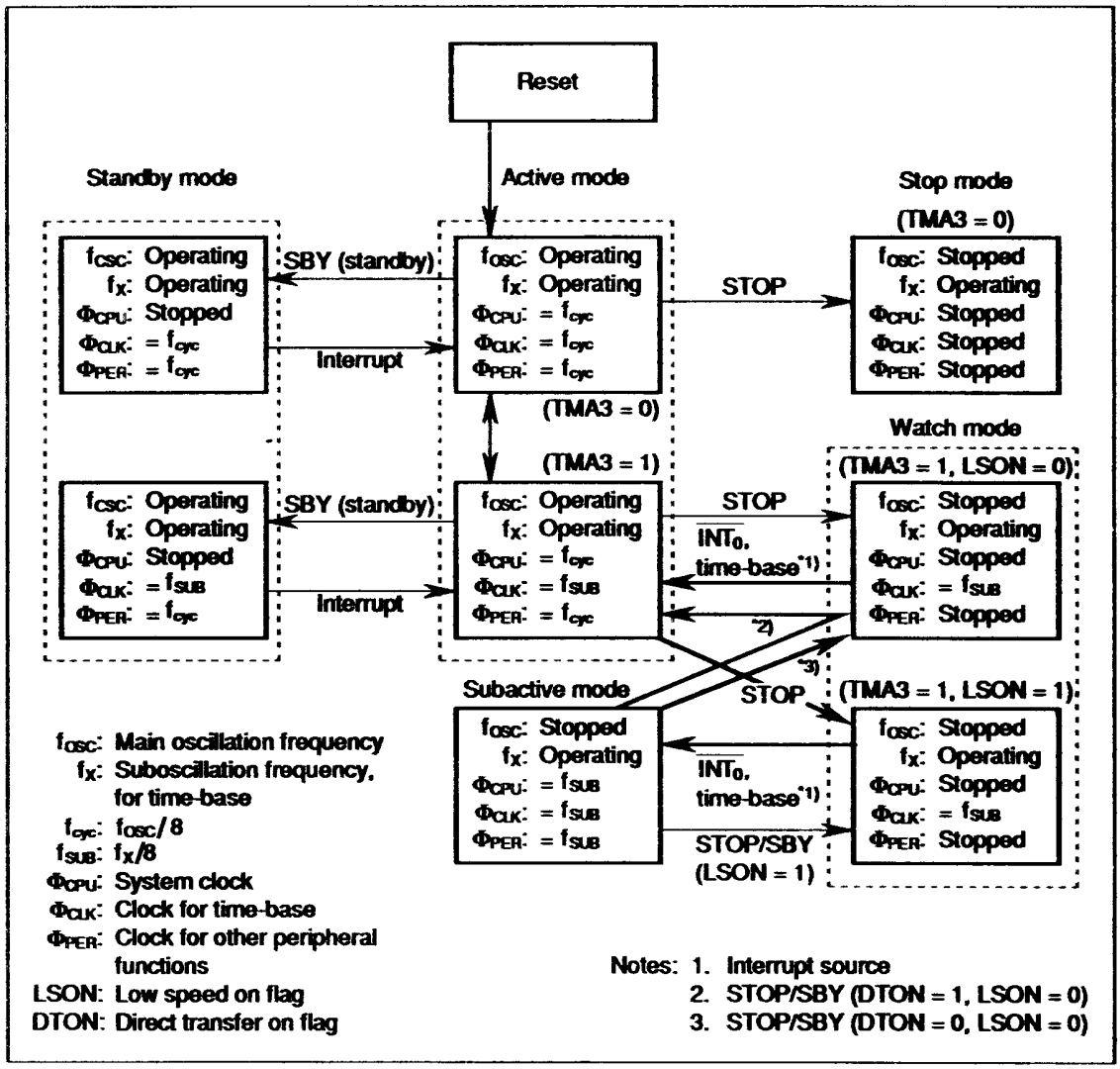


Figure 10 MCU Status Transitions

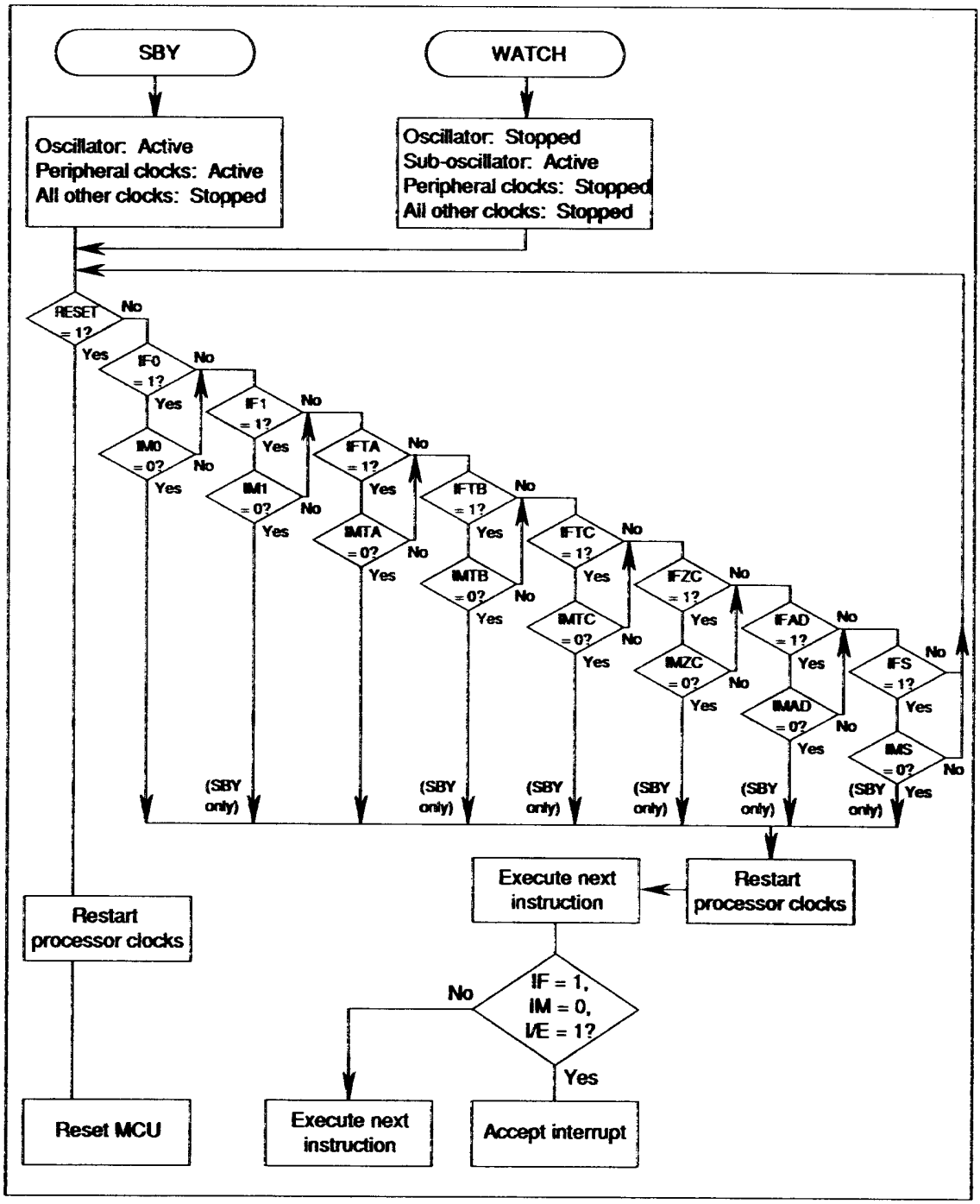


Figure 11 MCU Operation Flowchart

Operation during the transition from watch mode to active mode is the same as that at standby mode cancellation (figure 11).

MCU Operation Sequence: The MCU operates in the sequence shown in figures 15 to 17. It is reset by an asynchronous RESET input, regardless of its state.

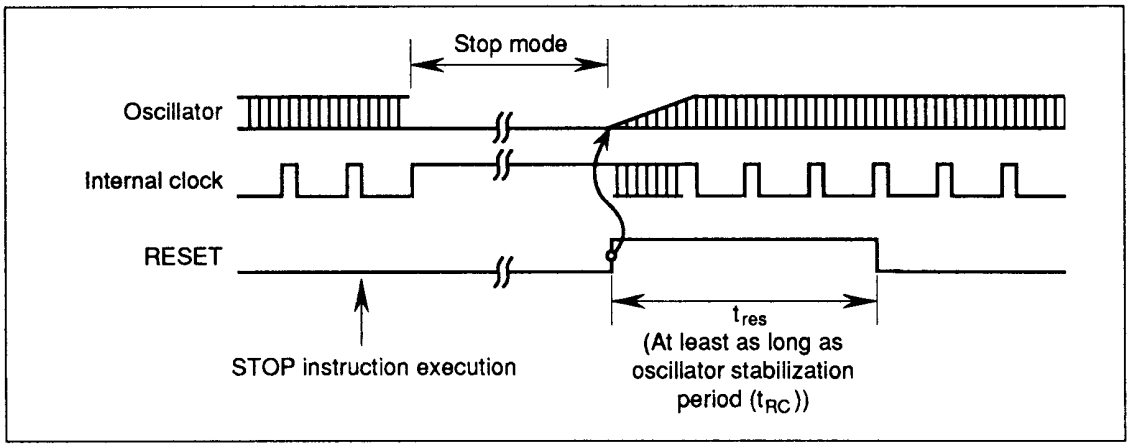


Figure 12 Timing of Stop Mode Cancellation

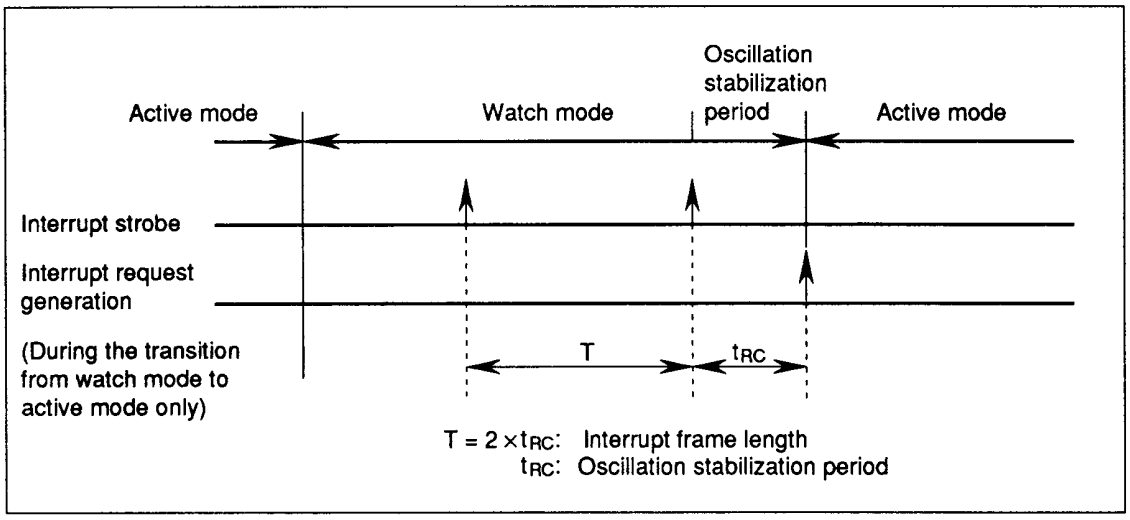
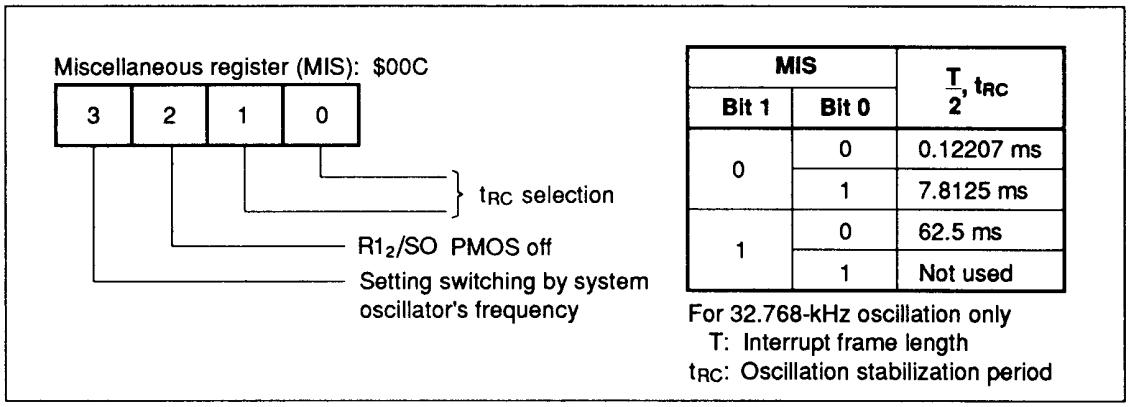


Figure 13 Interrupt Frame



MIS		T/2, tRC
Bit 1	Bit 0	
0	0	0.12207 ms
	1	7.8125 ms
1	0	62.5 ms
	1	Not used

For 32.768-kHz oscillation only
T: Interrupt frame length
tRC: Oscillation stabilization period

Figure 14 Miscellaneous Register

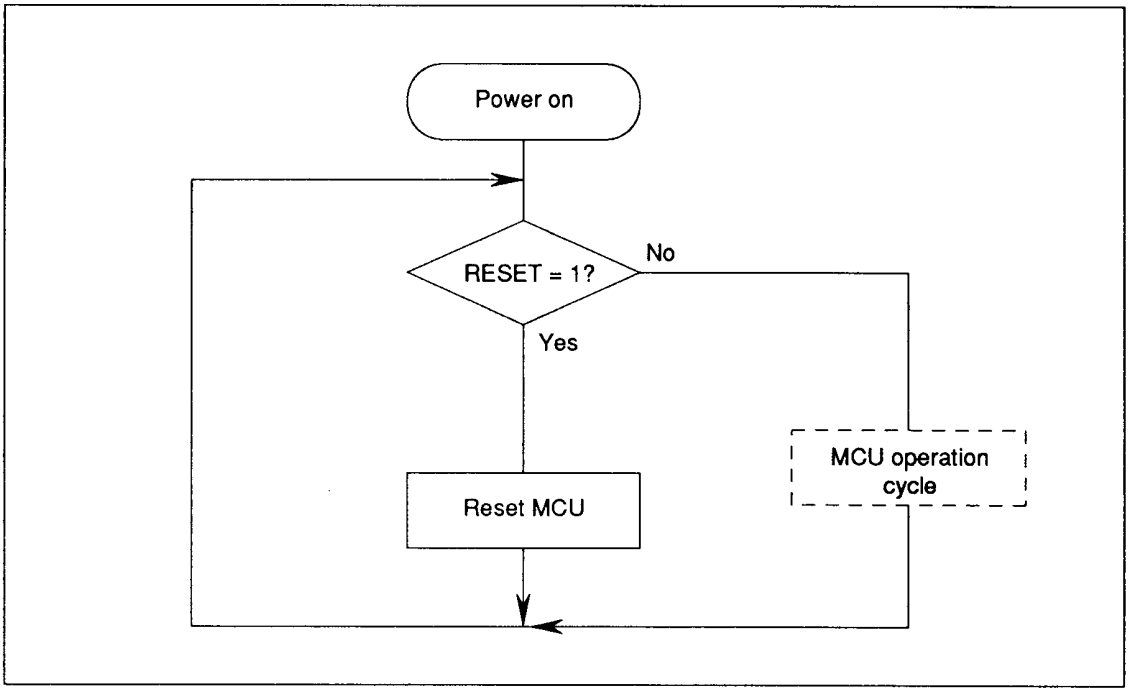


Figure 15 MCU Operating Sequence (power on)

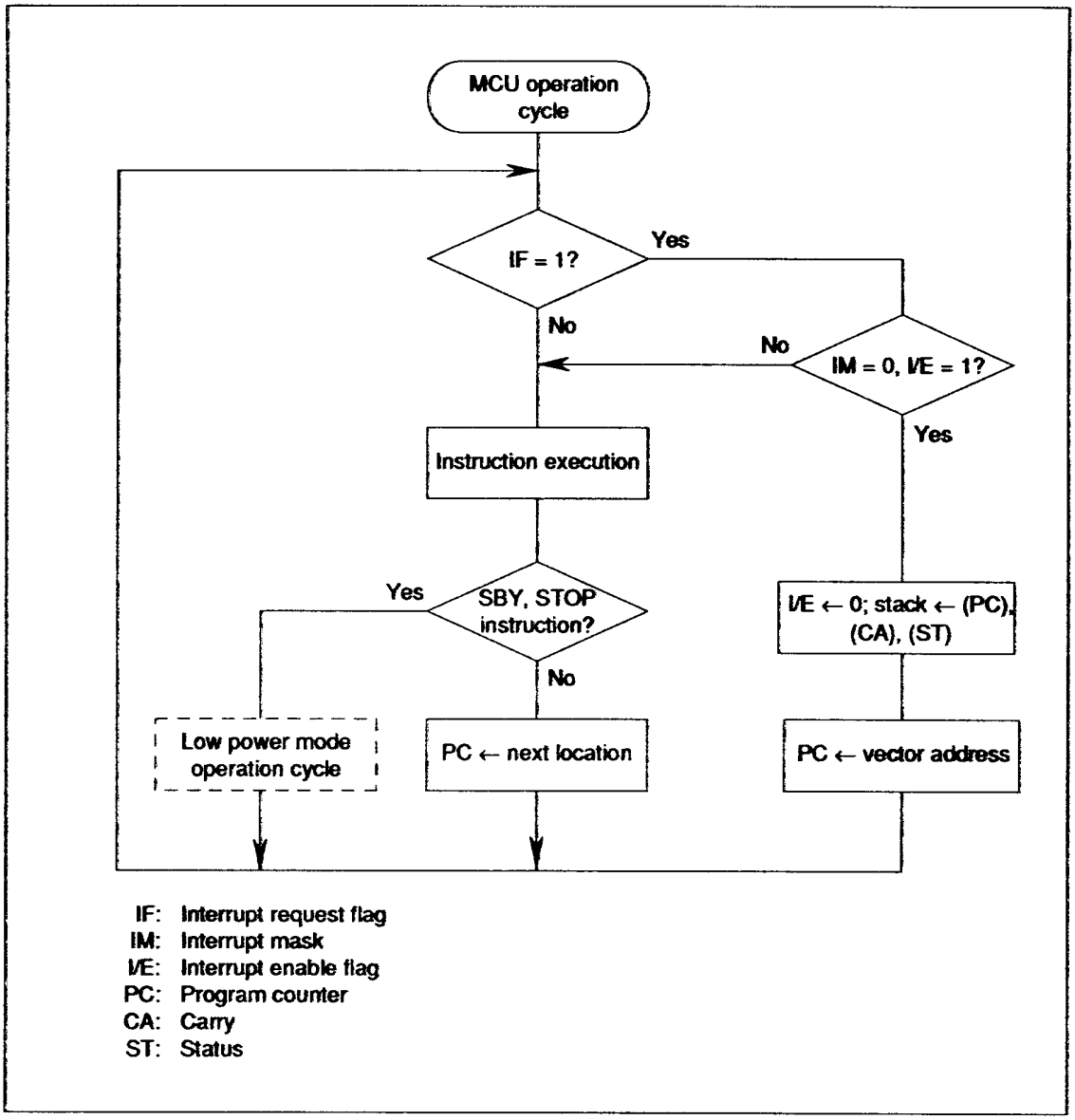


Figure 16 MCU Operating Sequence (MCU operation cycle)

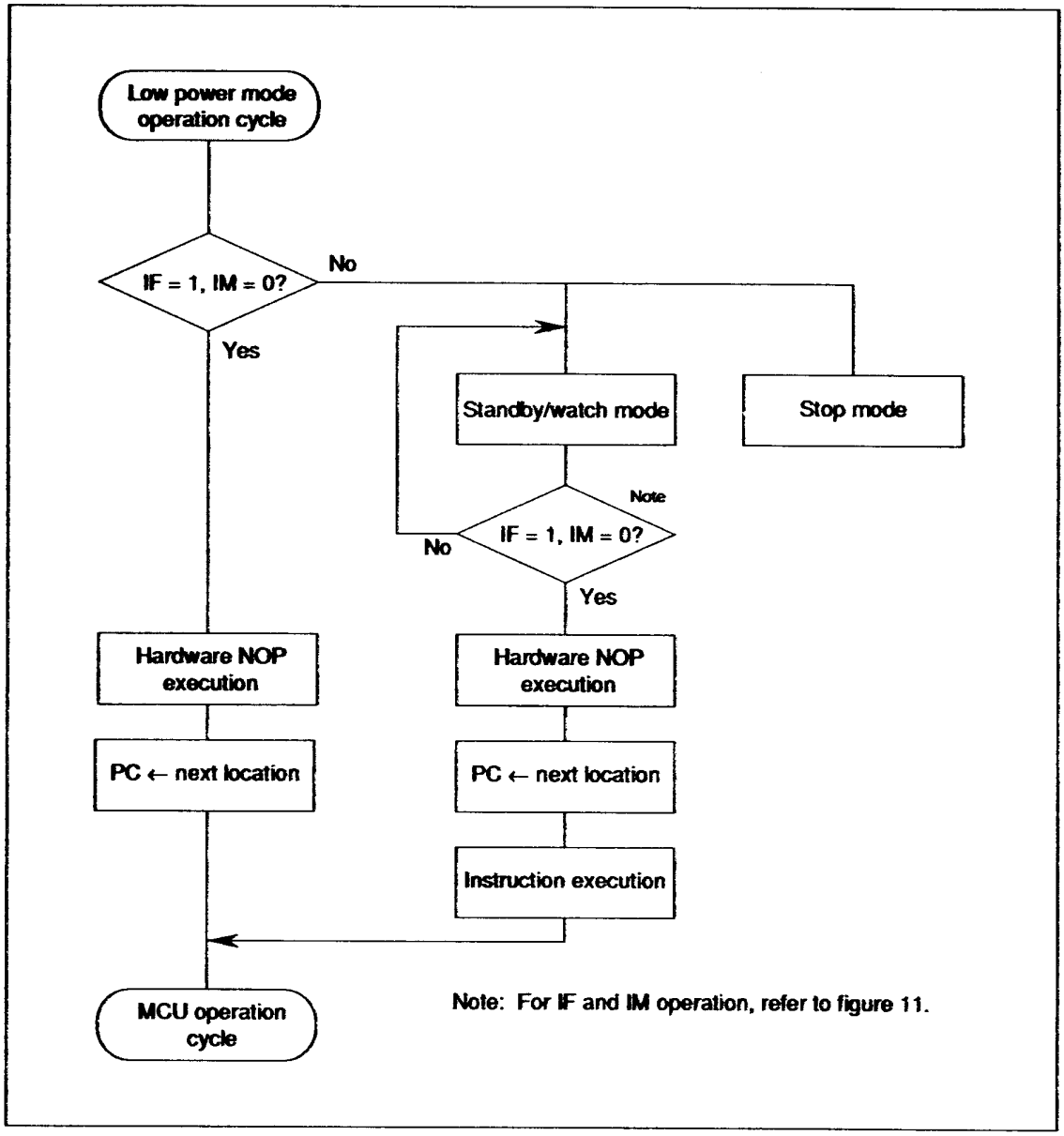
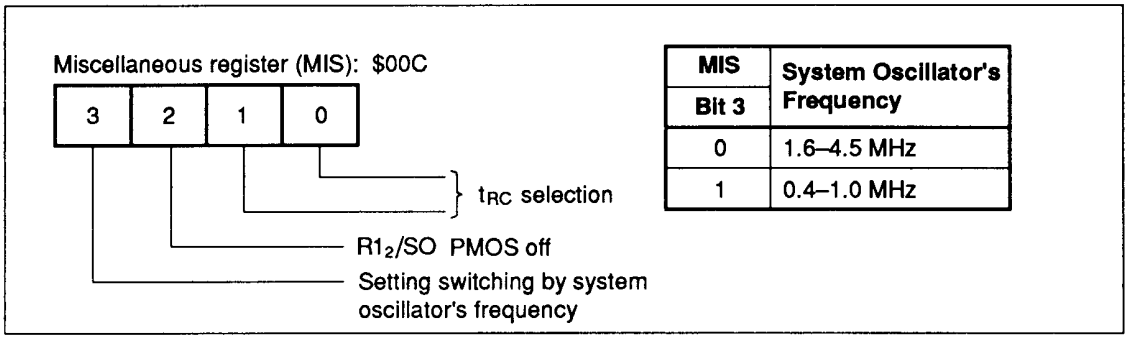


Figure 17 MCU Operating Sequence (low-power mode operation)

Internal Oscillator Circuit

A block diagram of the internal oscillator circuit is shown in figure 19. As shown in table 21, crystal and ceramic filter oscillators can be connected to OSC_1 and OSC_2, and a 32.768-kHz oscillator can be connected to X1 and X2. The system oscillator can also be operated by an external clock. Bit 3 of the miscellaneous register (MIS: $00C) must be set according to the frequency of the oscillator connected to OSC_1 and OSC_2.

Note: If the MIS register setting does not match the oscillator frequency, subsystems using 32-kHz oscillation will malfunction. Set the system oscillator frequency to anything outside the range of 1.0 to 1.6 MHz when using 32-kHz oscillation.



MIS Bit 3	System Oscillator's Frequency
0	1.6–4.5 MHz
1	0.4–1.0 MHz

Figure 18 Miscellaneous Register

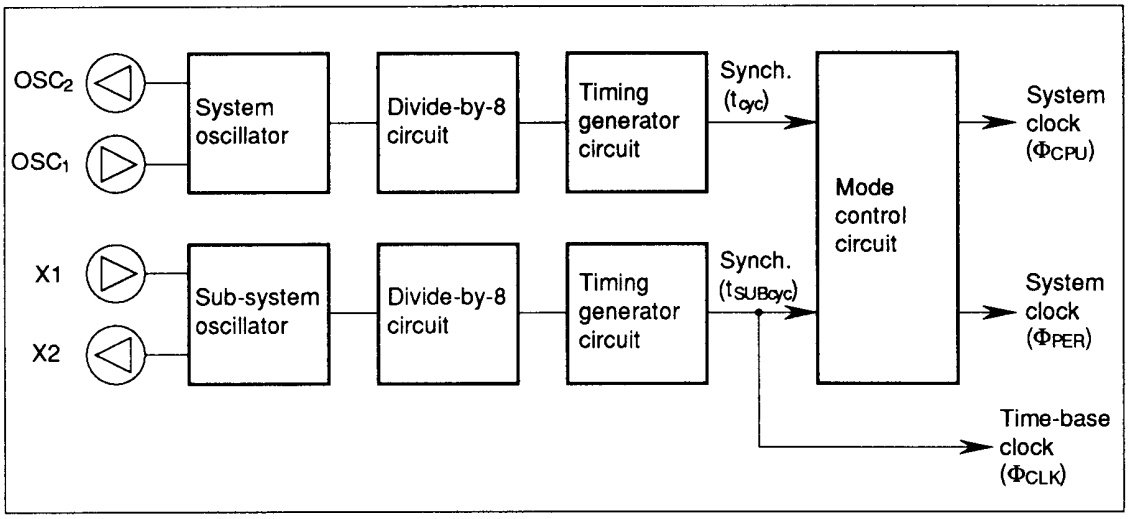


Figure 19 Internal Oscillator Circuit

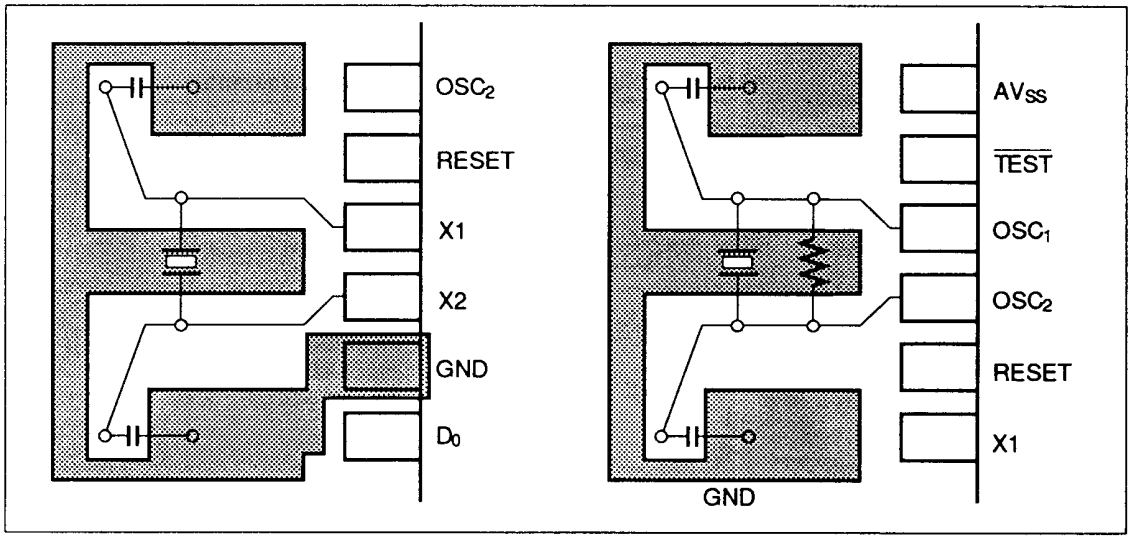
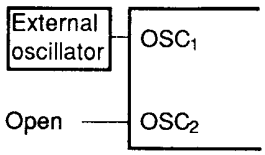
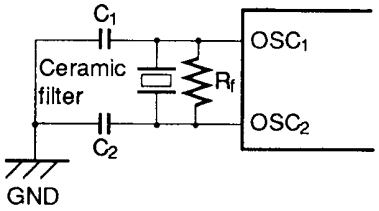
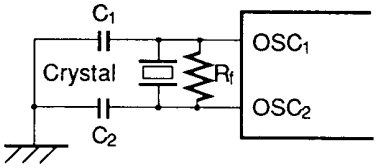
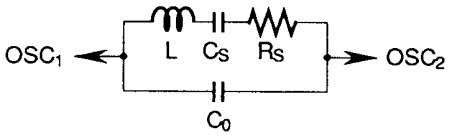
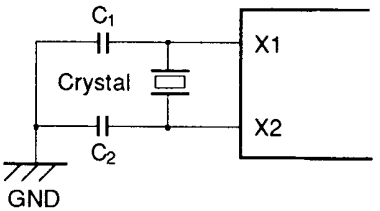
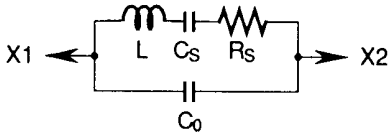


Figure 20 Typical Layouts of Crystal and Ceramic Filters

Table 21 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External Clock Operation (OSC_1, OSC_2)		
Ceramic Filter Oscillator (OSC_1, OSC_2)		Ceramic filter: CSA4.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%
Crystal Oscillator (OSC_1, OSC_2)	 AT cut parallel resonance crystal 	R_f: TBD $C_1 = C_2$ = TBD Crystal: Equivalent to circuit shown C_0 = 7 pF, max R_S = 100 Ω, max f = 1.0 to 4.5 MHz
Crystal Oscillator (X1, X2)	 	$C_1 = C_2$ = 15 pF ± 5% Crystal: 32.768 kHz, MX38T (Nippon Denpa) C_0 = 1.5 pF, typ R_S = 14 kΩ, typ

Notes:
1. Circuit constants differ with different types of crystal and ceramic filter oscillator, and with the stray capacitance of the board, so consult the manufacturer of the oscillator to determine the circuit parameters.
2. The wiring between the OSC_1 and OSC_2 pins (X1 and X2 pins) and the other elements should be as short as possible, and must not cross other wiring. Refer to figure 20.
3. If not using a 32.768-kHz crystal oscillator, fix the X1 pin to V_{CC} and leave the X2 pin open.

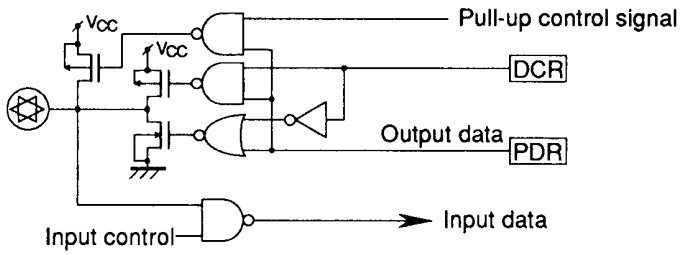
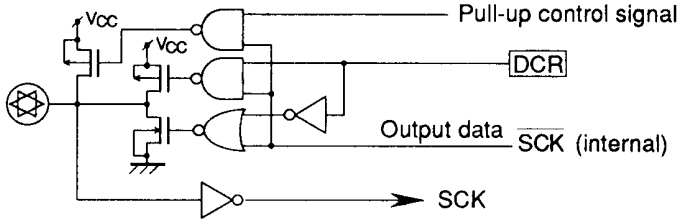
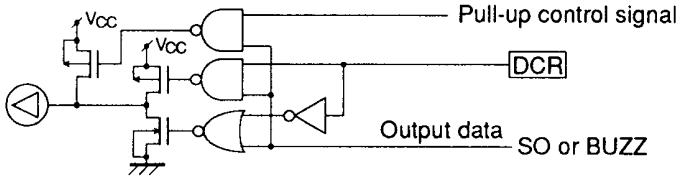
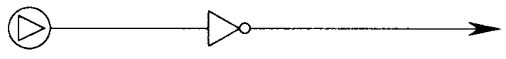
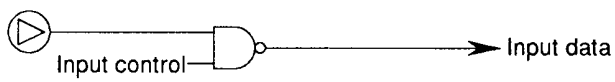
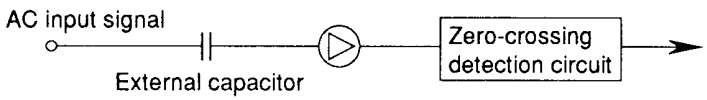
Input/Output

The MCU has 2 input pins and 33 input/output pins, 8 of the input/output pins being large-current pins (15 mA, max). A program-controlled pull-up MOS transistor is provided for each input/output pin.

The output buffer is turned on and off by the data control register (DCR) during input through an input/output pin.

I/O pin circuit types are shown in table 22.

Table 22 Circuit Configurations of I/O Pins

I/O Pin Type	Circuit	Applicable Pins
Common I/O Pin (with pull-up MOS transistor)		D_0–D_8 $R0_0$–$R0_3$ $R1_0$–$R1_3$ $R2_0$–$R2_3$ $R3_0$–$R3_3$ $R4_0$–$R4_3$ $R5_0$–$R5_3$
		$\overline{SCK}$
Output Pin (with pull-up MOS transistor)		SO BUZZ
Input Pin		$\overline{INT_0}$ SI $\overline{INT_1}$ $\overline{EVENT}$
		D_9 D_{10}
		ZCD

Note: For details of the $R1_2$ /SO pin, refer to note 2 of table 23.

D Ports (D_0–D_{10}): Consist of 9 input/output pins and 2 input pins. Ports D_0–D_7 are large-current I/O ports, D_8 is an ordinary input/output port, and D_9 and D_{10} are input-only ports. These ports are set by SED and SEDD instructions, reset by RED and REDD instructions, and tested by TD and TDD instructions.

The operating modes of ports D_8–D_{10} are set by bits 2 and 3 of port mode register A (PMRA) and bits 0 and 1 of port mode register B (PMRB), as shown in figure 21. The on/off status of the output buffer is controlled by D port data control registers (DCRB, DCRC, and DCRD) that are mapped to memory addresses.

R Ports: Accessed in 4-bit units. Data is input to these ports by LAR and LBR instructions and output from them by LRA and LRB instructions. The on/off status of the output buffers of the R ports are controlled by R port data control registers (DCR0–DCR5) that are mapped to memory addresses.

Pins $R1_0$–$R1_3$ are multiplexed with pins $\overline{SCK}$, SI, SO, and BUZZ, respectively. The operating modes of these pins are controlled by bit 3 of the serial mode register (SMR), bits 1 and 0 of port mode register A (PMRA), and bit 2 of port mode register C (PMRC), as shown in figure 21.

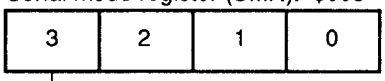
Pins R2–R5 are multiplexed with SEG1–SEG16. The functions of these pins must be specified by the LCD output register (LOR: $015).

Pull-up MOS Transistor Control: A program-controlled pull-up MOS transistor is provided for each input/output pin. The on/off status of all these transistors is controlled by bit 3 of port mode register C (PMRC), and the on/off status of an individual transistor can also be controlled by the port data register of the corresponding pin—enabling on/off control of that pin alone.

The configuration of the I/O buffer is shown in figure 22, and the configurations of various program-controlled I/O circuits are given in table 23.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ.

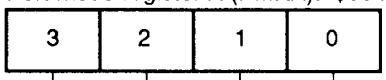
Serial mode register (SMR): $005



$R1_0/\overline{SCK}$ pin mode selection

SMR Bit 3	Port Selection
0	$R1_0$
1	$\overline{SCK}$

Port mode register A (PMRA): $004



$R1_2$/SO pin mode selection
$R1_1$/SI pin mode selection
$D_9/\overline{INT_0}$ pin mode selection
D_{10}/INT_1 pin mode selection

PMRA Bit 3	Port Selection	PMRA Bit 2	Port Selection	PMRA Bit 1	Port Selection	PMRA Bit 0	Port Selection
0	D_{10}	0	D_9	0	$R1_1$	0	$R1_2$
1	INT_1	1	$\overline{INT_0}$	1	SI	1	SO

Port mode register B (PMRB): $011

$D_8/ZCD/\overline{EVENT}$ pin mode selection

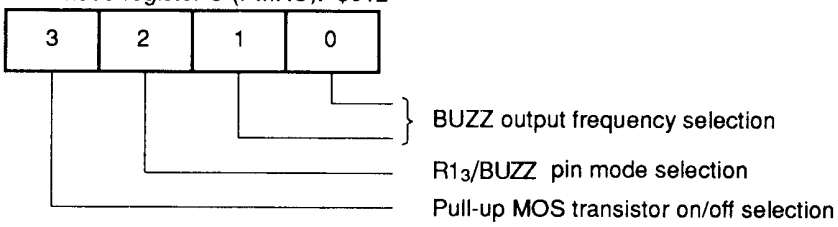
Not used

PMRB Bit 1	PMRB Bit 0	Port Selection
0	0	ZCD (low sensitivity)
	1	ZCD (high sensitivity)*
1	0	D_8
	1	$\overline{EVENT}$

* Becomes low sensitivity in subactive mode.

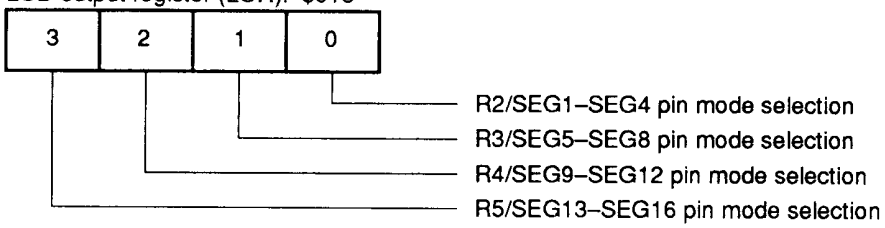
Figure 21 I/O Switching Mode Registers

Port mode register C (PMRC): $012



PMRC Bit 3	Pull-up MOS On/Off Selection	PMRC Bit 2	Port Selection
0	Off	0	$R1_3$
1	On	1	BUZZ

LCD output register (LOR): $015



LOR Bit 3	Port Selection	LOR Bit 2	Port Selection	LOR Bit 1	Port Selection	LOR Bit 0	Port Selection
0	R5	0	R4	0	R3	0	R2
1	SEG13–SEG16	1	SEG9–SEG12	1	SEG5–SEG8	1	SEG1–SEG4

Figure 21 I/O Switching Mode Registers (cont)

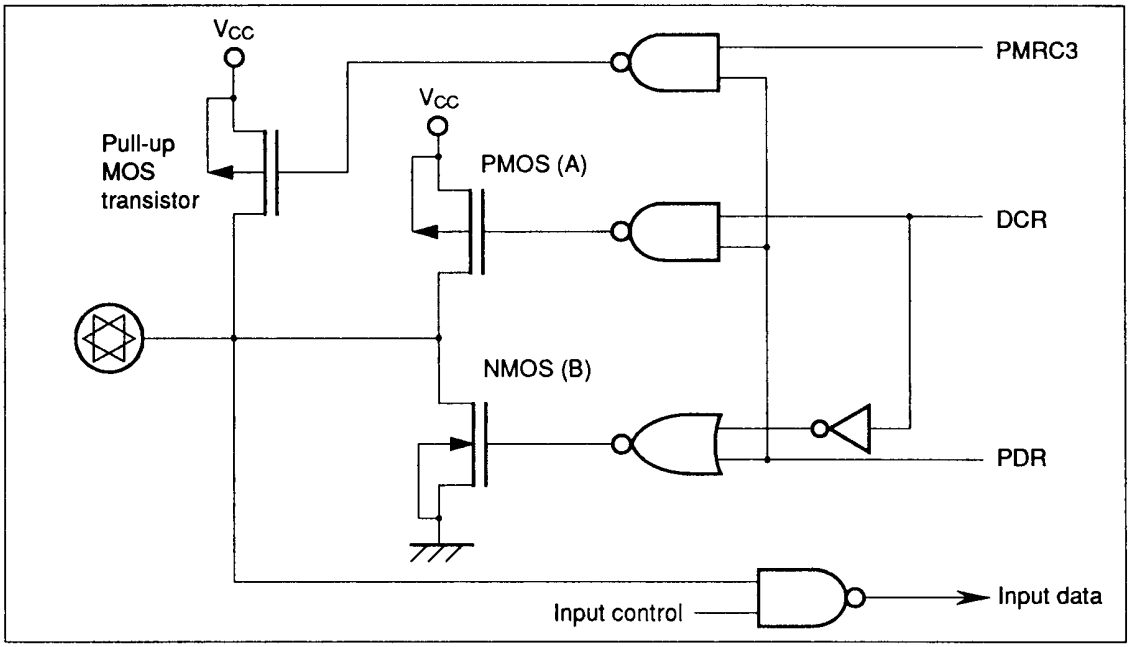


Figure 22 I/O Buffer Configuration

Table 23 Programmable I/O Circuits

PMRC, Bit 3		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS Buffer	PMOS (A)	Off	Off	Off	On	Off	Off	Off	On
	NMOS (B)	Off	Off	On	Off	Off	Off	On	Off
Pull-up MOS Transistor		Off	Off	Off	Off	Off	On	Off	On

Notes: 1. Various I/O methods can be selected by different combinations of settings of the above mode registers (PMRC3, DCR, PDR).

2. The PMOS (A) transistor of the $R1_2$ /SO pin can be turned off by setting bit 2 of the miscellaneous register (MIS) to 1.

MIS Bit 2	$R1_2$/SO Pin PMOS (A)
0	On
1	Off

3. The relationships between DCRs and pins are as shown on the right.

DCR	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCRB	D_3	D_2	D_1	D_0
DCRC	D_7	D_6	D_5	D_4
DCRD	—	—	—	D_8

Timers

The MCU has two prescalers (S and W) and three timer/counters (A, B, and C).

Prescaler S: Eleven-bit counter that inputs a system clock signal. After being initialized to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except in watch and stop modes, and at MCU reset. Of the prescaler S outputs, timer A input clock, timer B input clock, timer C input clock, and serial interface transmit clock are selected by timer mode register A (TMA), timer mode register B (TMB), timer mode register C (TMC), and the serial mode register (SMR).

Prescaler W: Five-bit counter that inputs the X1 input clock signal divided by eight. Prescaler W output can be selected as a timer A input clock by timer mode register A (TMA).

Timer A: Eight-bit timer that can be used as a clock time-base (figure 23). It is initialized to $00 and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow that sets the timer A interrupt request flag (IFTA: $001, 2) is generated, and timer A restarts from $00.

Timer A is used to generate regular interrupts (every 256 clocks) for measuring times between events. It can also be used as a clock time-base when bit 3 of timer mode register A (TMA) is set to 1. The timer is driven by the 32-kHz oscillator clock frequency divided by prescaler W, and the clock input to timer A is controlled by TMA. In this case, prescaler W and timer A can be initialized to $00 by software.

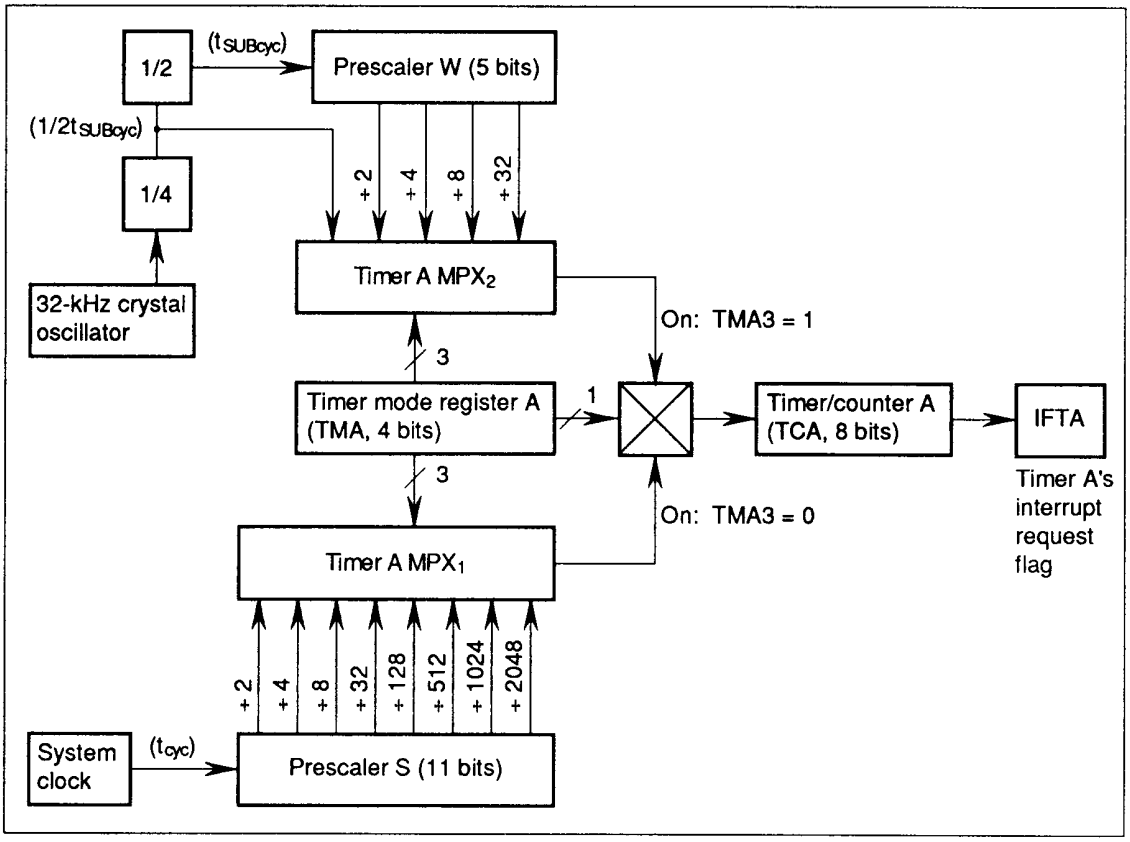


Figure 23 Block Diagram of Timer A

Timer B (TCBL and TLRL: $00A, TCBU and TLRU: $00B): Eight-bit write-only timer load register (TLRL and TLRU) and read-only timer/counter (TCBL and TCBU) located at the same addresses. The eight-bit configuration consists of lower and upper digits located at sequential addresses. A block diagram of timer B (and timer C) is shown in figure 24.

The timer/counter is initialized by writing to timer load register B (TLR). In this case, the lower nibble must be written to first. The contents of TLR are loaded into the timer/counter at the same time the upper nibble is written to, initializing the timer/counter. TLR is initialized to $00 by MCU reset.

The count of timer B is obtained by reading the timer/counter. In this case, the upper digit must be read first; the count is latched when the upper nibble is read.

An auto-reload function, input clock source, and prescaler division ratio of timer B depend on the state of timer mode register B (TMB). When an external event input is used as the input clock source of TMB, the D_8/ZCD/$\overline{\text{EVENT}}$ pin must be set to function as the ZCD or $\overline{\text{EVENT}}$ pin by setting port mode register B (PMRB: $011).

Timer B is initialized to the value set in TMB by software, and is then incremented by one by each clock input. If an input is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer B is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer B interrupt request flag (IFTB: $002, 0).

Timer C (TCCL and TCRL: $00E, TCCU and TCRU: $00F): Eight-bit write-only timer load register (TCRL and TCRU) and read-only timer/counter (TCCL and TCCU) located at the same addresses. The eight-bit configuration consists of lower and upper digits located at sequential addresses. The operation of timer C is basically the same as that of timer B.

The auto-reload function and prescaler division ratio of timer C depend on the state of timer mode register C (TMC). Timer C is initialized to the value set in TMC by software, then is incremented by one at each clock input. If an input is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer C is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer C interrupt request flag (IFTC: $002, 2).

Timer C also functions as a watchdog timer. If a program routine runs out of control and an overflow is generated while the watchdog on (WDON) flag is set, the MCU is reset. This error can be detected by having the program control timer C reset before timer C reaches $FF.

The WDON can only have 1 written to it; it is cleared to 0 only by MCU reset.

Timer Mode Register A (TMA: $008): Four-bit write-only register that controls timer A as shown in table 24.

Timer Mode Register B (TMB: $009): Four-bit write-only register that selects the auto-reload function, input clock source, and the prescaler division ratio as shown in table 25. It is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer B initialization set by writing to TMB must be done after a mode change becomes valid.

Timer Mode Register C (TMC: $00D): Four-bit write-only register that selects the auto-reload function and prescaler division ratio as shown in table 26. It is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer C initialization set by writing to TMC must be done after a mode change becomes valid.

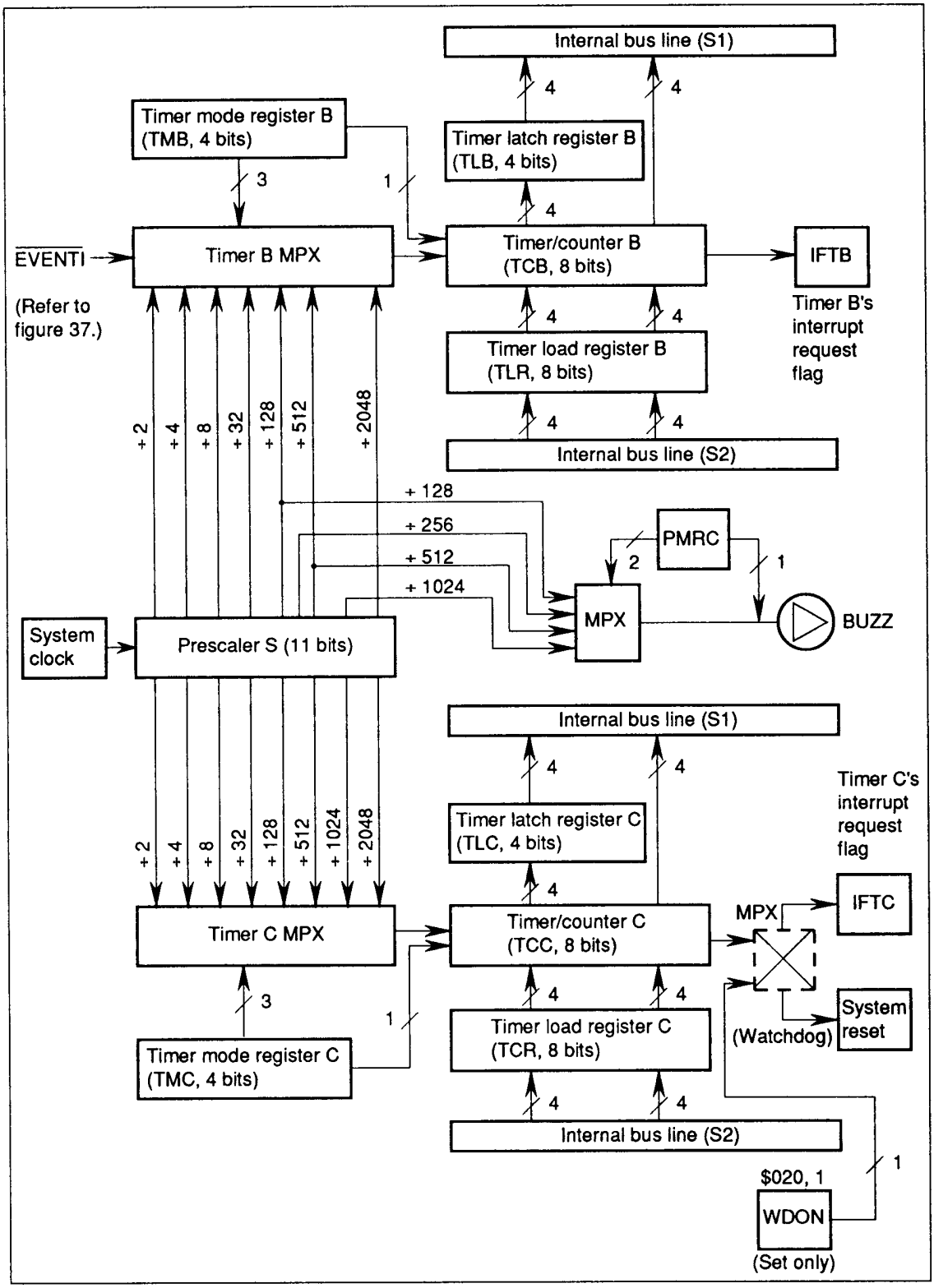


Figure 24 Block Diagram of Timers B and C

Table 24 Timer Mode Register A

TMA					
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Source Prescaler, Input Clock Period, Operating Mode**	
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{SUBcyc}	Time-base mode
			1	PSW, 16 t_{SUBcyc}	
		1	0	PSW, 8 t_{SUBcyc}	
			1	PSW, 2 t_{SUBcyc}	
	1	0	0	PSW, 1/2 t_{SUBcyc}	
			1	Do not use	
		1	0	PSW, TCA reset	
			1		

Notes:
1. t_{SUBcyc} = 244.14 µs (when 32.768-kHz crystal oscillator is used)
2. t_{cyc} = 1.9074 µs (when 4.1943-MHz crystal oscillator is used)
3. Timer counter overflow output period (seconds) = input clock period (seconds) × 256.
4. If PSW or TCA reset is selected while the LCD is operating, LCD operation halts (power switch goes off and all SEG and COM pins are grounded).
   When an LCD is connected for display, the PSW and TCA reset periods must be set in the program to the minimum.

Pulse Output

The MCU has a built-in pulse output function called BUZZ. The pulse frequency can be selected from the prescaler S's outputs, and the output frequency depends on the state of port mode register C (PMRC: $012), as shown in table 27. The duty cycle of the pulse output is fixed at 50%. When the pulse output function is used, the $R1_3$/BUZZ pin must be specified as BUZZ by PMRC.

Serial Interface

The MCU has a clock-synchronous serial interface which transmits and receives 8-bit data.

The serial interface consists of a serial data register (SR), serial mode register (SMR), port mode register A (PMRA), octal counter, and multiplexers, as shown in figure 25. The $R1_0/\overline{SCK}$ pin and the transmit clock are controlled by writing data to the SMR. The transmit clock shifts the contents of the SR, which can be read and written to by software, before transmission starts between two MCUs.

Table 25 Timer Mode Register B

TMB Bit 3	Auto Reload Function
0	Disabled
1	Enabled

TMB Bit 2	TMB Bit 1	TMB Bit 0	Input Clock Period/ Input Clock Source
0	0	0	2048 t_{cyc}
		1	512 t_{cyc}
	1	0	128 t_{cyc}
		1	32 t_{cyc}
1	0	0	8 t_{cyc}
		1	4 t_{cyc}
	1	0	2 t_{cyc}
		1	ZCD/$\overline{EVENT}$ (external event input)

Table 26 Timer Mode Register C

TMC Bit 3	Auto Reload Function
0	Disabled
1	Enabled

TMC Bit 2	TMC Bit 1	TMC Bit 0	Input Clock Period
0	0	0	2048 t_{cyc}
		1	1024 t_{cyc}
	1	0	512 t_{cyc}
		1	128 t_{cyc}
1	0	0	32 t_{cyc}
		1	8 t_{cyc}
	1	0	4 t_{cyc}
		1	2 t_{cyc}

Table 27 Port Mode Register C

PMRC Bit 1	PMRC Bit 0	Prescaler Division Ratio
0	0	÷ 1024
	1	÷ 512
1	0	÷ 256
	1	÷ 128

The serial interface is activated by the STS instruction. The octal counter is reset to 000 by this instruction, it starts counting at the falling edge of the transmit clock ($\overline{SCK}$), and it increments at the rising edge of the clock. A serial interrupt request flag is set when the eighth transmit clock signal is input (the serial interface is reset) or when serial transmission is discontinued (the octal counter is reset).

Serial Mode Register (SMR: $005): Four-bit write-only register that controls the $R1_0/\overline{SCK}$ pin, transmit clock, and prescaler division ratio as shown in figure 26. Writing to this register initializes the serial interface.

A write signal input to the serial mode register discontinues the input of the transmit clock to the serial data register and octal counter. Therefore, if a write is performed during data transmission, the octal counter is reset to 000 to stop transmission, and, at the same time, the serial interrupt request flag is set.

Write operations are valid from the second instruction execution cycle, so the STS instruction must be executed after at least two cycles have been executed. The serial mode register is initialized to $0 by MCU reset.

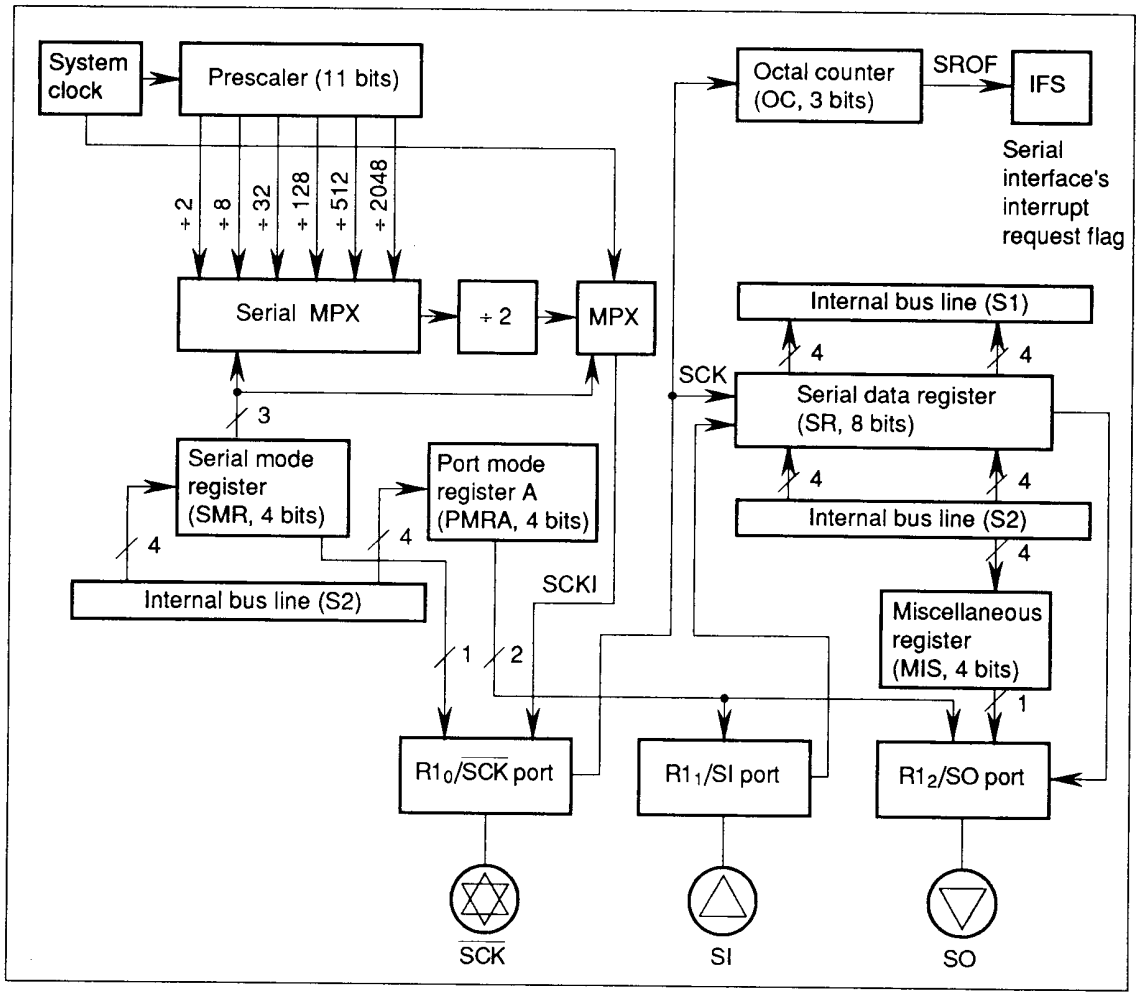


Figure 25 Block Diagram of Serial Interface

Serial Data Register (SRL: $006, SRU: $007): Eight-bit read/write register separated into upper and lower digits located at sequential addresses. Data in this register is output from the SO pin, LSB first, in synchronism with the falling edge of the transmit clock; and data is input, LSB first, through the SI pin at the rising edge of the transmit clock. Input/output timing is shown in figure 27.

Data cannot be read or written during serial data transmission. If a read/write occurs during transmission, the accuracy of the resultant data cannot be guaranteed.

Selecting and Changing Operating Mode: Table 28 lists the serial interface's operating modes. To select an operating mode, use one of these combinations of PMR and SMR settings; to change the operating mode, always initialize the serial interface internally by writing data to the SMR.

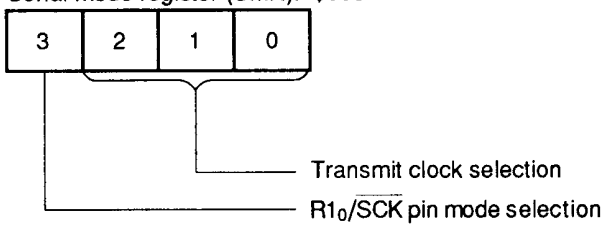
Serial Interface Operation: Three operating modes are provided for the serial interface; transitions between them are shown in figure 28.

In STS wait state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed, the serial interface enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal clock, shifts the serial clock register, and activates serial transmission. However, note that if clock output mode is selected, the transmit clock is continuously output but data is not transmitted.

During transmission, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters transmit clock wait state. If the state changes from transmit to another state, the serial interrupt request flag is set by the octal counter reaching 000.

Serial mode register (SMR): $005



SMR Bit 3	R1₀/SCK Pin
0	R1₀ port input pin
1	SCK input or output pin

SMR Bit 2	SMR Bit 1	SMR Bit 0	R1₀/SCK Pin	Clock Source	Prescaler Division Ratio	Transmit Clock Period
0	0	0	SCK output	Prescaler	÷ 2048	4096 t_{cyc}
		1	SCK output	Prescaler	÷ 512	1024 t_{cyc}
	1	0	SCK output	Prescaler	÷ 128	256 t_{cyc}
		1	SCK output	Prescaler	÷ 32	64 t_{cyc}
1	0	0	SCK output	Prescaler	÷ 8	16 t_{cyc}
		1	SCK output	Prescaler	÷ 2	4 t_{cyc}
	1	0	SCK output	System clock	—	1 t_{cyc}
		1	SCK input	External clock	—	—

Note: t_{cyc} = 1.9074 µs (with 4.1943–MHz crystal oscillator used at 1/8 division ratio)

Figure 26 Serial Mode Register

In this state, if the internal clock has been selected, the transmit clock is output in answer to the execution of the STS instruction, but serial transmission is inhibited after the eighth clock is output.

If port mode register A (PMRA) is written to in transmit clock wait state or during transmission, the serial mode register (SMR) must be written to, to initialize the serial interface. The serial interface then enters STS wait state.

If the serial interface shifts from transmission state to another state, the octal counter returns to 000, setting the serial interrupt request flag.

Transmit Clock Error Detection: The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transmission. A transmit clock error of this type can be detected as shown in figure 29.

If more than eight transmit clocks are input in transmit clock wait state, the serial interface's state changes to transmission, transmit clock wait, then back to transmission.

If the serial interface is set to STS wait state by writing data to the SMR after the serial interrupt request flag has been reset, the flag is set again.

Note on Use: The serial interrupt request flag might not be set if the status is changed from transfer by the execution of an SMR write or STS instruction during the first period that the transmit clock is low. To prevent this, program a check that the $\overline{SCK}$ pin is at 1 (by executing an input instruction for the R1 port) before the execution of an SMR write or STS instruction, to ensure that the serial interrupt request flag is set.

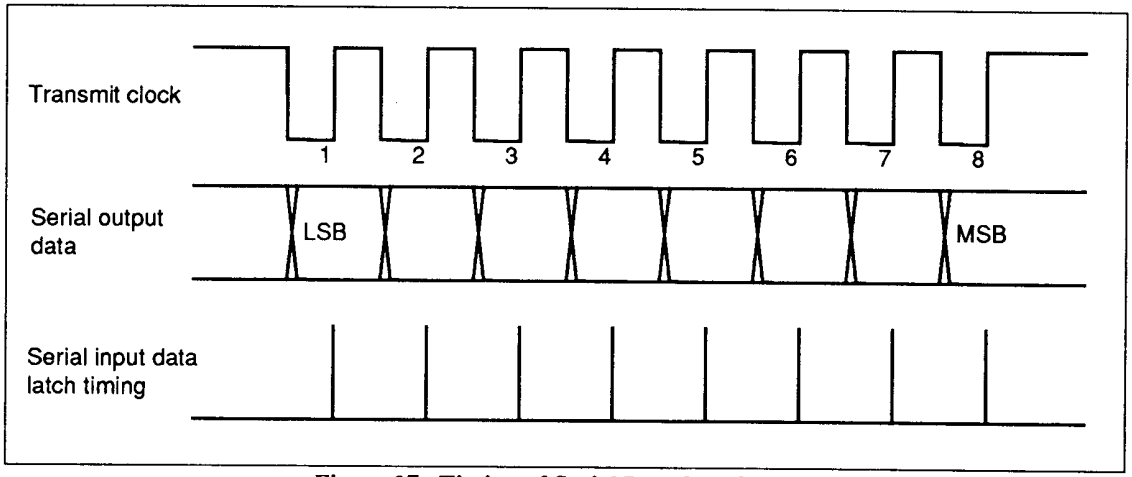


Figure 27 Timing of Serial Interface Output

Table 28 Serial Interface Operating Modes

SMR		PMRA	
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

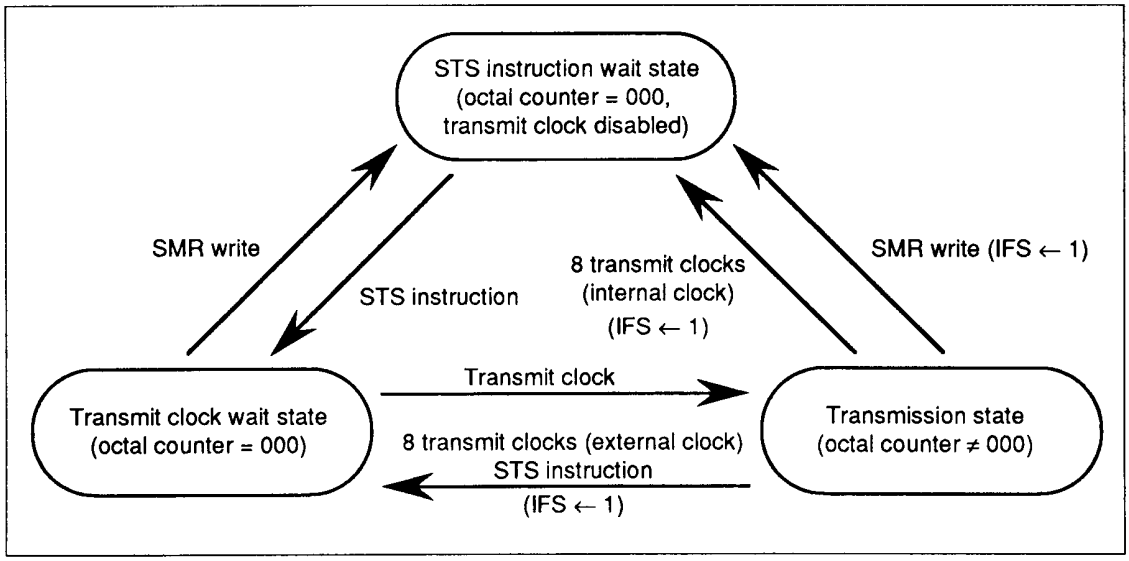


Figure 28 Serial Interface Mode Transitions

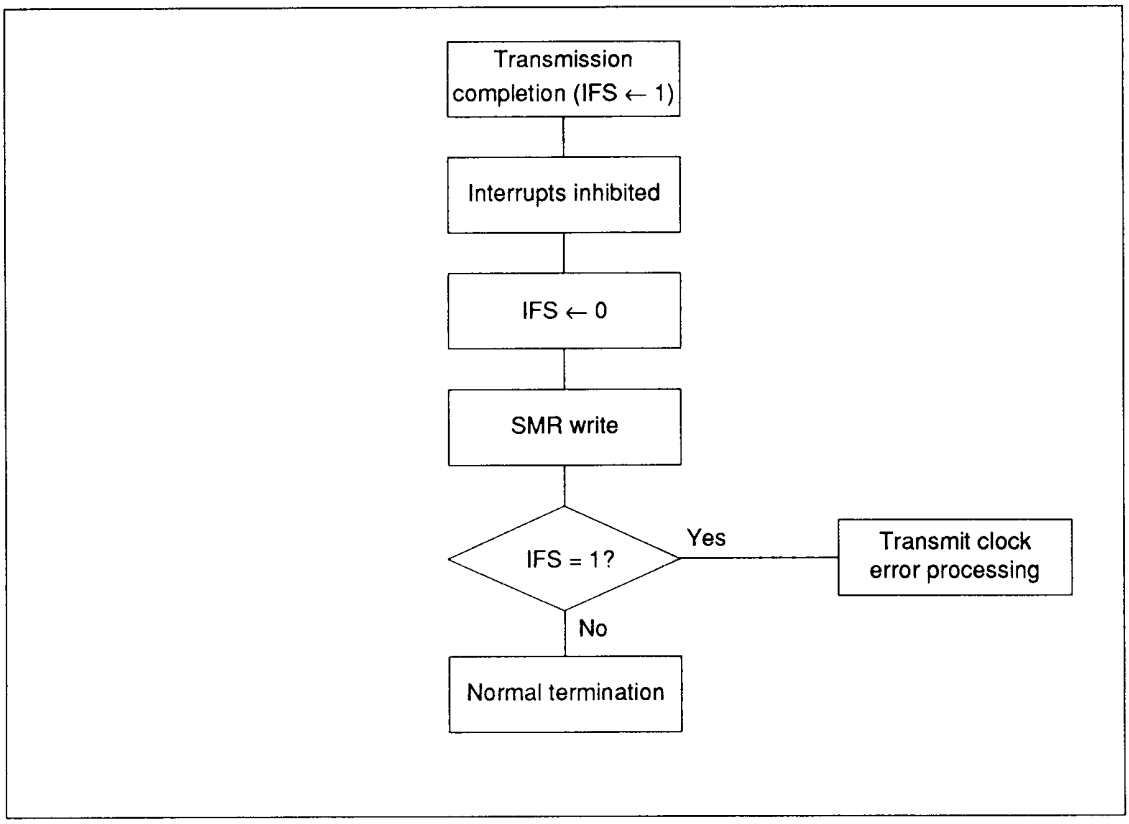


Figure 29 Transmit Clock Error Detection

A/D Converter

The MCU has a built-in A/D converter that uses a sequential comparison method with a resistor ladder. It can measure four analog inputs with an eight-bit resolution. As shown in the block diagram of figure 30, the A/D converter has a four-bit A/D mode register, a one-bit A/D start flag, and a four-bit plus four-bit A/D data register.

A/D Mode Register (AMR: $016): Four-bit write-only register which selects the A/D conversion period and indicates analog input pin information. Bit 0 of the AMR selects the A/D conversion period, and bits 2 and 3 select a channel, as shown in figure 31.

A/D Start Flag (ADSF: $020, 2): One-bit flag that initiates A/D conversion when 1 is written to it. At the completion of A/D conversion, the converted data is stored in the A/D data register and the ADSF is cleared. Refer to figure 31.

Note: Use the SEM and SEMD instructions to write data to the ADSF, but make sure that the ADSF is not written to during A/D conversion.

A/D Data Register (ADRL: $017, ADRU: $018): Eight-bit read-only register that is not cleared by a reset. Note that data read from this register during A/D conversion cannot be guaranteed. After the completion of A/D conversion, the resultant eight-bit data is held in this register, as shown in figure 32, until the start of the next conversion.

Note on Use: The contents of the A/D data register are not guaranteed during A/D conversion. To ensure that the A/D converter operates stably, do not execute port output instructions during A/D conversion.

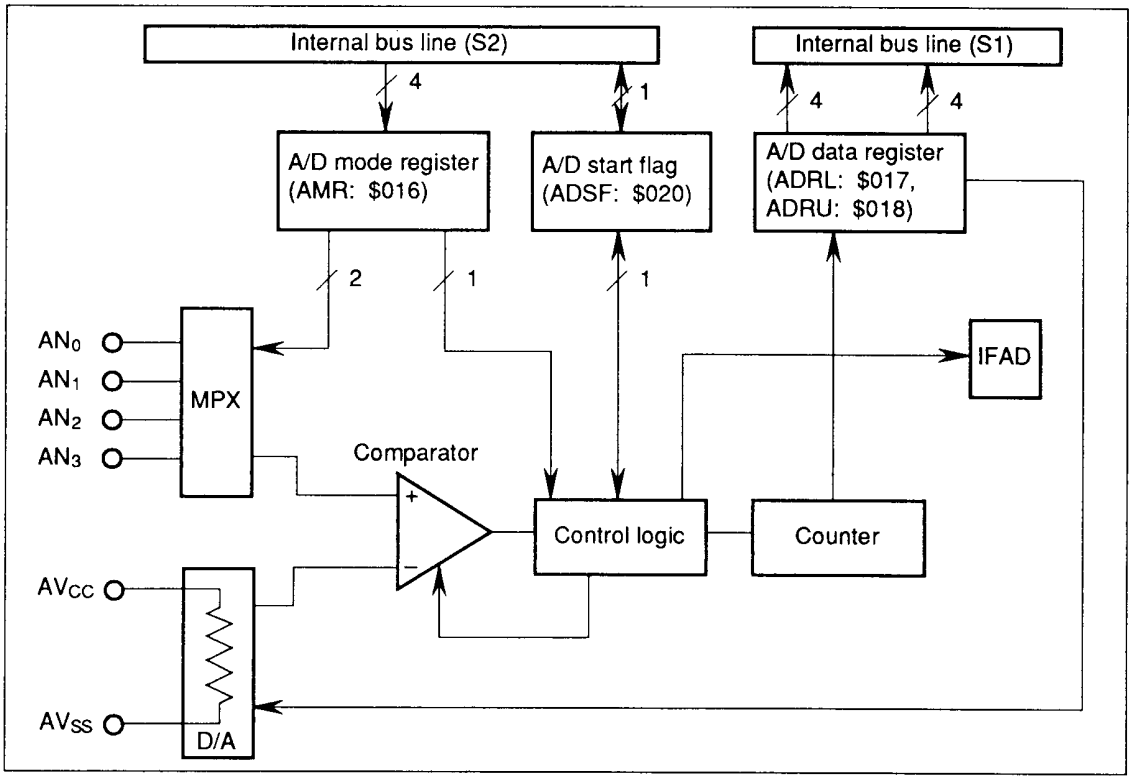


Figure 30 Block Diagram of A/D Converter

A/D mode register (AMR): $016

3	2	1	0

Switching time

Analog input selection

AMR		Switching Time
Bit 1	Bit 0	
0	0	34 t_{cyc}
	1	67 t_{cyc}
1	0	Not used
	1	

AMR		Analog Input Selection
Bit 3	Bit 2	
0	0	AN_0
	1	AN_1
1	0	AN_2
	1	AN_3

Special flag bits: $020

3	2	1	0

LSON (refer to description of low-power dissipation modes)

WDON (refer to description of timers)

A/D start flag (ADSF)

DTON (refer to description of low-power dissipation modes)

Bit 2	A/D Start Flag (ADSF)
1	A/D conversion started
0	A/D conversion completed

Figure 31 A/D Registers

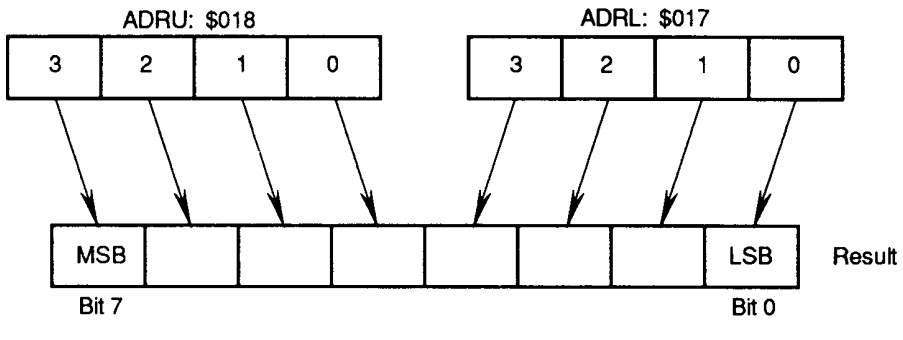


Figure 32 A/D Data Registers

Liquid-Crystal Display (LCD)

The MCU has an LCD controller and driver which drive four common signal pins and 24 segment pins. The controller consists of a RAM area in which display data is stored, a display control register (LCR), and a duty cycle/clock control register (LMR), as shown in figures 33 and 34.

Four duty cycles and the LCD clock are program-controllable, and a built-in dual-port RAM ensures that display data can be automatically transmitted to the segment signal pins without program intervention. If a 32-kHz oscillation clock is selected as the LCD clock source, the LCD can be used even in watch mode, in which the system clock stops.

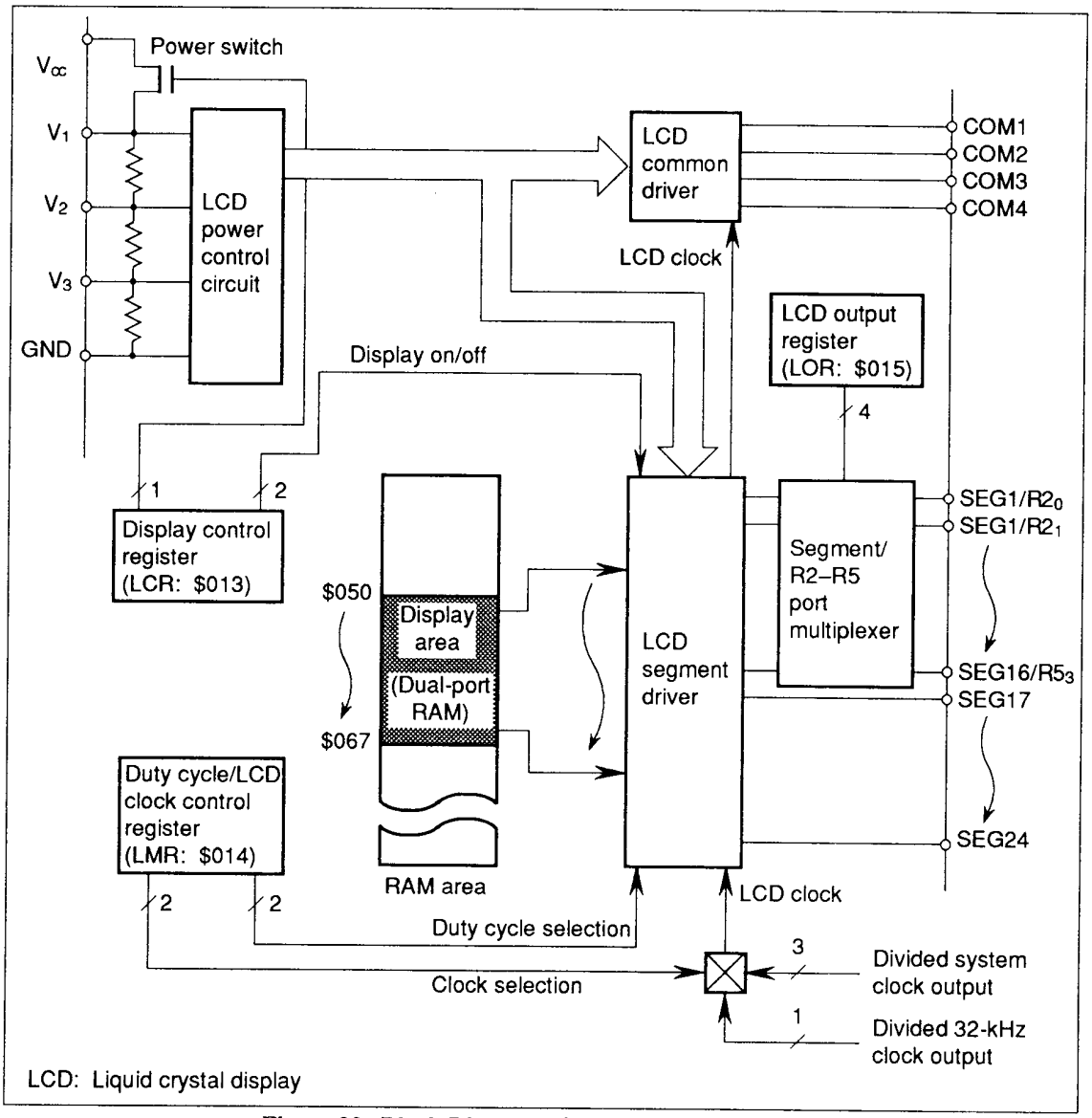


Figure 33 Block Diagram of Liquid Crystal Display

LCD Data Area and Segment Data ($050–$067): As shown in figure 35, each bit of the storage area corresponds to one of four duty cycles. If data is written to an area corresponding to a certain duty cycle, it is automatically output to the corresponding segments as display data.

LCD Control Register (LCR: $013): Three-bit write-only register which controls LCD blanking, the turning on and off of the liquid-crystal display's power supply division resistor, and display in watch and subactive modes, as shown in table 29.

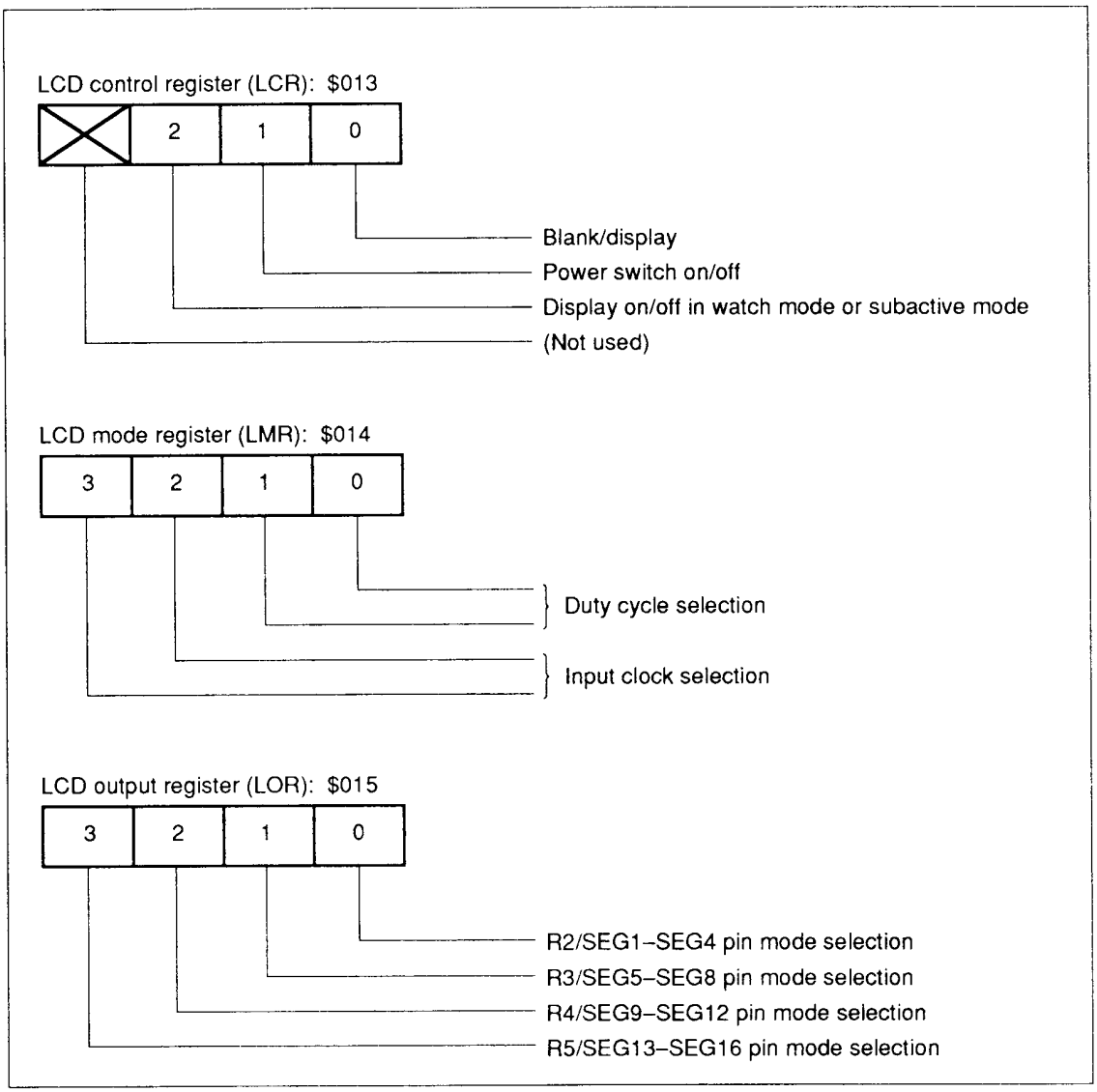


Figure 34 LCD Registers

- Blank/display
  Blank: Segment signals are turned off, regardless of LCD RAM data setting.
  Display: LCD RAM data is output as segment signals.

- Power switch on/off
  Off: The power switch is off.
  On: The power switch is on and V_1 is V_{CC}.

- Watch/subactive mode display
  Off: In watch and subactive modes, all common and segment pins are grounded and the liquid-crystal power switch is turned off.
  On: In watch and subactive modes, LCD RAM data is output as segment signals.

LCD Duty Cycle/Clock Control Register (LMR: $014): Four-bit write-only register which selects the display duty cycle and LCD clock source, as shown in table 30. The dependence of frame frequency on duty cycle is shown in table 31.

LCD Output Register (LOR: $015): Write-only register used to specify that ports R2–R5 act as pins SEG1–SEG16, as shown in table 32.

Large Liquid-Crystal Panel Drive and V_{LCD}: To drive a large-capacity LCD, decrease the resistance of the built-in division resistors by attaching external resistors in parallel, as shown in figure 36.

The size of these resistors cannot be simply calculated from the LCD load capacitance because the matrix configuration of the LCD complicates the paths of charge/discharge currents flowing through the capacitors—and the resistance will also vary with lighting conditions. This size must be determined by trial-and-error, taking into account the power dissipation of the device using the LCD, but a resistance of 1 to 10 kΩ would usually be suitable. (Another effective method is to attach capacitors of 0.1 to 0.3 μF.)

Always turn off the power switch (set bit 1 of the LCR to 0) before changing the liquid-crystal drive voltage (V_{LCD}).

	Bit 3	Bit 2	Bit 1	Bit 0	
80	SEG1	SEG1	SEG1	SEG1	$050
81	SEG2	SEG2	SEG2	SEG2	$051
82	SEG3	SEG3	SEG3	SEG3	$052
83	SEG4	SEG4	SEG4	SEG4	$053
84	SEG5	SEG5	SEG5	SEG5	$054
85	SEG6	SEG6	SEG6	SEG6	$055
86	SEG7	SEG7	SEG7	SEG7	$056
87	SEG8	SEG8	SEG8	SEG8	$057
88	SEG9	SEG9	SEG9	SEG9	$058
89	SEG10	SEG10	SEG10	SEG10	$059
90	SEG11	SEG11	SEG11	SEG11	$05A
91	SEG12	SEG12	SEG12	SEG12	$05B
	COM4	COM3	COM2	COM1	

	Bit 3	Bit 2	Bit 1	Bit 0	
92	SEG13	SEG13	SEG13	SEG13	$05C
93	SEG14	SEG14	SEG14	SEG14	$05D
94	SEG15	SEG15	SEG15	SEG15	$05E
95	SEG16	SEG16	SEG16	SEG16	$05F
96	SEG17	SEG17	SEG17	SEG17	$060
97	SEG18	SEG18	SEG18	SEG18	$061
98	SEG19	SEG19	SEG19	SEG19	$062
99	SEG20	SEG20	SEG20	SEG20	$063
100	SEG21	SEG21	SEG21	SEG21	$064
101	SEG22	SEG22	SEG22	SEG22	$065
102	SEG23	SEG23	SEG23	SEG23	$066
103	SEG24	SEG24	SEG24	SEG24	$067
	COM4	COM3	COM2	COM1	

Figure 35 Configuration of LCD RAM Area (for dual-port RAM)

Table 29 LCD Control Register

LCR Bit 2	Display in Watch Mode or Subactive Mode	LCR Bit 1	Power Switch On/Off	LCR Bit 0	Blank/Display
0	Off	0	Off	0	Blank
1	On	1	On	1	Display

Note: When using an LCD in watch mode or subactive mode, use the divided output of a 32-kHz oscillator as the LCD clock and set bit 2 of the LCR to 1. If using the divided output of the system clock as the LCD clock, always set bit 2 of the LCR to 0.

Table 30 LCD Duty Cycle/Clock Control Register

LMR				
Bit 3	Bit 2	Bit 1	Bit 0	Duty Selection/Input Clock Selection
—	—	0	0	1/4 duty cycle
			1	1/3 duty cycle
		1	0	1/2 duty cycle
			1	Static
0	0	—	—	CL0 (32.768/64 kHz when using 32.768-kHz oscillator)
	1			CL1 (f_{cyc}/256)
1	0			CL2 (f_{cyc}/2048)
	1			CL3 (refer to table 31)

Note: f_{cyc} is the divided system clock output.

Table 31 LCD Frame Periods for Different Duty Cycles

Static Duty Cycle

	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
	0	0	0	1	1	0	1	1
Instruction Cycle Time	CL0		CL1		CL2		CL3[Note]	
2 µs	512 Hz		1953 Hz		244 Hz		122 Hz/64 Hz	

1/2 Duty Cycle

	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
	0	0	0	1	1	0	1	1
Instruction Cycle Time	CL0		CL1		CL2		CL3[Note]	
2 µs	256 Hz		976.5 Hz		122 Hz		61 Hz/32 Hz	

1/3 Duty Cycle

	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
	0	0	0	1	1	0	1	1
Instruction Cycle Time	CL0		CL1		CL2		CL3[Note]	
2 µs	170.6 Hz		651 Hz		81.3 Hz		40.6 Hz/21.3 Hz	

1/4 Duty Cycle

	LMR							
	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2	Bit 3	Bit 2
	0	0	0	1	1	0	1	1
Instruction Cycle Time	CL0		CL1		CL2		CL3[Note]	
2 µs	128 Hz		488.2 Hz		61 Hz		30.5 Hz/16 Hz	

Note: The division ratio depends on the value of bit 3 of timer mode register A (TMA): the first value is for TMA3 = 0 and the second is for TMA3 = 1.

When TMA3 = 0, CL3 = f_{cyc}/4096.
When TMA3 = 1, CL3 = 32.768 kHz/512.

Table 32 LCD Output Register

LOR		LOR		LOR		LOR	
Bit 3	Port Selection	Bit2	Port Selection	Bit 1	Port Selection	Bit 0	Port Selection
0	R5	0	R4	0	R3	0	R2
1	SEG16–SEG13	1	SEG12–SEG9	1	SEG8–SEG5	1	SEG4–SEG1

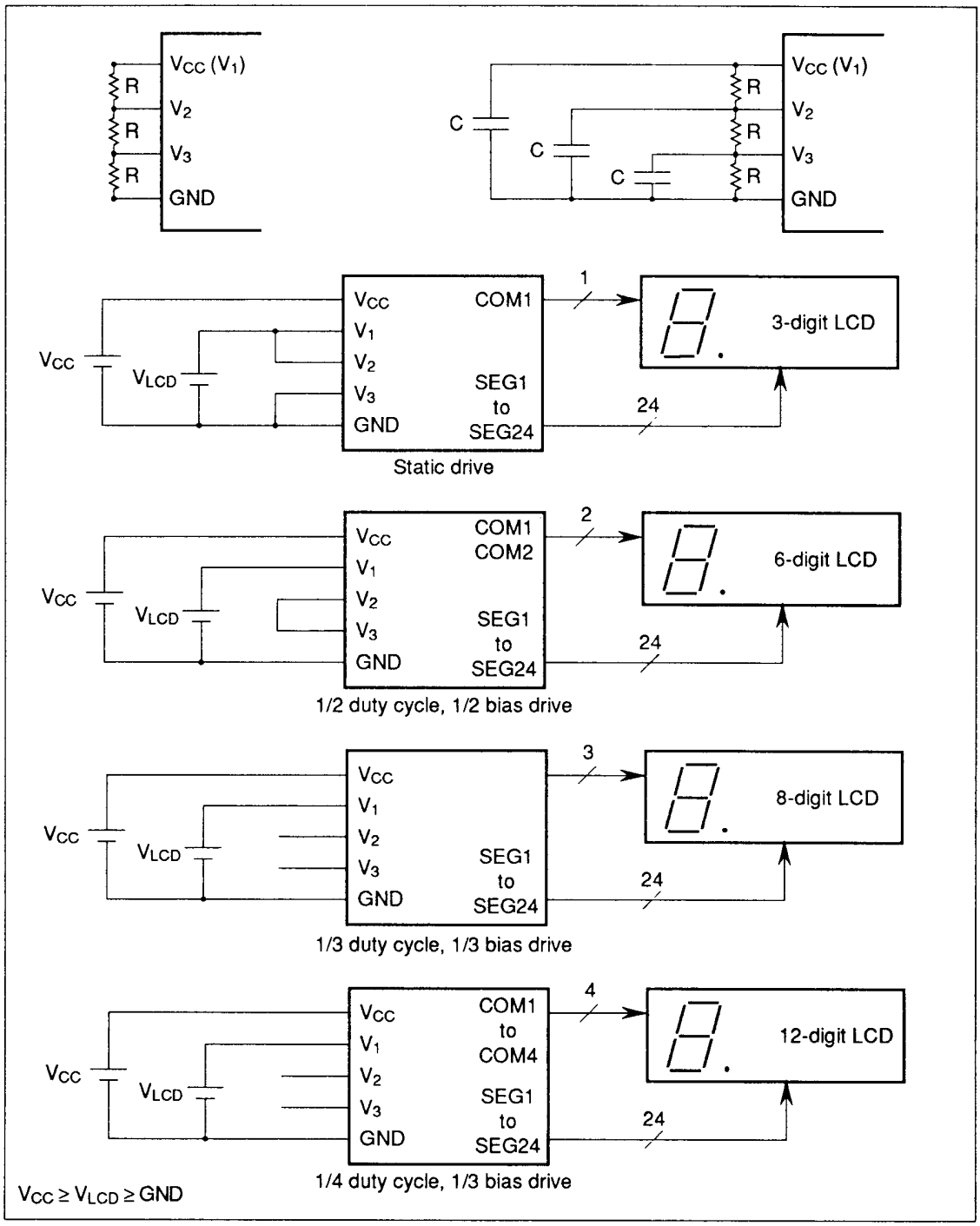


Figure 36 LCD Connection Examples

Zero-Crossing Detection Circuit

The MCU has a zero-crossing detection circuit that generates a digital signal in synchronism with an AC signal input to the ZCD pin through an external capacitor. A block diagram of the zero-crossing detection circuit is shown in figure 37.

The zero-crossing detection circuit has two modes (low sensitivity mode and high sensitivity mode) which are set by port mode register B (PMRB: $011) as shown in table 33.

A digital signal generated by the zero-crossing detection circuit sets the zero-crossing interrupt request flag (IFZC). The interrupt edge is selected by the interrupt mode register (IMR: $010). This signal can be made the input clock of timer B by setting the input clock source of timer mode register B (TMB: $009) for external event input.

Note: After MCU reset, the D_8/ZCD/$\overline{EVENT}$ pin is set to ZCD. With this setting, a supply current (bias current) always flows because a bias circuit within the zero-crossing circuit is still operating. This current flows in all MCU operation modes, but it is particularly critical in stop mode because the MCU is more affected by bias current since the other circuits of the LSI are not dissipating much current. If the zero-crossing detection function is not being used, use port mode register B to set this pin to D_8 or $\overline{EVENT}$. This prevents the bias current from flowing.

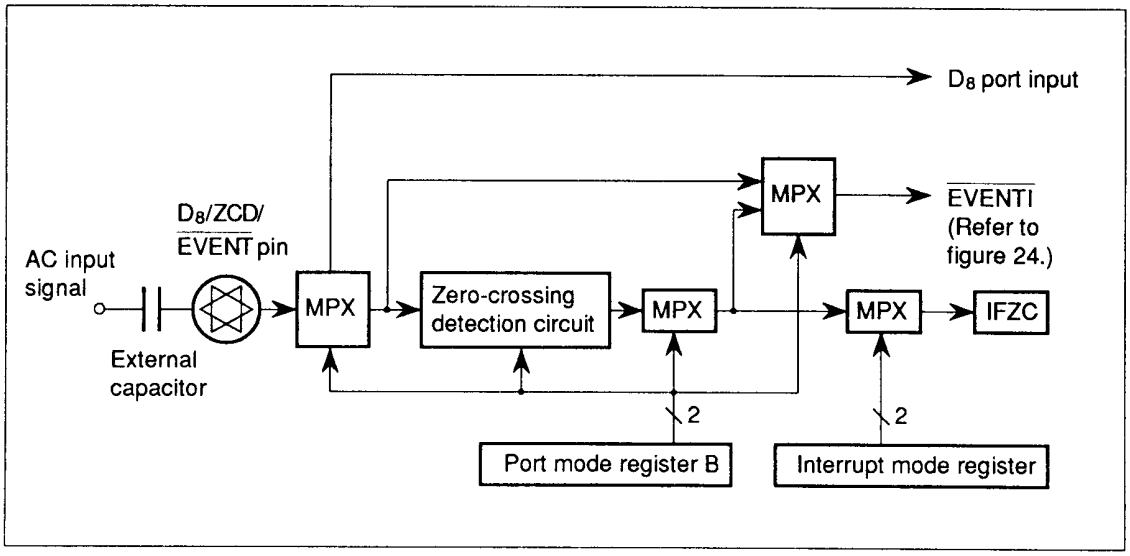


Figure 37 Block Diagram of Zero-Crossing Detection Circuit

Table 33 Port Mode Register B

PMRB		
1	**0**	**Port Selection**
0	0	ZCD (low sensitivity mode)
	1	ZCD (high sensitivity mode)*
1	0	D_8
	1	$\overline{EVENT}$

* Becomes low sensitivity in subactive mode.

Table 34 Registers in Special Register Area

Name	Address	R/W	Bit	Description
PMRA	$004	W	0	$R1_2$/S0 pin mode selection
			1	$R1_1$/SI pin mode selection
			2	$D_9/\overline{INT_0}$ pin mode selection
			3	D_{10}/INT_1 pin mode selection
SMR	$005	W	2–0	Serial transfer clock speed selection
			3	$R1_0/\overline{SCK}$ pin mode selection
SRL	$006	R/W	3–0	SCI data register, lower 4 bits
SRU	$007	R/W	3–0	SCI data register, upper 4 bits
TMA	$008	W	2–0	Input clock selection (timer A)
			3	Timer A/time-base mode selection
TMB	$009	W	2–0	Input clock selection (timer B)
			3	Auto reload function selection
TCBL/TLRL	$00A	R/W	3–0	Timer counter/timer load register (timer B), lower 4 bits
TCBU/TLRU	$00B	R/W	3–0	Timer counter/timer load register (timer B), upper 4 bits
MIS	$00C	W	1, 0	Interrupt frame period selection
			2	$R1_2$/SO PMOS off
			3	Changeover to setting by system oscillator frequency
TMC	$00D	W	2–0	Input clock selection (timer C)
			3	Auto reload function selection
TCCL/TCRL	$00E	R/W	3–0	Timer counter/timer load register (timer C), lower 4 bits
TCCU/TCRU	$00F	R/W	3–0	Timer counter/timer load register (timer C), upper 4 bits
IMR	$010	W	1, 0	INT_1 detection edge selection
			3, 2	Zero-crossing detection edge selection
PMRB	$011	W	1, 0	D_8/ZCD/$\overline{EVENT}$ pin mode selection
			3, 2	Do not use
PMRC	$012	W	1, 0	Buzzer frequency selection
			2	$R1_3$/ BUZZ pin mode selection
			3	Pull-up MOS transistor on/off selection
LCR	$013	W	0	LCD display selection
			1	LCD power switch on/off selection
			2	LCD display selection during watch mode
			3	Do not use
LMR	$014	W	1, 0	LCD duty cycle selection
			3, 2	LCD input clock selection

Table 34 Registers in Special Register Area (cont)

Name	Address	R/W	Bit	Description
LOR	$015	W	0	R2/SEG1–SEG4 pin mode selection
			1	R3/SEG5–SEG8 pin mode selection
			2	R4/SEG9–SEG12 pin mode selection
			3	R5/SEG13–SEG16 pin mode selection
AMR	$016	W	0	Conversion timing selection (A/D)
			1	Do not use
			3, 2	Analog input selection (A/D)
ADRL	$017	R	3–0	A/D data register, lower 4 bits
ADRU	$018	R	3–0	A/D data register, upper 4 bits
DCR0	$030	W	3–0	Data control register for port R0
DCR1	$031	W	3–0	Data control register for port R1
DCR2	$032	W	3–0	Data control register for port R2
DCR3	$033	W	3–0	Data control register for port R3
DCR4	$034	W	3–0	Data control register for port R4
DCR5	$035	W	3–0	Data control register for port R5
DCRB	$03B	W	3–0	Data control register for port D_0–D_3
DCRC	$03C	W	3–0	Data control register for port D_4–D_7
DCRD	$03D	W	0	Data control register for port D_8
			3–1	Do not use

PROM Mode Description

Programming the Built-in ROM

The MCU's built-in ROM is programmed in PROM mode in which the pins are arranged as shown in figure 38. PROM mode is set by pulling $\overline{TEST}$, $\overline{M}_0$, and $\overline{M}_1$ low and RESET high as shown in figure 39. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and a 64-to-28–pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 35.

Since an HMCS400–series instruction is ten bits long, the HMCS400–series MCU has a built-in conversion circuit to enable use of a general-purpose PROM programmer. This circuit splits each instruction into a lower five bits and an upper five bits that are read from or written to consecutive addresses. This means that if, for example, 16 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.

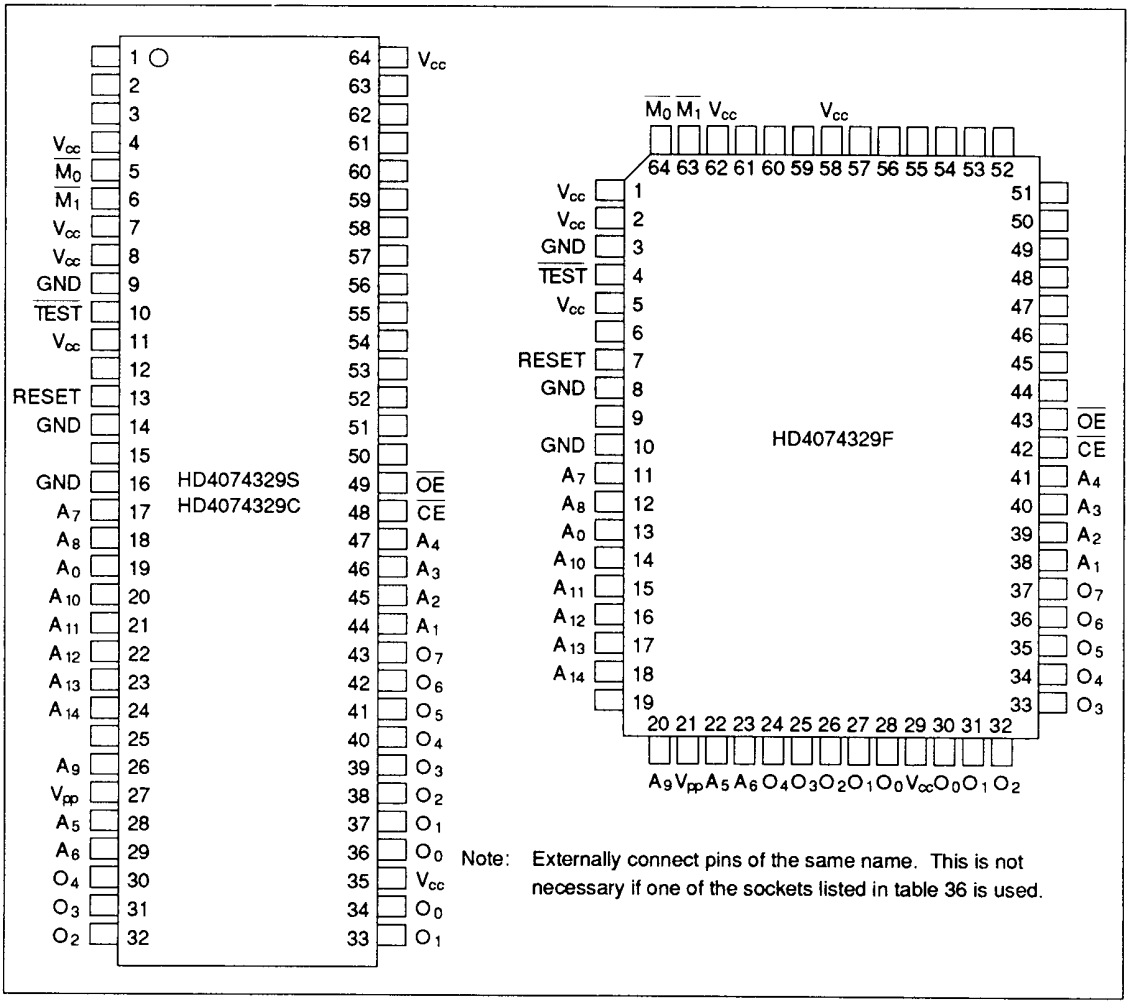


Figure 38 Pin Arrangement in PROM Mode

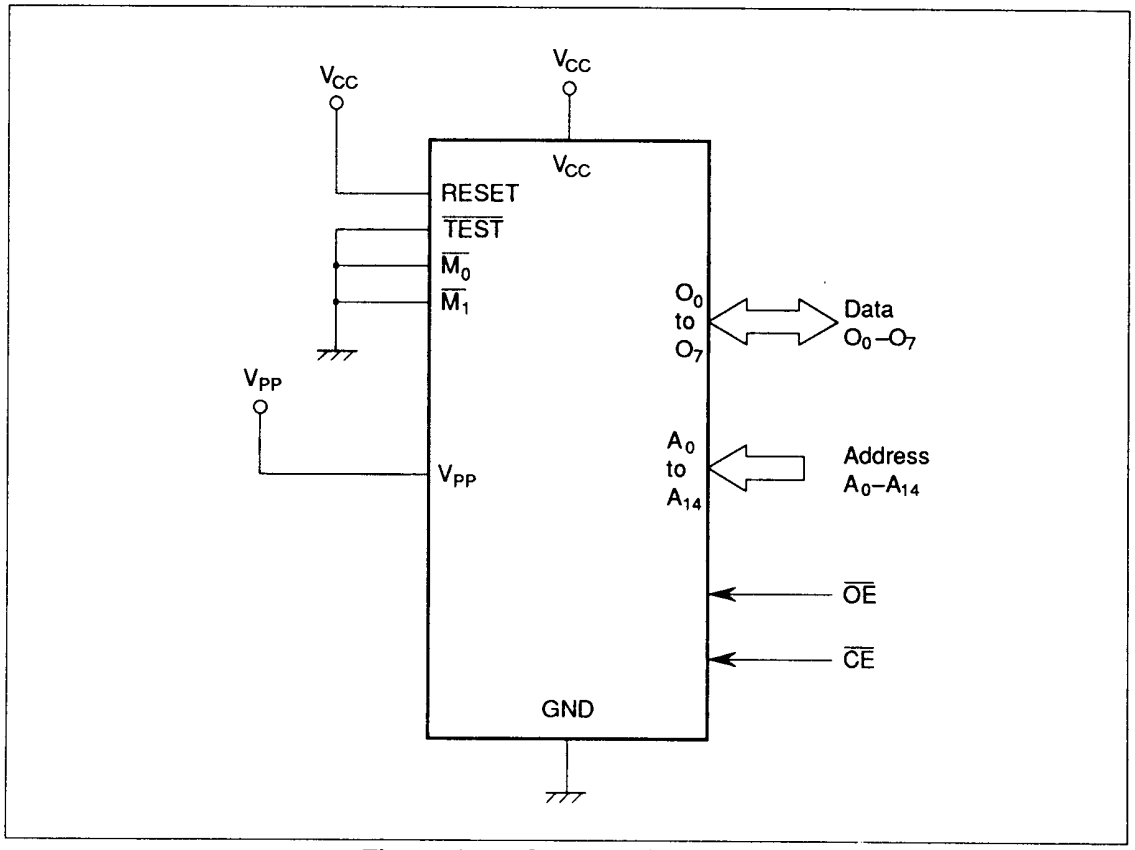


Figure 39 PROM Mode Connections

Table 35 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model name**	**Package**	**Manufacturer**	**Model Name**
DATA I/O Corp.	29B	DP–64S DC–64S	Hitachi	TBD
		FP–64B	Hitachi	TBD
AVAL Data Corp.	PKW–1000	DP–64S DC–64S	Hitachi	TBD TBD
		FP–64B	Hitachi	TBD

Table 36 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_7**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed, but the ceramic window-package version can be reprogrammed after being exposed to ultraviolet light.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed in the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Programming and Verification: The built-in PROM of the MCU can be programmed at high speed without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as shown in table 36, the memory map in PROM mode is shown in figure 40, the programming flowchart is shown in figure 41, and a timing chart of PROM programming and verification is shown in figure 42.

For details of PROM programming, refer to the Notes on PROM Programming section.

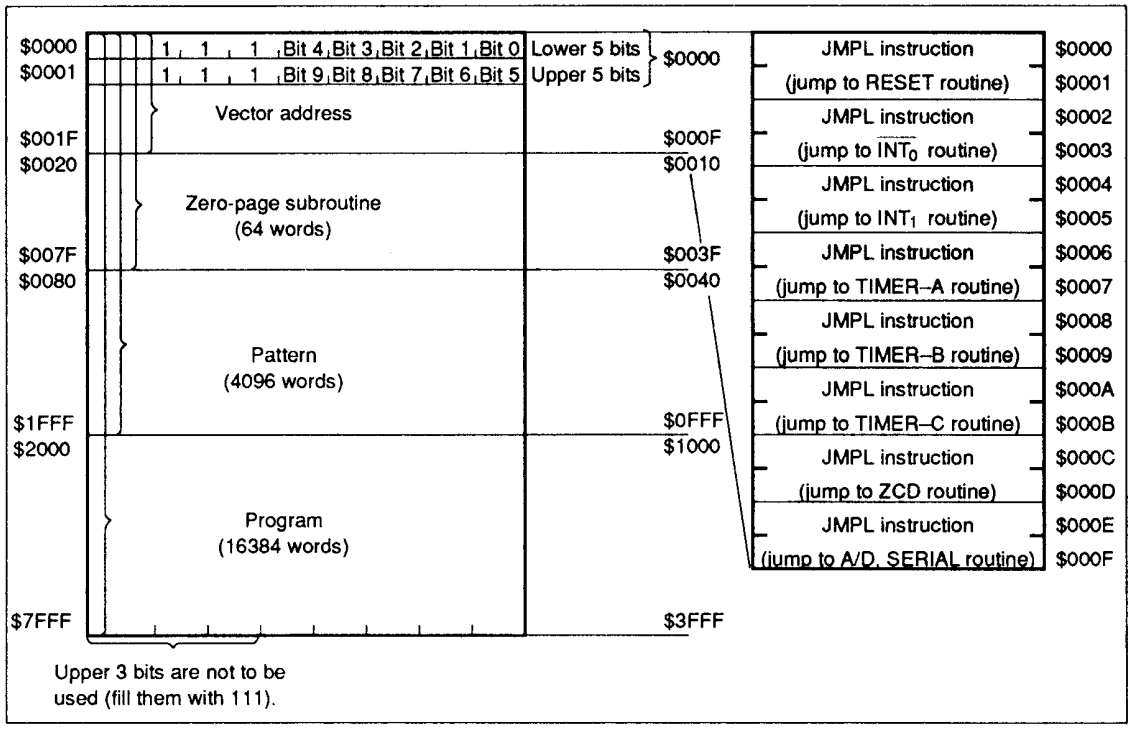


Figure 40 Memory Map in PROM Mode

Erasure (Window Package)

Data in the PROM is erased by exposing the LSI to ultraviolet light of a wavelength of 2537 Å for an integrated dose of at least 15 W.s/cm^2. These conditions can be satisfied by placing the LSI about 2–3 cm away from an ultraviolet lamp with a rating of 12,000 μW/cm^2 for about 20 minutes. After erasure, all PROM bits are set to 1.

For details of packages with windows, refer to the Notes on Window Packages section.

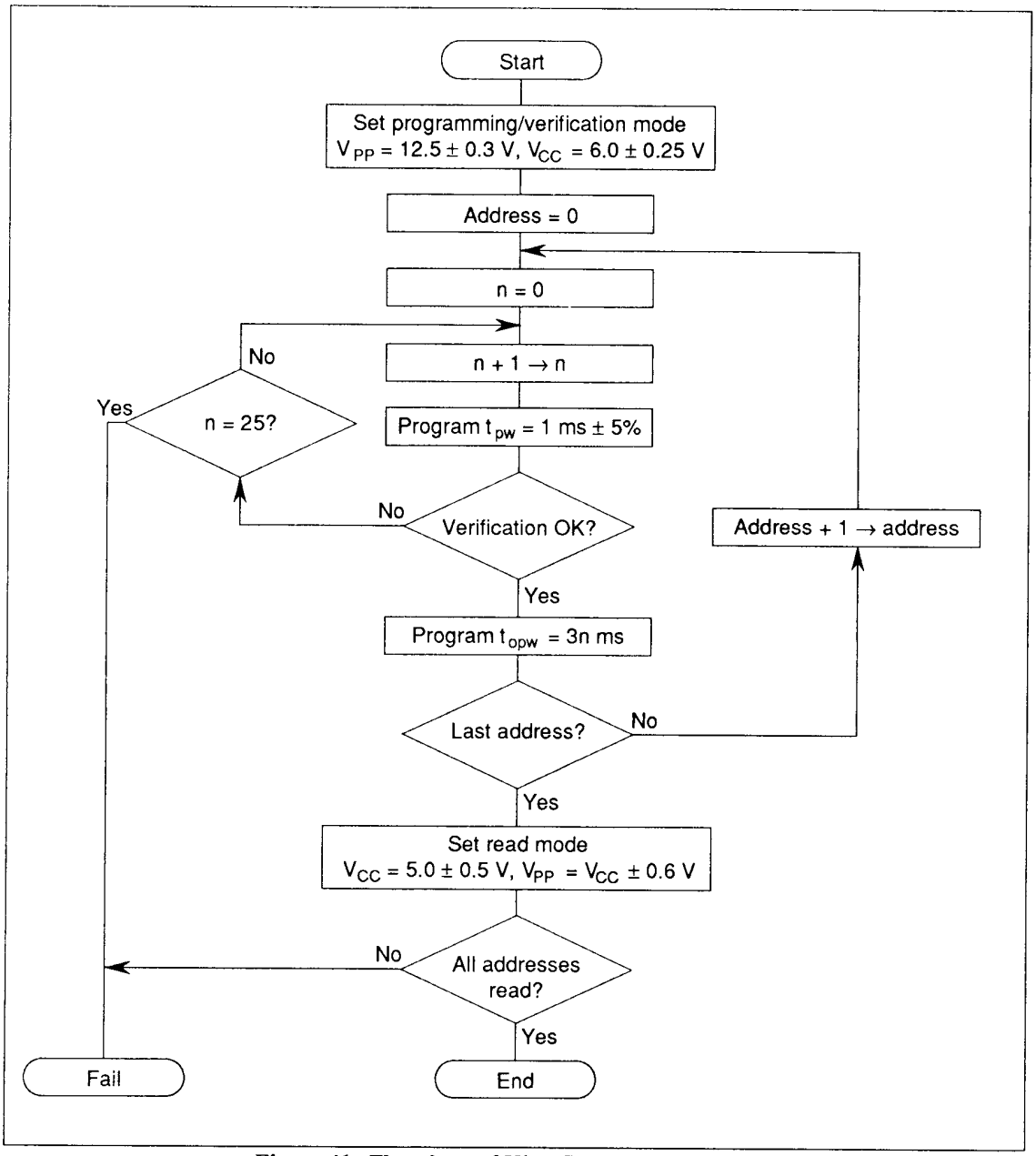


Figure 41 Flowchart of High-Speed Programming

Programming Electrical Characteristics

DC Characteristics during Programming/Verification (V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, V_{SS} = 0.0 V, Ta = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH}	O_0–O_7, A_0 –A_{14}, $\overline{OE}$, $\overline{CE}$	2.2	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	O_0–O_7, A_0 –A_{14}, $\overline{OE}$, $\overline{CE}$	–0.3	—	0.8	V	
Output high voltage	V_{OH}	O_0–O_7	2.4	—	—	V	I_{OH} = -200 µA
Output low voltage	V_{OL}	O_0–O_7	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage	$\lvert I_{LI} \rvert$	O_0–O_7, A_0 –A_{14}, $\overline{OE}$, $\overline{CE}$	—	—	2	µA	V_{in} = 5.25 V/0.5V
V_{CC} current	I_{CC}		—	—	30	mA	
V_{PP} current	I_{PP}		—	—	40	mA	

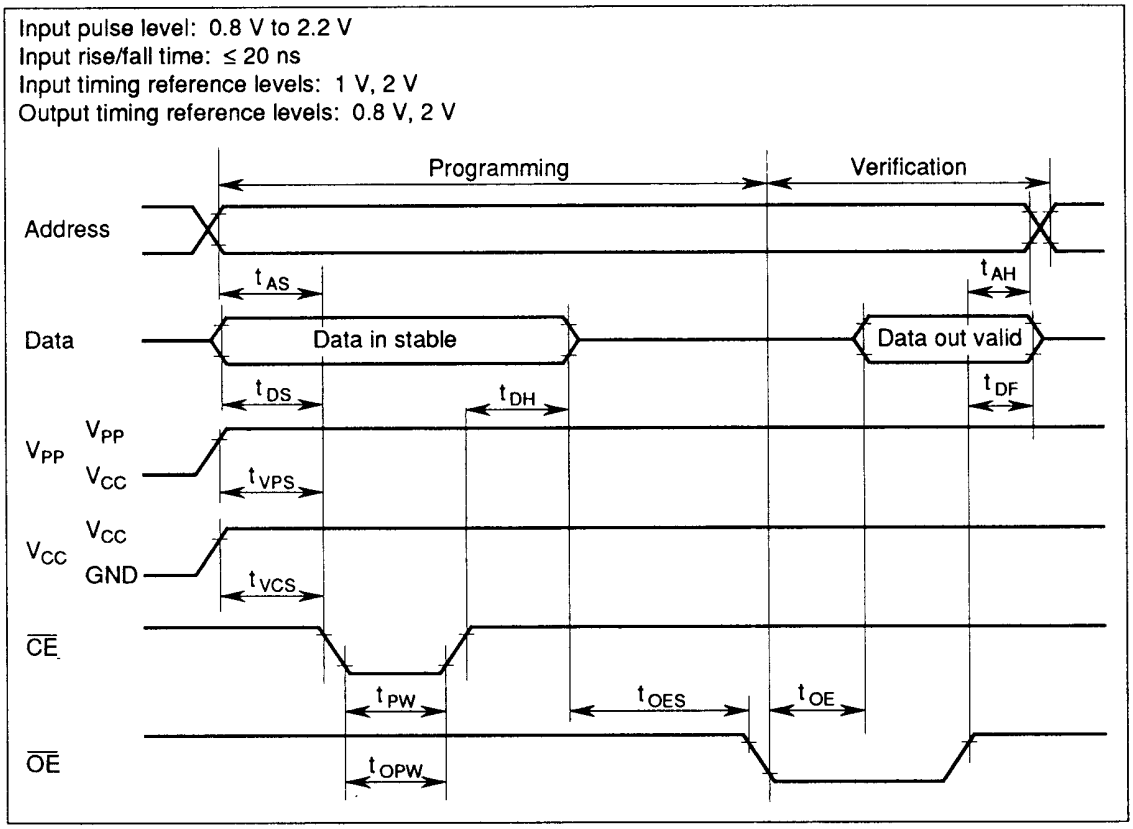


Figure 42 PROM Programming/Verification Timing

AC Characteristics during Programming/Verification (V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
Data output disable time	t_{DF}[Note]	—	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width during overprogram	t_{OPW}	2.85	—	78.75	ms	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
Data output delay time	t_{OE}	0	—	500	ns	

Note: t_{DF} is defined at the point where the output level can no longer be referenced after output is released.

DC Characteristics during Read (V_{CC} = 5.0 V ± 10%, V_{PP} = V_{CC} ± 0.6 V, Ta = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	1	µA	V_{CC} = 5.5 V, V_{in} = GND to V_{CC}
Output leakage current	I_{LO}	—	—	1	µA	V_{CC} = 5.5 V, V_{out} = GND to V_{CC}
Program pin current	I_{PP}	—	1	100	µA	V_{PP} = V_{CC} + 0.6 V
Power current in operation	I_{CC}[Note]	—	—	30	mA	f = 1 MHz, I_{out} = 0 mA
Input voltage	V_{IL}	–0.3	—	0.8	V	
	V_{IH}	2.2	—	V_{CC} + 0.3	V	
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –200 µA

Note: Excluding input through current.

AC Characteristics during Read (V_{CC} = 5.0 V ± 10%, V_{PP} = V_{CC} ± 0.6 V, Ta = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Min	Max	Unit	Test Conditions
Access time	t_{ACC}	—	500	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ output delay time	t_{CE}	—	500	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ output delay time	t_{OE}	10	150	ns	$\overline{CE}$ = V_{IL}
Output disable delay time	t_{DF}[Note]	0	105	ns	$\overline{CE}$ = V_{IL}
Data output hold time	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: t_{DF} is defined at the point where the output level can no longer be referenced after output is released.

Input pulse level: 0.8 V to 2.2 V
Input rise/fall time: ≤ 20 ns
Output loading: 1 TTL gate + 100 pF
Input timing reference levels: 1 V, 2 V
Output timing reference levels: 0.8 V, 2 V

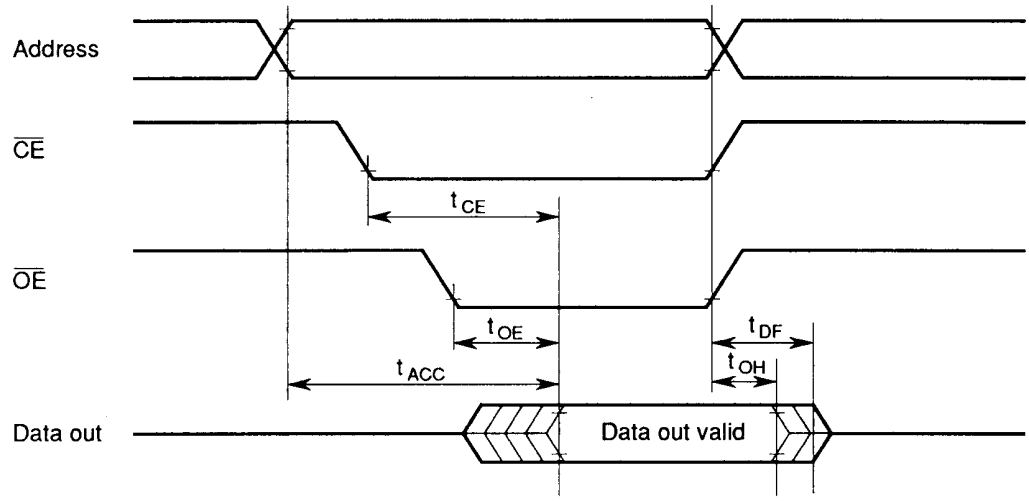


Figure 43 PROM Read Timing

Notes on PROM Programming

Principles of Programming/Erasure: A memory cell in a ZTAT microcomputer is the same as an EPROM cell: it is programmed by applying a high voltage between its control gate and drain to inject hot electrons into its floating gate. These electrons are stable, surrounded by an energy barrier formed by an SiO_2 film. The change in threshold voltage of a memory cell with a charged floating gate makes the corresponding bit appear as 0; a cell whose floating gate is not charged appears as a 1 bit (figure 44).

The charge in a memory cell may decrease with time. This decrease is usually due to one of the following causes:

- Ultraviolet light excites electrons, allowing them to escape. This effect is the basis of the erasure principle.
- Heat excites trapped electrons, allowing them to escape.
- High voltages between control gate and drain may erase electrons.

If the oxide film covering a floating gate is defective, the electron erasure rate will be greater. However, electron erasure does not often occur because defective devices are detected and removed at the testing stage.

PROM Programming: EPROM memory cells must be programmed under specific voltage and timing conditions. The higher the programming voltage V_{PP} and the longer the programming pulse t_{pw} is applied, the more electrons are injected into the floating gates. However, if V_{PP} exceeds specifications, the p-n junctions may be permanently damaged. Pay particular attention to overshooting in the PROM programmer. In addition, note that negative voltage noise will produce a parasitic transistor effect that may reduce breakdown voltages.

The ZTAT microcomputer is electrically connected to the PROM programmer by a socket adapter. Therefore, note the following points:

- Check that the socket adapter is firmly mounted on the PROM programmer.
- Do not touch the socket adapter or the LSI during the programming. Touching them may affect the quality of the contacts, which will cause programming errors.

PROM Reliability after Programming: In general, semiconductor devices retain their reliability, provided that some initial defects can be excluded. These initial defects can be detected and rejected by screening. Baking devices under high-temperature conditions is one method of screening that can rapidly eliminate data-hold defects in memory cells. (Refer to the Principles of Programming/ Erasure section.)

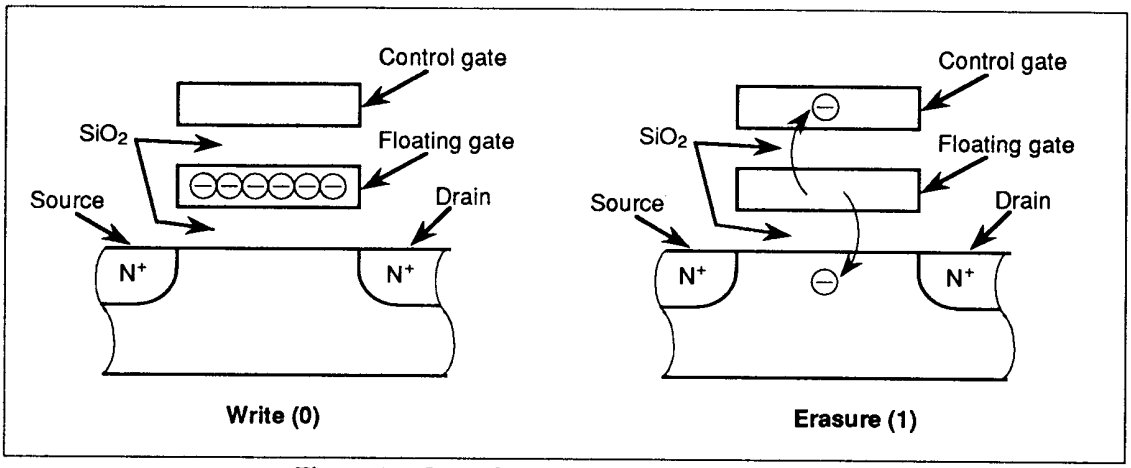


Figure 44 Cross-Sections through EPROM Cell

ZTAT microcomputer devices are extremely reliable because they have been subjected to such a screening method during the wafer fabrication process, but Hitachi recommends that each device is exposed to 150°C at one atmosphere for at least 48 hours after it is programmed, to ensure its best performance. The recommended screening process is shown in figure 45.

Notes on Window Packages

Glass Erasure Window: If the glass window comes into contact with plastic or something carrying a static charge, electrostatic charge on the window may make the LSI malfunction. If this occurs, expose the LSI to ultraviolet light for a few minutes to neutralize the charge and restore the LSI to normal operation. Unfortunately, this will also reduce the magnitude of charges stored in the floating gates, so reprogramming is recommended.

Build-up of electrostatic charge on the window is the main cause of malfunctions, so follow these basic rules for preventing electrostatic build-up:

- Everybody handling LSIs must either be grounded or wearing gloves.
- Never allow plastic to rub across the window.
- Be careful when using coolant sprays—they often contain ions.
- Cover the window with an ultraviolet-proof label (preferably one that contains a conductive material)—it's an effective way of neutralizing charge.

Ultraviolet-Proof Label: If the LSI is exposed to fluorescent light or sunlight, its memory contents may be erased by the small proportion of ultraviolet light present in such sources. In strong light, the MCU may even be damaged by photocurrents generated in it. To prevent such problems, Hitachi recommends that an ultraviolet-proof label is placed over the erasure window after the PROM is programmed.

Special labels containing metal to absorb ultraviolet light are sold for this purpose. When choosing labels, bear the following characteristics in mind:

- Adhesion (mechanical strength): Reuse and dust reduce adhesion, and peeling off a label may generate static electricity. Therefore it is best to erase and reprogram the PROM after peeling off its label. Rather than remove an old label, it is better to stick a new label over it.
- Allowable temperature range: Check the permissible environmental temperature range of the label. If used under conditions outside this range, the gum of the label may stiffen or adhere permanently to the window, even after the label is removed.
- Moisture resistance: Check the permissible humidity range and environmental conditions of the label. It is currently difficult to find a ultraviolet-proof label suitable for all conditions, so select a label that is appropriate for the conditions under which the MCU will operate.

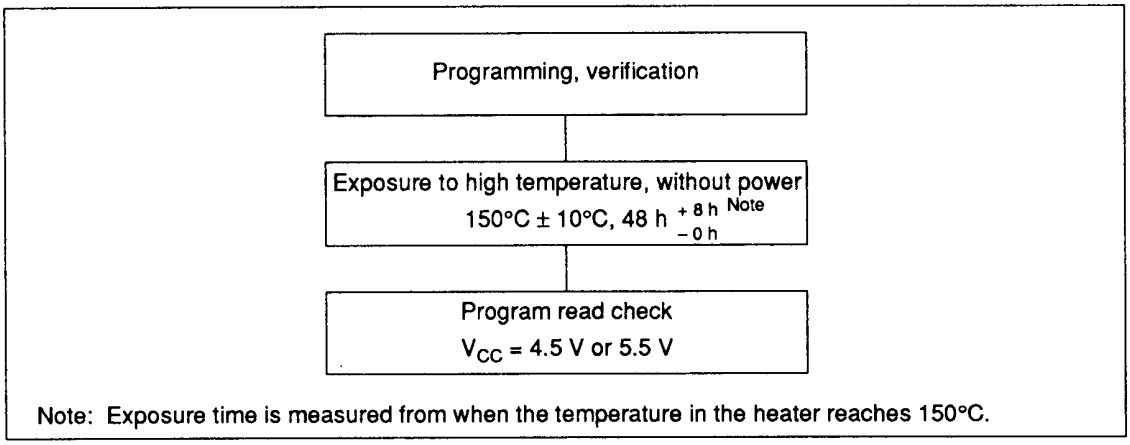


Figure 45 Recommended Screening Flow

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 46 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory register (MR), which consists of 16 addresses from $040 to $04F, is accessed with the LAMR and XMRA instructions.

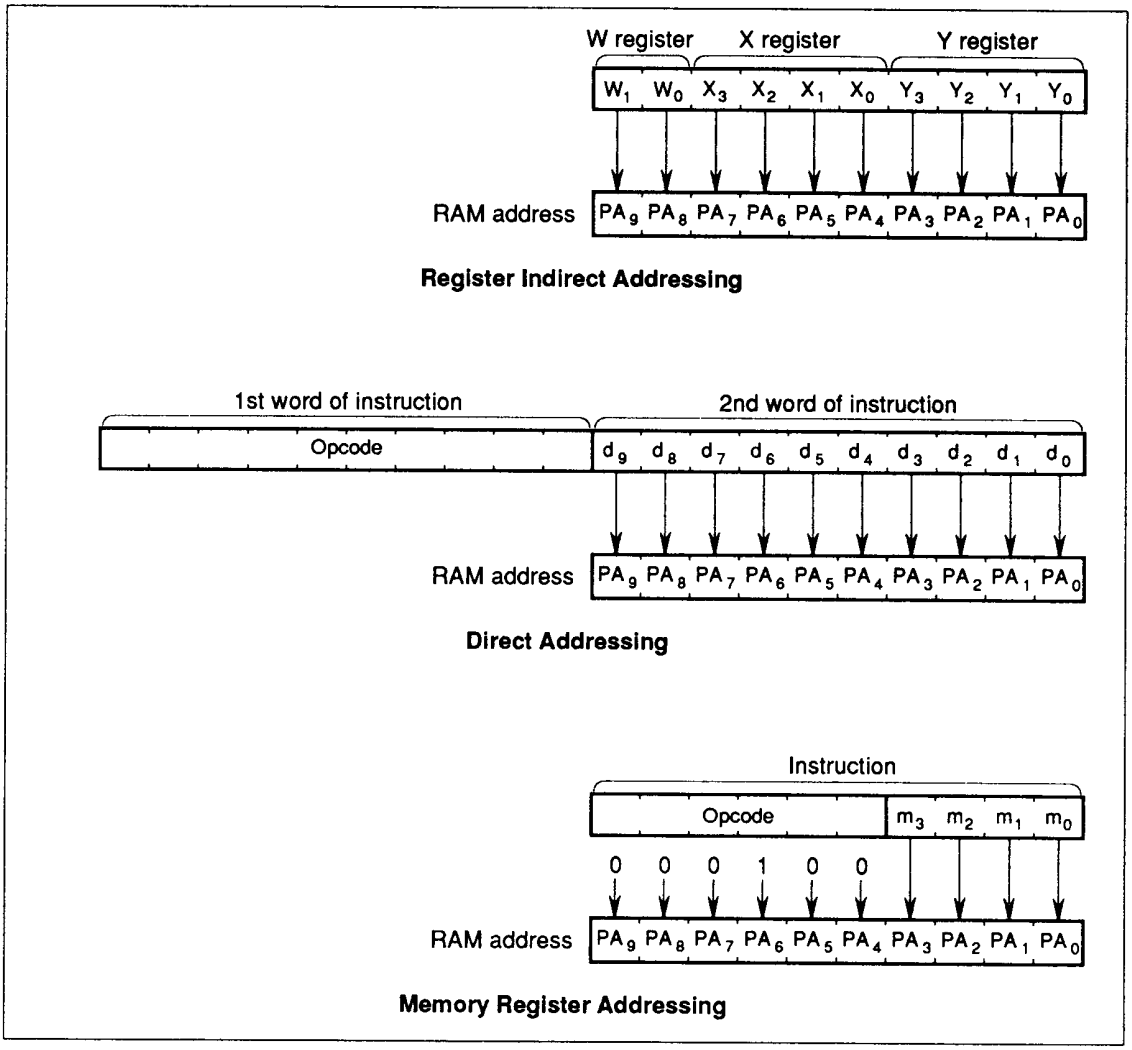


Figure 46 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 47 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 49. This means that the execution of a BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macro assembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at $000–$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 48. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R0 and R1 port output register. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register and also to the R0 and R1 port output register at the same time.

The P instruction has no effect on the program counter.

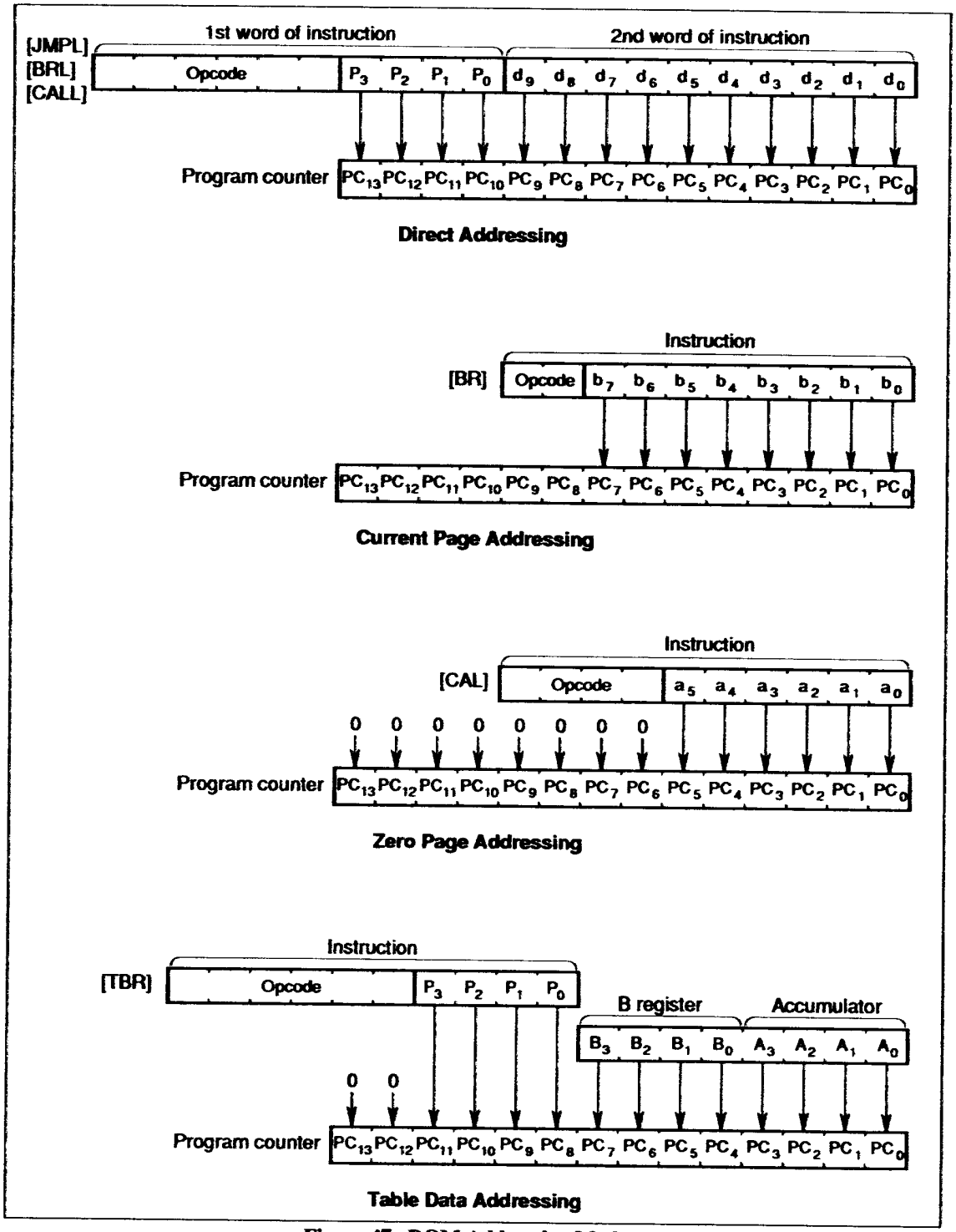


Figure 47 ROM Addressing Modes

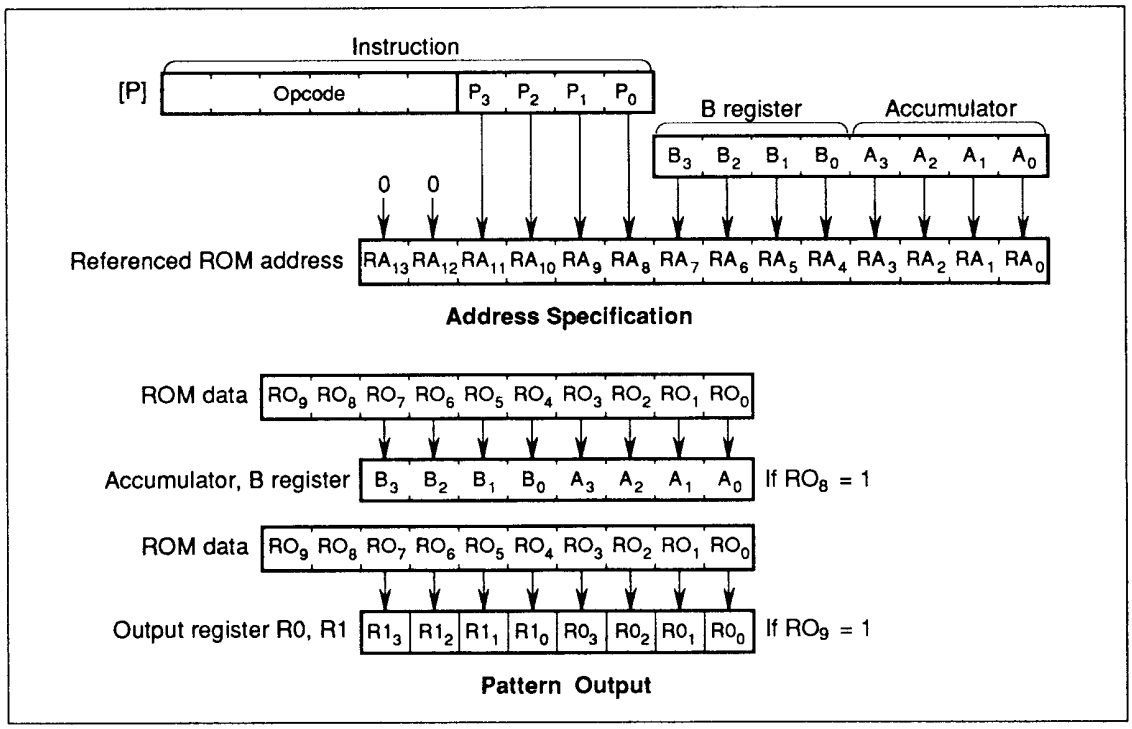


Figure 48 P Instruction

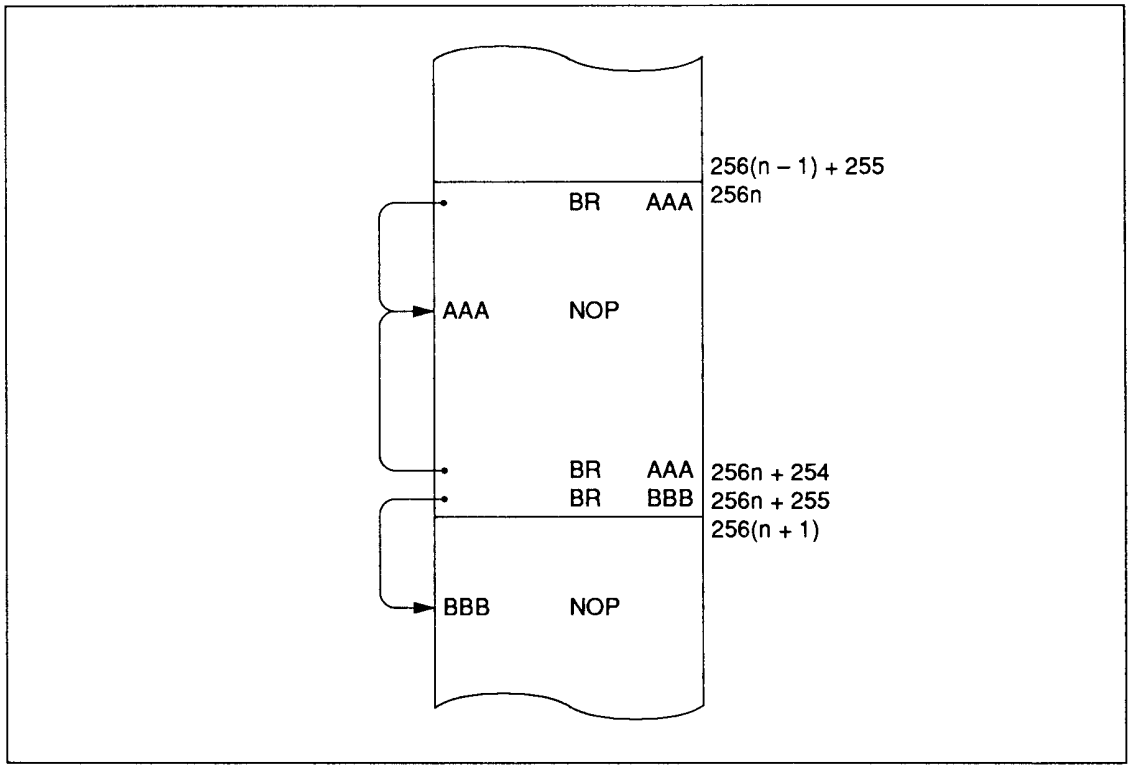


Figure 49 Branching when Branch Destination is on Page Boundary

Instruction Set

The HD404328 and HD4074329 each have 101 instructions, classified into the following 10 groups:

- Immediate instructions
- Register-to-register instructions
- RAM address instructions
- RAM register instructions
- Arithmetic instructions
- Compare instructions
- RAM bit manipulation instructions
- ROM address instructions
- Input/output instructions
- Control instructions

The functions of these instructions are listed in tables 38 to 47, and an opcode map is shown in table 48.

Table 38 Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from immediate	LAIi	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i → A		1/1
Load B from immediate	LBIi	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i → B		1/1
Load memory from immediate	LMIDi,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i → M		2/2
Load memory from immediate, increment Y	LMIIYi	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i → M, Y + 1 → Y	NZ	1/1

Table 39 Register-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2[Note]
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMRm	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m) → A		1/1
Exchange MR and A	XMRAm	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m) ↔ A		1/1

Note: The assembler automatically provides an operand for the second word of the LAW instruction.

Table 40 RAM Address Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Load W from immediate	LWIi	0	0	1	1	1	1	0	0	i_1	i_0	i → W		1/1
Load X from immediate	LXIi	1	0	0	0	1	0	i_3	i_2	i_1	i_0	i → X		1/1
Load Y from immediate	LYIi	1	0	0	0	0	1	i_3	i_2	i_1	i_0	i → Y		1/1
Load W from A	LWA	0	1	0	0	0	1	0	0	0	0	A → W		2/2[Note]
		0	0	0	0	0	0	0	0	0	0			
Load X from A	LXA	0	0	1	1	1	0	1	0	0	0	A → X		1/1
Load Y from A	LYA	0	0	1	1	0	1	1	0	0	0	A → Y		1/1
Increment Y	IY	0	0	0	1	0	1	1	1	0	0	Y + 1 → Y	NZ	1/1
Decrement Y	DY	0	0	1	1	0	1	1	1	1	1	Y − 1 → Y	NB	1/1
Add A to Y	AYY	0	0	0	1	0	1	0	1	0	0	Y + A → Y	OVF	1/1
Subtract A from Y	SYY	0	0	1	1	0	1	0	1	0	0	Y − A → Y	NB	1/1
Exchange X and SPX	XSPX	0	0	0	0	0	0	0	0	0	1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0	0	0	0	0	0	0	0	1	0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0	0	0	0	0	0	0	0	1	1	X ↔ SPX,Y ↔ SPY		1/1

Note: The assembler automatically provides an operand for the second word of the LWA instruction.

Table 41 RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A (X ↔ SPX, Y ↔ SPY)		1/1
Load A from memory	LAMDd	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M → A		2/2
Load B from memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B (X ↔ SPX, Y ↔ SPY)		1/1
Load memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M (X ↔ SPX, Y ↔ SPY)		1/1
Load memory from A	LMADd	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A → M		2/2
Load memory from A, increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y + 1 → Y (X ↔ SPX)	NZ	1/1
Load memory from A, decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y − 1 → Y (X ↔ SPX)	NB	1/1
Exchange memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A (X ↔ SPX, Y ↔ SPY)		1/1
Exchange memory and A	XMADd	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M ↔ A		2/2
Exchange memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B (X ↔ SPX, Y ↔ SPY)		1/1

Note: The meanings of (XY) and (X) are as follows:

Each instruction marked with (XY) has 4 mnemonics, each with different object codes. For example, different values of x and y of the opcode of the LAM(XY) instruction are given below.

Mnemonic	Y	X	Function
LAM	0	0	None
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X ↔ SPX, Y ↔ SPY

Each instruction marked with (X) has 2 mnemonics, each with different object codes. For example, different values of x of the opcode of the LMAIY(X) instruction are given below.

Mnemonic	X	Function
LMAIY	0	None
LMAIYX	1	X ↔ SPX

Table 42 Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add immediate to A	Ali	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A + i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B + 1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B − 1 → B	NB	1/1
Decimal adjust for addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal adjust for subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A}$ + 1 → A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B}$ → B		1/1
Rotate right A with carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate left A with carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to memory	AM	0 0 0 0 0 0 1 0 0 0	M + A → A	OVF	1/1
Add A to memory	AMDd	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M + A → A	OVF	2/2
Add A to memory with carry	AMC	0 0 0 0 0 1 1 0 0 0	M + A + CA → A OVF → CA	OVF	1/1
Add A to memory with carry	AMCDd	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M + A + CA → A OVF → CA	OVF	2/2
Subtract A from memory with carry	SMC	0 0 1 0 0 1 1 0 0 0	M − A − $\overline{CA}$ → A NB → CA	NB	1/1
Subtract A from memory with carry	SMCDd	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M − A − $\overline{CA}$ → A NB → CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1/1
AND memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND memory with A	ANMDd	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∩ M → A	NZ	2/2
OR memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1/1
OR memory with A	ORMDd	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∪ M → A	NZ	2/2
EOR memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR memory with A	EORMDd	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ⊕ M → A	NZ	2/2

Table 43 Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate not equal to memory	INEMi	0 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \neq M$	NZ	1/1
Immediate not equal to memory	INEMDi,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \neq M$	NZ	2/2
A not equal to memory	ANEM	0 0 0 0 0 0 0 1 0 0	$A \neq M$	NZ	1/1
A not equal to memory	ANEMDd	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \neq M$	NZ	2/2
B not equal to memory	BNEM	0 0 0 1 0 0 0 1 0 0	$B \neq M$	NZ	1/1
Y not equal to immediate	YNEIi	0 0 0 1 1 1 i_3 i_2 i_1 i_0	$Y \neq i$	NZ	1/1
Immediate less than or equal to memory	ILEMi	0 0 0 0 1 1 i_3 i_2 i_1 i_0	$i \leq M$	NB	1/1
Immediate less than or equal to memory	ILEMDi,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \leq M$	NB	2/2
A less than or equal to memory	ALEM	0 0 0 0 0 1 0 1 0 0	$A \leq M$	NB	1/1
A less than or equal to memory	ALEMDd	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \leq M$	NB	2/2
B less than or equal to memory	BLEM	0 0 1 1 0 0 0 1 0 0	$B \leq M$	NB	1/1
A less than or equal to immediate	ALEIi	1 0 1 0 1 1 i_3 i_2 i_1 i_0	$A \leq i$	NB	1/1

Table 44 RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set memory bit	SEMn	0 0 1 0 0 0 0 1 n_1 n_0	$i \rightarrow M(n)$		1/1
Set memory bit	SEMDn,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \rightarrow M(n)$		2/2
Reset memory bit	REMn	0 0 1 0 0 0 1 0 n_1 n_0	$0 \rightarrow M(n)$		1/1
Reset memory bit	REMDn,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$0 \rightarrow M(n)$		2/2
Test memory bit	TMn	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test memory bit	TMn,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 45 ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on status 1	BRb	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long branch on status 1	BRLu	0 1 0 1 1 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long jump unconditionally	JMPLu	0 1 0 1 0 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine jump on status 1	CALa	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long subroutine jump on status 1	CALLu	0 1 0 1 1 0 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table branch	TBRp	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E, carry restored	ST	1/3

Table 46 Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set discrete I/O latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D (Y)		1/1
Set discrete I/O latch direct	SEDDm	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1 → D (m)		1/1
Reset discrete I/O latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D (Y)		1/1
Reset discrete I/O latch direct	REDDm	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0 → D (m)		1/1
Test discrete I/O latch	TD	0 0 1 1 1 0 0 0 0 0		D (Y)	1/1
Test discrete I/O latch direct	TDDm	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D (m)	1/1
Load A from R-port register	LARm	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R (m) → A		1/1
Load B from R-port register	LBRm	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R (m) → B		1/1
Load R-port register from A	LRAm	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A → R (m)		1/1
Load R-port register from B	LRBm	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B → R (m)		1/1
Pattern generation	Pp	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 47 Control Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
No operation	NOP	0	0	0	0	0	0	0	0	0	0			1/1
Start serial	STS	0	1	0	1	0	0	1	0	0	0			1/1
Standby mode/watch mode[Note]	SBY	0	1	0	1	0	0	1	1	0	0			1/1
Stop mode/watch mode	STOP	0	1	0	1	0	0	1	1	0	1			1/1

Note: Only after a transition from subactive mode.

Table 48 Opcode Map

R9	H \ L	R8=0 L=0	L=1	L=2	L=3	L=4	L=5	L=6	L=7	L=8	L=9	L=A	L=B	L=C	L=D	L=E	L=F
0	0	NOP	XSPX	XSPY	XSPXY	ANEM				AM				ORM			
	1	RTN	RTNI			ALEM				AMC				EORM			
	2	INEM i (4)															
	3	ILEM i (4)															
	4	LBM(XY)				BNEM				LAB				IB			
	5	LMAIY(X)				AYY				LASPY				IY			
	6	NEGA				RED				LASPX							TC
	7	YNEI i (4)															
	8	XMA(XY)				SEM n (2)				REM n (2)				TM n (2)			
	9	LAM(XY)				LMA(XY)				SMC				ANM			
	A	ROTR	ROTL					DAA				DAS					LAY
	B	TBR p (4)															
	C	XMB(XY)				BLEM				LBA							DB
	D	LMADY(X)				SYY				LYA							DY
	E	TD				SED				LXA				REC			SEC
	F	LWI i (2)															
1	0	LBI i (4)															
	1	LYI i (4)															
	2	LXI i (4)															
	3	LAI i (4)															
	4	LBR m (4)															
	5	LAR m (4)															
	6	REDD m (4)															
	7	LAMR m (4)															
	8	AI i (4)															
	9	LMIIY i (4)															
	A	TDD m (4)															
	B	ALEI i (4)															
	C	LRB m (4)															
	D	LRA m (4)															
	E	SEDD m (4)															
	F	XMRA m (4)															

1-word/2-cycle instruction

1-word/3-cycle instruction

RAM direct address instruction (2-word/2-cycle)

2-word/2-cycle instruction

Table 48 Opcode Map (cont)

R9	H \ L	R8=0	1	2	3	4	5	6	7	R8=1	9	A	B	C	D	E	F
0	0	LAW				ANEMD				AMD				ORMD			
	1	LWA				ALEMD				AMCD				EORMD			
	2	INEMD i (4)															
	3	ILEMD i (4)															
	4	COMB				OR				STS				SBY	STOP		
	5	JMPL p (4)															
	6	CALL p (4)															
	7	BRL p (4)															
	8	XMAD				SEMD n (2)				REMD n (2)				TMD n (2)			
	9	LAMD				LMAD				SMCD				ANMD			
	A	LMID i (4)															
	B	P p (4)															
	C	CAL a (6)															
	D																
	E																
	F																
1	0	BR b (8)															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																

1-word/2-cycle instruction

1-word/3-cycle instruction

RAM direct address instruction (2-word/2-cycle)

2-word/2-cycle instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	2
Pin voltage	V_T	–0.3 to (V_{CC} + 0.3)	V	
Total permissible input current	ΣI_o	100	mA	3
Total permissible output current	$-\Sigma I_o$	50	mA	4
Maximum input current	I_o	4	mA	5, 6
		30	mA	5, 7
Maximum output current	$-I_o$	4	mA	8, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	
Storage temperature (bias)	T_{bias}	–25 to +80	°C	

Notes:
1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the Electrical Characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.
2. D_{10} (V_{PP}) of the HD4074329.
3. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to ground.
4. The total permissible output current is the total of output currents simultaneously flowing out from V_{cc} to all I/O pins.
5. The maximum input current is the maximum current flowing from any I/O pin to ground.
6. Applies to D_8, R0–R5.
7. Applies to D_0–D_7.
8. The maximum output current is the maximum current flowing from V_{cc} to any I/O pin.
9. Applies to D_0–D_8, R0–R5.

Electrical Characteristics

DC Characteristics (HD404328: V_{CC} = 2.7 to 6.0 V, HD4074329: V_{CC} = 3.0 to 5.5 V; GND = 0.0 V; Ta = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, INT_1, SI, $\overline{EVENT}$	0.8V_{CC}	—	V_{CC} + 0.3	V	V_{CC} = 3.5 to 6.0 V	
			0.9V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V	V_{CC} = 3.5 to 6.0 V	
			V_{CC} – 0.3	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, INT_1, $\overline{EVENT}$, SI	–0.3	—	0.2V_{CC}	V	V_{CC} = 3.5 to 6.0 V	
			–0.3	—	0.1V_{CC}	V		
		OSC_1	–0.3	—	0.5	V	V_{CC} = 3.5 to 6.0 V	
			–0.3	—	0.3	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, BUZZ	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, BUZZ	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, INT_1, SI SO, OSC_1, BUZZ	—	—	1.0	µA	V_{in} = 0 to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	3	6	mA	V_{CC} = 5.0 V, f_{osc} = 4 MHz	2, 4
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	0.6	1.5	mA	V_{CC} = 3.0 V, LCD on	3, 4
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	70	100	µA	V_{CC} = 3.0 V, LCD on	
			—	50	70			5
Current dissipation in watch mode (1)	I_{WTC1}	V_{CC}	—	4	15	µA	V_{CC} = 3.0 V, LCD off	6
Current dissipation in watch mode (2)	I_{WTC2}	V_{CC}	—	15	35	µA	V_{CC} = 3.0 V, LCD on	6
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	1	10	µA	V_{CC} = 3.0 V, X1 = V_{CC}	6
Stop mode retain voltage	V_{STOP}	V_{CC}	2	—	—	V	No 32-kHz oscillator	7

Notes on next page

Notes: 1. Output buffer current is excluded.
2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
Test conditions: MCU: Reset
Pins: RESET, $\overline{TEST}$, D_0–D_7, D_9, D_{10}, R0–R5 at V_{CC}
D_8 open
3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
Test conditions: MCU: I/O reset
Serial interface stopped
Standby mode
Pins: RESET at GND
$\overline{TEST}$, D_0–D_7, D_9, D_{10}, R0–R5 at V_{CC}
D_8 open
4. The power dissipation while the MCU is operating or is in standby mode is in proportion to f_{osc}. The value of the dissipation current when f_{osc} = x MHz is given by the following equation: Maximum value (f_{osc} = x MHz) = x/4 × maximum value (f_{osc} = 4 MHz)
5. Applies to HD404328 only.
6. D_{10} is connected to V_{CC} in the HD4074329.
7. RAM data retention

I/O Characteristics for Standard Pins (HD404328: V_{CC} = 2.7 to 6.0 V, HD4074329: V_{CC} = 3.0 to 5.5 V; GND = 0.0 V; Ta = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Input high voltage	V_{IH}	D_8–D_{10}, R0–R5	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_8–D_{10}, R0–R5	–0.3	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_8, R0–R5	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_8, R0–R5	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	D_8, D_9, R0–R5	—	—	1.0	µA	V_{in} = 0 to V_{CC}	1
		D_{10}	—	—	20.0	µA		
Pull-up MOS current	$-I_P$	D_8, R0–R5	5	25	90	µA	V_{CC} = 3.0V, V_{in} = 0.0V	

Note: 1. Output buffer current is excluded.

I/O Characteristics for Large-Current Pins (HD404328: V_{CC} = 2.7 to 6.0 V, HD4074329: V_{CC} = 3.0 to 5.5 V; GND = 0.0 V; Ta = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Input high voltage	V_{IH}	D_0–D_7	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_7	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_7	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_0–D_7	—	—	0.4	V	I_{OL} = 0.4 mA	
			—	—	2.0	V	I_{OL} = 15 mA V_{CC} = 4.5 to 6.0 V	
I/O leakage current	$\lvert I_{IL} \rvert$	D_0–D_7	—	—	1.0	µA	V_{in} = 0 to V_{CC}	1
Pull-up MOS current	$-I_P$	D_0–D_7	5	25	90	µA	V_{CC} = 3.0, V_{in} = 0	

Note: 1. Output buffer current is excluded.

LCD Circuit Characteristics (HD404328: V_{CC} = 2.7 to 6.0 V, HD4074329: V_{CC} = 3.0 to 5.5 V; GND = 0.0 V; Ta = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Segment driver voltage drop	V_{ds}	SEG1–SEG24	—	—	0.6	V	I_d = 3.0 µA	1
Common driver voltage drop	V_{dc}	COM1–COM4	—	—	0.3	V	I_d = 3.0 µA	1
LCD power supply division resistor	R_{well}		100	300	900	kΩ	Between V_1 and GND, V_1 = V_{CC}	
LCD voltage	V_{LCD}	V_1	3.0	—	V_{CC}	V		2, 3

Notes: 1. V_{ds} and V_{dc} are the voltage drops from power supply pins V_1, V_2, and V_3, and GND to each segment pin and each common pin.
2. When V_{LCD} is supplied from an external source, the following relations must be retained: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq$ GND
3. The minimum value of V_{LCD} in the HD404328 is 2.7 V.

A/D Converter Characteristics (V_{CC} = 5.0 V ± 10%, AV_{SS} = 0.0 V, Ta = 0°C to +70°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Analog power voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		
Analog input voltage	AV_{in}	AN_0–AN_3	AV_{SS}		AV_{CC}	V		
Current between AV_{CC} and AV_{SS}	I_{AD}	—	—	50	—	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0–AN_3	—	TBD	—	pF		
Resolution			8	8	8	Bit		
Number of inputs			0	—	4	Channel		
Absolute accuracy			—	—	± 2.0	LSB	Ta = 25°C f_{OSC} = 1.0–4.5 MHz	1
Conversion period			34	—	67	t_{cyc}		
Analog input impedance		AN_0–AN_3	1	—	—	MΩ	f = 1 MHz, V_{in} = 0.0V	

Note: 1. Operating frequency of A/D conversion "f_{OSC}" is from 1 (MHz) to 4.5 (MHz).

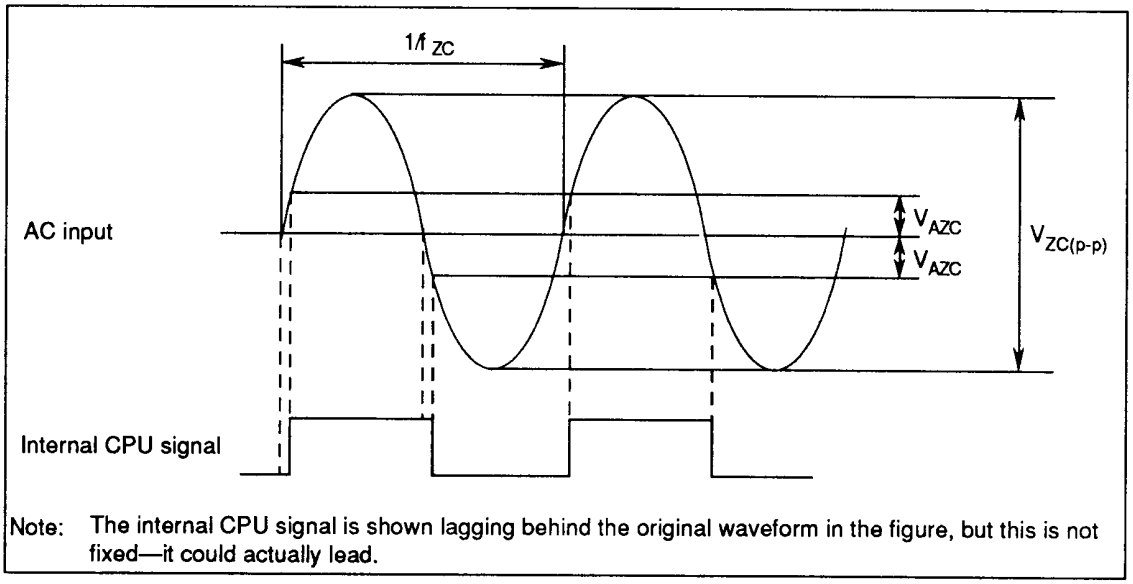
Zero-Crossing Detection Circuit Characteristics

Low Sensitivity Mode (HD404328: V_{CC} = 2.7 to 6.0 V, HD4074329: V_{CC} = 3.0 to 5.5 V; GND = 0.0 V; Ta = 0°C to +70°C; unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Zero-crossing detection input voltage	V_{ZC}	ZCD	2.0	—	3.0	V_{P-P}	AC connection, C = 0.1 µF	
Zero-crossing detection accuracy	V_{AZC}		—	—	± 750	mV	f_{ZC} = 50 Hz (sine wave) f_{OSC} = 4 MHz V_{CC} = 5.0 V	Refer to Figure 50
Zero-crossing detection input frequency	f_{ZC}		45	—	250	Hz		

High Sensitivity Mode (V_{CC} = 5.0 V ± 10%, GND = 0.0 V, Ta = 0°C to +70°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Zero-crossing detection input voltage	V_{ZC}	ZCD	1.0	—	3.0	V_{P-P}	AC connection, C = 0.1 µF	
Zero-crossing detection accuracy	V_{AZC}		—	—	± 100	mV	f_{ZC} = 50 Hz (sine wave) f_{OSC} = 4 MHz V_{CC} = 5.0 V	Refer to Figure 50
Zero-crossing detection input frequency	f_{ZC}		45	—	1000	Hz		



Note: The internal CPU signal is shown lagging behind the original waveform in the figure, but this is not fixed—it could actually lead.

Figure 50 Zero-Crossing Detection

AC Characteristics (HD404328: V_{CC} = 2.7 to 6.0 V, HD4074329: V_{CC} = 3.0 to 5.5 V; GND = 0.0 V; Ta = –20°C to +75°C; unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4.0	4.5	MHz	1/8 division, 32 kHz used	1
			0.4	4.0	4.5	MHz	1/8 division used, 32 kHz not used	
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		—	2	—	µs	f_{OSC} = 4 MHz	
Oscillation stabilization time (crystal)	t_{RC}	OSC_1, OSC_2	—	—	40	ms	V_{CC} = 3.5 to 6.0 V	2
			—	—	60	ms		2
Oscillation stabilization time (ceramic filter)	t_{RC}	OSC_1, OSC_2	—	—	20	ms	V_{CC} = 3.5 to 6.0 V	2
			—	—	60	ms		2
Oscillation stabilization time	t_{RC}	X1, X2	—	—	3	s		3
External clock high width	t_{CPH}	OSC_1	90	—	—	ns		4
External clock low width	t_{CPL}	OSC_1	90	—	—	ns		4
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		4
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		4
$\overline{INT_0}$, INT_1, $\overline{EVENT}$ high width	t_{IH}	$\overline{INT_0}$, INT_1, $\overline{EVENT}$	2	—	—	t_{cyc}/ t_{SUBcyc}		5, 6
$\overline{INT_0}$, INT_1, $\overline{EVENT}$ width	t_{IL}	$\overline{INT_0}$, INT_1, $\overline{EVENT}$	2	—	—	t_{cyc}/ t_{SUBcyc}		5, 6
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		7
RESET fall time	t_{RSTf}	RESET	—	—	20	ms		7
Input capacitance	C_{in}	D_{10}	—	—	TBD	pF	f = 1 MHz, V_{in} = 0.0 V	
		All pins except D_{10}, AN_0–AN_3	—	—	15	pF	f = 1 MHz, V_{in} = 0.0 V	

Notes:
1. If f_{OSC} = 0.4 to 1.0 MHz, bit 3 of the miscellaneous register (MIS: $00C) must be set to 1; if f_{OSC} = 1.6 to 4.5 MHz, bit 3 must be set to 0. Do not use f_{OSC} = 1.0 to1.6 MHz with 32-kHz oscillation.
2. The oscillation stabilization time is the time required for the oscillator to stabilize after V_{CC} reaches 2.7 V (3.0 V for the HD4074329, or 3.5 V if V_{CC} = 3.5 to 6.0 V) at power-on or after RESET input goes high after stop mode is canceled. At power-on and when stop mode is canceled, RESET must be input for at least t_{RC} to ensure the oscillation stabilization time. If using a crystal oscillator or a ceramic filter oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitances.
3. The oscillation stabilization time is the time required for the oscillator to stabilize after V_{CC} reaches 2.7 V (3.0 V for the HD4074329) at power-on—at least t_{RC} must be ensured. If using a 32.768 kHz crystal oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitances.
4. Refer to figure 51.
5. Refer to figure 52. The t_{cyc} unit applies when the MCU is in standby or active mode.
6. Refer to figure 52. The t_{SUBcyc} unit applies when the MCU is in watch or subactive mode. t_{SUBcyc} = 244.14 µs (32.768-kHz crystal)
7. Refer to figure 53.

Serial Interface Timing Characteristics (HD404328: V_{CC} = 2.7 to 6.0 V, HD4074329: V_{CC} = 3.0 to 5.5 V; GND = 0.0 V; Ta = –20°C to +75°C; unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1.0	—	—	t_{cyc}	Load shown in figure 55	1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.3	—	—	t_{Scyc}	Load shown in figure 55	1, 2
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.3	—	—	t_{Scyc}	Load shown in figure 55	1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns	V_{CC} = 3.5 to 6.0 V, load shown in figure 55	1, 2
			—	—	200	ns	Load shown in figure 55	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns	V_{CC} = 3.5 to 6.0 V, load shown in figure 55	1, 2
			—	—	200	ns	Load shown in figure 55	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	V_{CC} = 3.5 to 6.0 V, load shown in figure 55	1, 2
			—	—	500	ns	Load shown in figure 55	1, 2
Serial input data setup time	t_{SSI}	SI	200	—	—	ns	V_{CC} = 3.5 to 6.0 V	1
			300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	V_{CC} = 3.5 to 6.0 V	1
			300	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1.0	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.3	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.3	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns	V_{CC} = 3.5 to 6.0 V	1
			—	—	200	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns	V_{CC} = 3.5 to 6.0 V	1
			—	—	200	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	V_{CC} = 3.5 to 6.0 V, load shown in figure 55	1, 2
			—	—	500	ns	Load shown in figure 55	1, 2
Serial input data setup time	t_{SSI}	SI	200	—	—	ns	V_{CC} = 3.5 to 6.0 V	1
			300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	V_{CC} = 3.5 to 6.0 V	1
			300	—	—	ns		1

Notes: 1. Refer to figure 54.
2. Refer to figure 55.

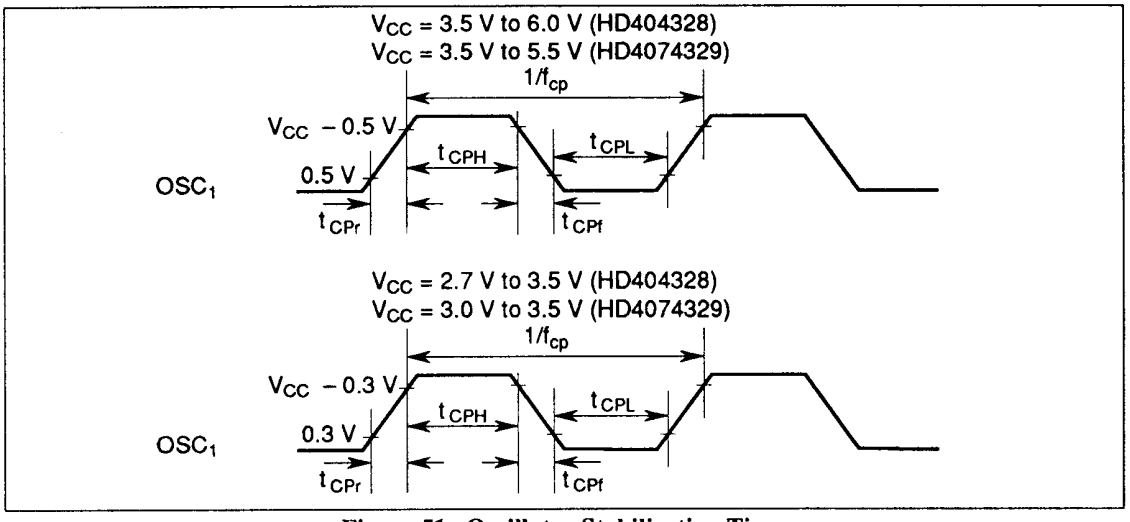


Figure 51 Oscillator Stabilization Time

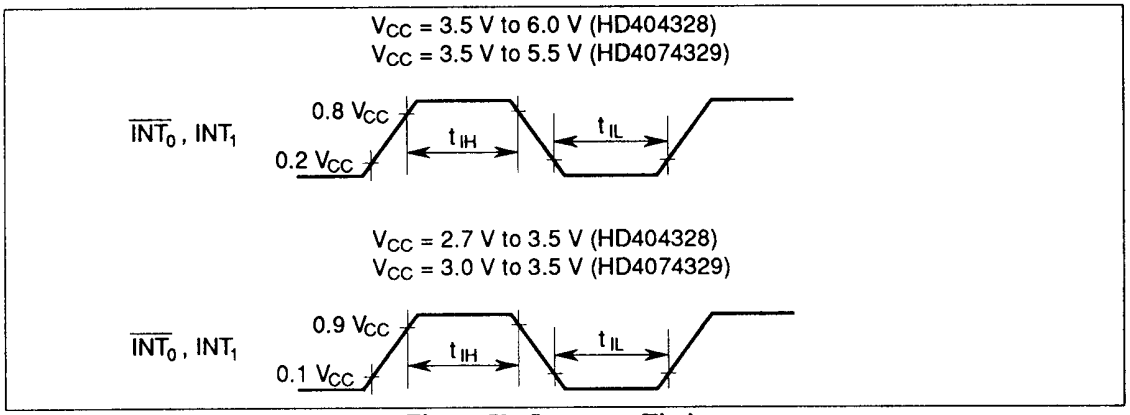


Figure 52 Interrupt Timing

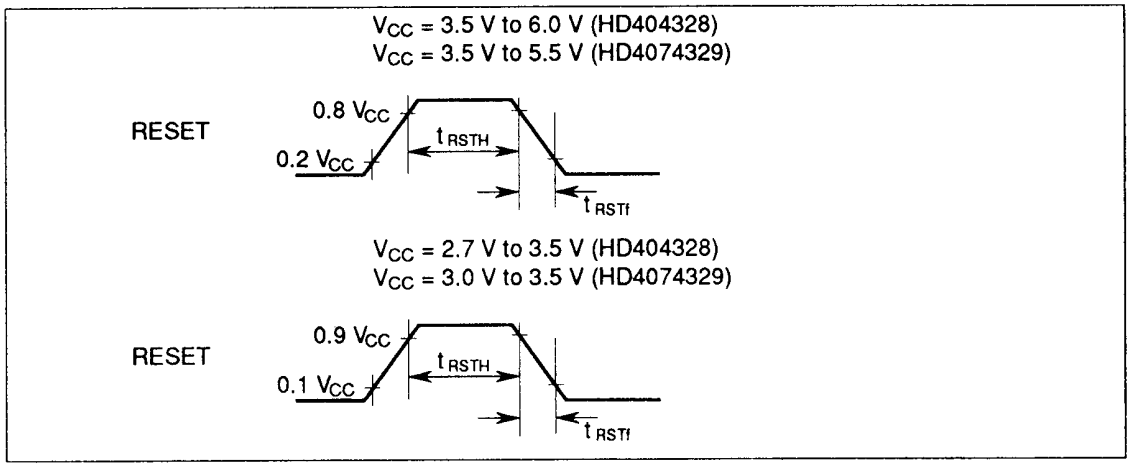


Figure 53 Reset Timing

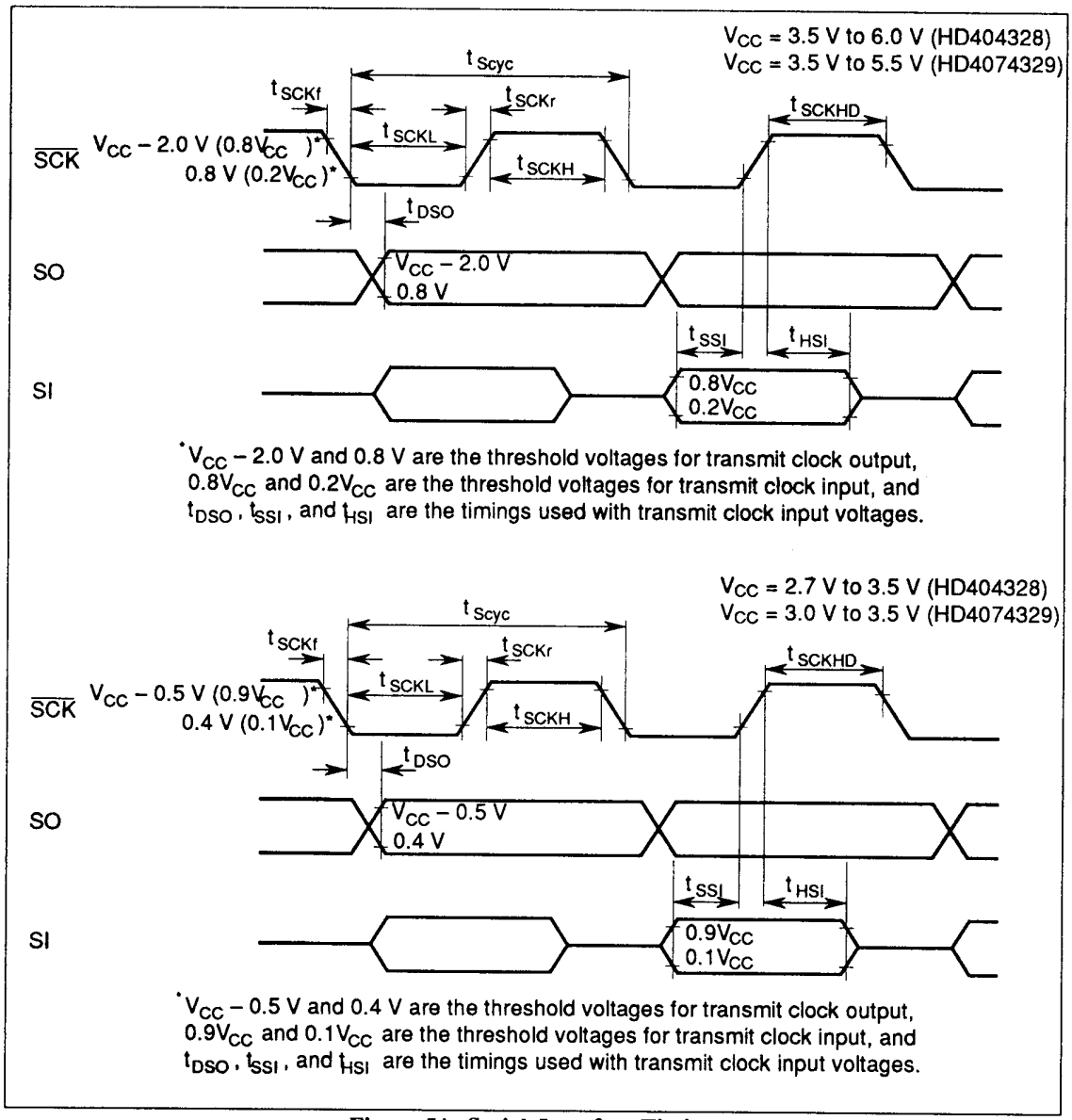


Figure 54 Serial Interface Timing

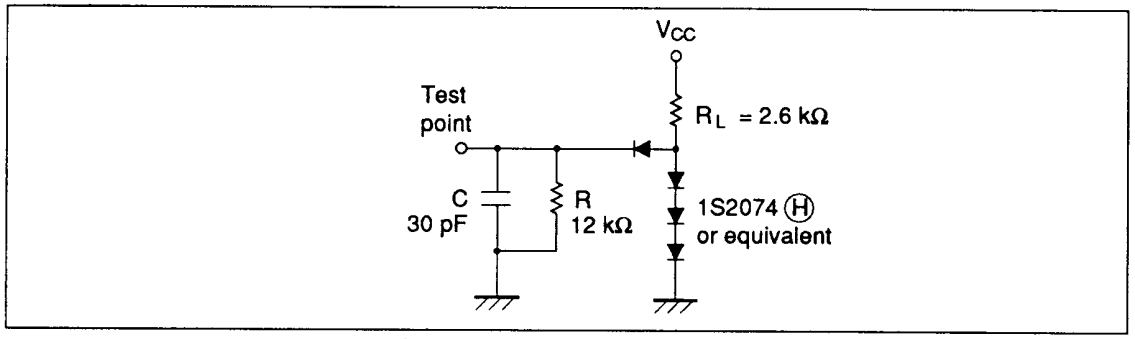


Figure 55 Timing Load Circuit

HD404328 Option List

Please enter check marks (■, ×, or ✔) in boxes by applicable items.

Packages

☐ DP–64S
☐ FP–64B

Date of order	/ /19
Customer	
Department	
ROM code name	
LSI number (to be filled in by Hitachi)	

Optional Functions

☐ With 32-kHz CPU operation
☐ Without 32-kHz CPU operation, with time-base for clock
☐ Without 32-kHz CPU operation, without time-base
☐ With zero-crossing detection function
☐ Without zero-crossing detection function

ROM Code Media

☐ EPROM: Emulator type
☐ HD4074329

Usage Conditions Check

Oscillator for OSC_1 and OSC_2

☐ Ceramic filter	f =	MHz
☐ Crystal	f =	MHz
☐ External clock	f =	MHz

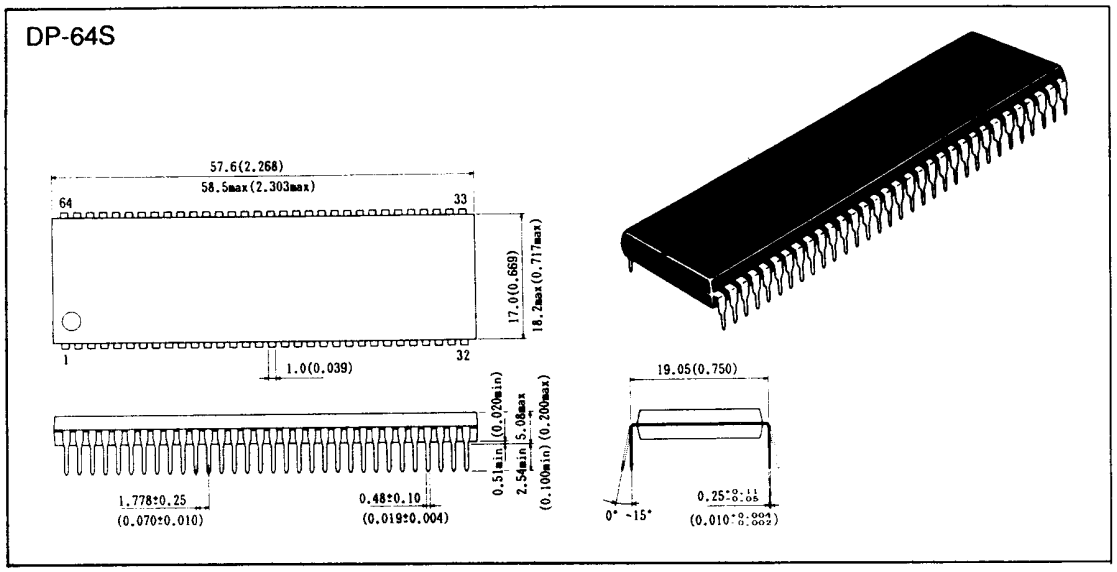
Oscillator for X1 and X2

☐ Not used	—
☐ Crystal	f = 32.768 kHz

Package Dimensions

Unit: mm (inch)

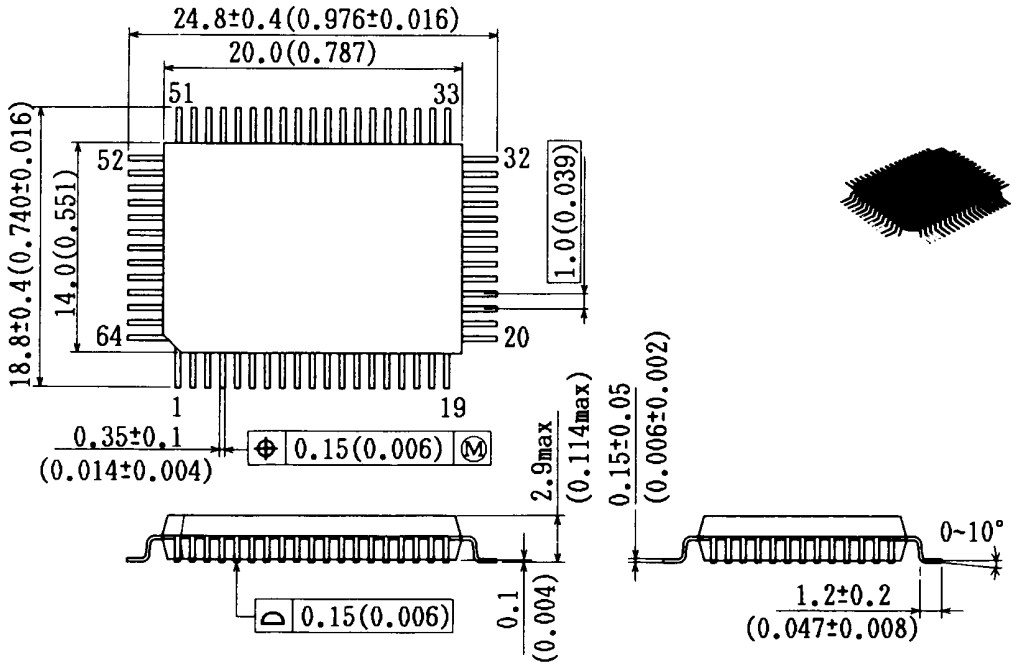
DP-64S



Package Dimensions

Unit: mm (inch)

FP-64B



DC-64S