HD44100R
(LCD Driver with 40-Channel Outputs)

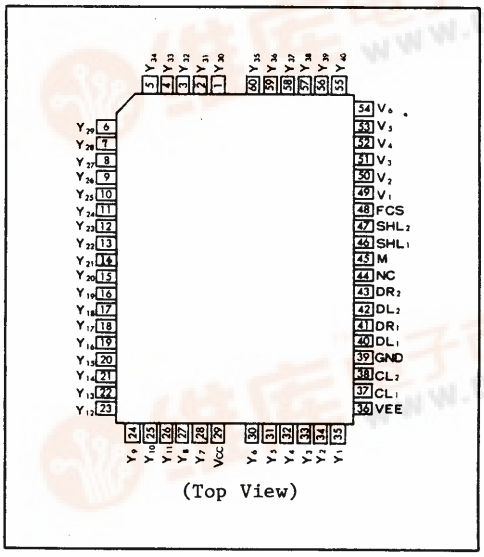
— Preliminary —

Description

The HD44100R has two sets of 20-bit bidirectional shift registers, 20 data latch flipflops and 20 liquid crystal display driver circuits. It receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.

The HD44100R is a highly general liquid crystal display driver which can drive a static drive liquid crystal and a dynamic drive liquid crystal, and can be applied as a common driver or segment driver.

Pin Arrangement



(Top View)

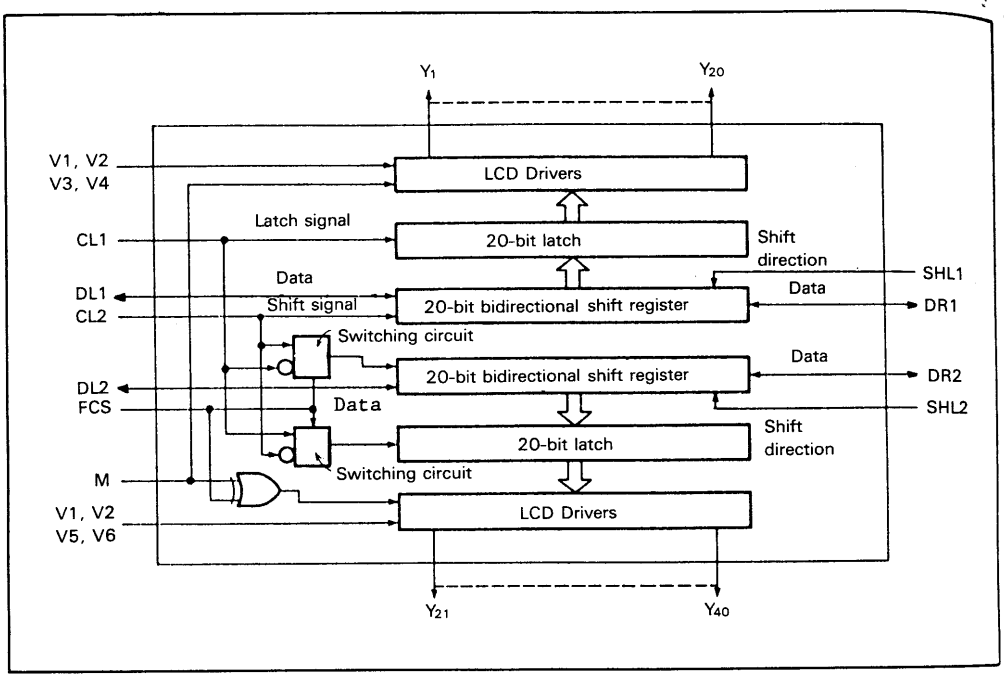
Features

- Liquid crystal display driver with serial/parallel conversion function
- Serial transfer facilitates board design
- Capable of interfacing to liquid crystal display controllers: HD43160AH, LCTC (HD61830/61830B), LCD-II (HD44780S, HD44780U), LCD-IIA (HD66780), LCD-II/E (HD66702), LCD-III (HD44790), HD66710
- 40 internal liquid crystal display drivers
- Internal serial/parallel conversion circuits:
  —20-bit shift register × 2
  —20-bit data latch × 2
- Display bias: Static to 1/5
- Power supply:
  —Internal logic: V_{CC} = 2.7 to 5.5V
  —Liquid crystal display driver circuit: $V_{CC} - V_{EE}$ = 3 to 13V
- Separation of internal logic from liquid crystal display driver circuit increases applicable controllers and liquid crystal types
- CMOS process

Ordering Information

Type No.	V_{CC} (V)	$V_{CC} - V_{EE}$ (V)	Package
HD44100RFS	2.7 to 5.5	3 to 13	60-pin Plastic QFP (FP-60A)
HCD44100R	2.7 to 5.5	3 to 13	Chip

Block Diagram



Absolute Maximum Ratings

Item		Symbol	Value	Unit
Supply voltage	Logic	V_{CC} *1	− 0.3 to + 7.0	V
	LCD drivers	V_{EE} *2	V_{CC} − 15.0 to V_{CC} + 0.3	V
Input voltage		V_{T1} *1	− 0.3 to V_{CC} + 0.3	V
Input voltage		V_{T2} *3	V_{CC} + 0.3 to V_{EE} − 0.3	V
Operating temperature		T_{opr}	− 20 to + 75	°C
Storage temperature		T_{stg}	− 55 to + 125	°C

Notes: *1 All voltage values are referred to GND.
*2 Connect a protection resistor of 220 Ω ± 5 % to V_{EE} power supply in series.
*3 Applies to V_1 to V_6.

Electrical Characteristics

(V_{CC} = 2.7 to 5.5 V, $V_{CC} - V_{EE}$ = 3 to 13 V, GND = 0 V, T_a = − 20 to + 75°C)

Item	Symbol	Applicable Terminals	Min	Typ	Max	Unit	Test Condition
Input voltage	V_{IH}	CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS	0.7 V_{CC}	—	V_{CC}	V	V_{CC}=4.5 to 5.5V
			0.8 V_{CC}	—	V_{CC}	V	V_{CC}=2.7 to 4.5V
	V_{IL}		0	—	0.3 V_{CC}	V	V_{CC}=4.5 to 5.5V
			0	—	0.2 V_{CC}	V	V_{CC}=2.7 to 4.5V
Output voltage	V_{OH}	DL1, DL2, DR1, DR2	V_{CC} − 0.4	—	—	V	I_{OH} = − 0.4 mA
	V_{OL}		—	—	0.4	V	I_{OL} = + 0.4 mA
On resistance	R_{ON}	*1	—	—	20	kΩ	±I_d = 0.05 mA, $V_{CC}-V_{EE}$=4V
Input leakage current	I_{IL}	CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS, NC	− 5.0	—	5.0	μA	V_{in} = 0 to V_{CC}
Vi leakage current	I_{VL}	*2	− 10.0	—	10.0	μA	V_{in} = V_{CC} to V_{EE}
Power supply current	I_{CC}	*3	—	—	1.0	mA	f_{CL2} = 400 kHz
	I_{EE}		—	—	10	μA	f_{CL1} = 1 kHz

Notes: *1 Applies to the resistance between V_i and Y_j when a current ± I_d = 0.05 mA flows through all of the Y pins.

*2 Output Y1 to Y40 open.

*3 Input/output current is excluded; when input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

Timing Characteristics

(V_{CC} = 2.7 to 5.5 V, V_{CC} − V_{EE} = 3 to 13 V, GND = 0 V, T_a = − 20 to + 75°C)

Item	Symbol	Applicable Terminals	Min	Typ	Max	Unit	Test Condition
Data shift frequency	f_{CL}	CL2	—	—	400	kHz	
Clock high level width Low level	t_{CWH}	CL1, CL2	800	—	—	ns	
	t_{CWL}	CL2	800	—	—	ns	
Data set-up time	t_{SU}	DL1, DL2, DR1, DR2, FLM	300	—	—	ns	
Clock set-up time	t_{SL}	CL1, CL2	500	—	—	ns	(CL2→CL1)
Clock set-up time	t_{LS}	CL1, CL2	500	—	—	ns	(CL1→CL2)
Data delay time	t_{pd}	DL1, DL2, DR1, DR2	—	—	500	ns	C_L = 15 pF
Clock rise/fall time	t_{ct}	CL1, CL2	—	—	200	ns	
Data hold time	t_{DH}	DL1, DL2, DR1, DR2, FLM	300	—	—	ns	

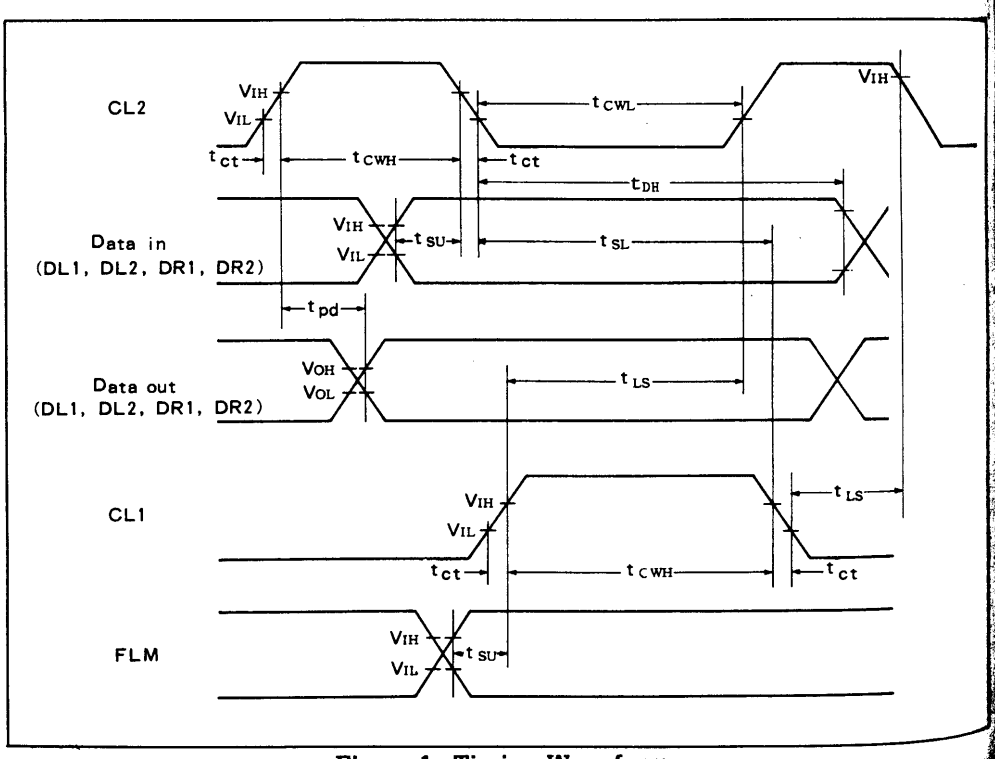


Figure 1 Timing Waveform

Terminal Function

Table 1 Functional Description of Terminals

Signal Name	Number of Lines	Input/ Output	Connected to	Function
V_{CC}	1		power supply	Power supply for logical circuit
GND	1		Power supply	0 V
V_{EE}	1		Power supply	Power supply for liquid crystal display drive
Y_1–Y_{20}	20	Output	Liquid crystal	Liquid crystal driver output (Channel 1)
Y_{21}–Y_{40}	20	Output	Liquid crystal	Liquid crystal driver output (Channel 2)
V_1, V_2	2	Input	Power supply	Power supply for liquid crystal display drive (Select level)
V_3, V_4	2	Input	Power supply	Power supply for liquid crystal display drive (Non-select level for channel 1)
V_5, V_6	2	Input	Power supply	Power supply for liquid crystal display drive (Non-select level for channel 2)
SHL1	1	Input	V_{CC} or GND	Selection of the shift direction of channel 1 shift register SHL1 = V_{CC}: DL1 Out, DR1 In SHL1 = GND: DL1 In, DR1 Out
SHL2	1	Input	V_{CC} or GND	Selection of the shift direction of channel 2 shift register SHL2 = V_{CC}: DL2 Out, DR2 In SHL2 = GND: DL2 In, DR2 Out
DL1, DR1	2	Input/ output	Controller or HD44100R	Data input/output of channel 1 shift register
DL2, DR2	2	Input/ output	Controller or HD44100R	Data input/output of channel 2 shift register
M	1	Input	Controller	Alternated signal for liquid crystal driver output
CL1	1	Input	Controller	Latch signal for channel 1 (⌐¬) *1 Used for channel 2 when FCS is GND
CL2	1	Input	Controller	Shift signal for channel 1 (⌐¬) *1 Used for channel 2 when FCS is GND
FCS	1	Input	V_{CC} or GND	Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift signal of channel 2 and inverts M for channel 2. Thus, this signal exchanges the function of channel 2.

	Channel 2			
FCS Level	Latch signal	Shift signal	M Polarity	Function
V_{CC}	CL2 ⌐¬	CL1 ⌐¬	$\overline{M}$	For common drive
GND	CL1 ⌐¬	CL2 ⌐¬	M	For segment drive
	*1	*1		*2

NC	1	Don't connect any wires to this terminal.

Notes: *1 ⌐¬ and ⌐¬ indicate the latches at rise and fall times, respectively.
*2 The output level relationship between channel 1 and channel 2 based on the FCS signal level is as follows:

FCS	Data	M	Output Level: Channel 1 (Y_1—Y_{20})	Output Level: Channel 2 (Y_{21}—Y_{40})
	1	1	V_1	V_2
V_{CC}	(Select)	0	V_2	V_1
(1)	0	1	V_3	V_6
	(Non-select)	0	V_4	V_5
	1	1	V_1	V_1
GND	(Select)	0	V_2	V_2
(0)	0	1	V_3	V_5
	(Non-select)	0	V_4	V_6

1 and 0 indicate high and low levels, respectively.

Applications

Segment Driver

When the HD44100R is used as a segment driver, FCS is set to GND to transfer display data with the timing shown in figure 2. In this case, both channel 1 and channel 2 shift data at the fall of CL2 and latch it at the fall of CL1. V_3 and V_5, V_4 and V_6 of the liquid crystal display driver power supply are short-circuited, respectively.

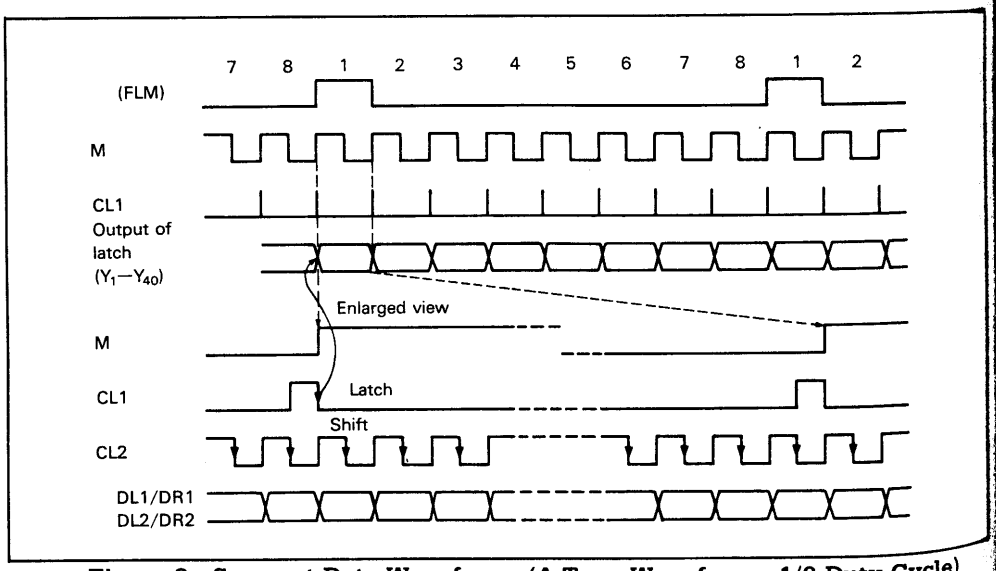


Figure 2 Segment Data Waveforms (A Type Waveforms, 1/8 Duty Cycle)

Common Driver

In this case, channel 1 is used as a segment driver and channel 2 as common driver. When channel 2 of HD44100R is used as common driver, FCS is set to V_{CC} to transfer display data with the timing shown in figure 3.

In this case, channel 2 shifts data at the rise of CL1 and latches it at the rise of CL2. Channel 1 shifts and latches as shown in figure 2.

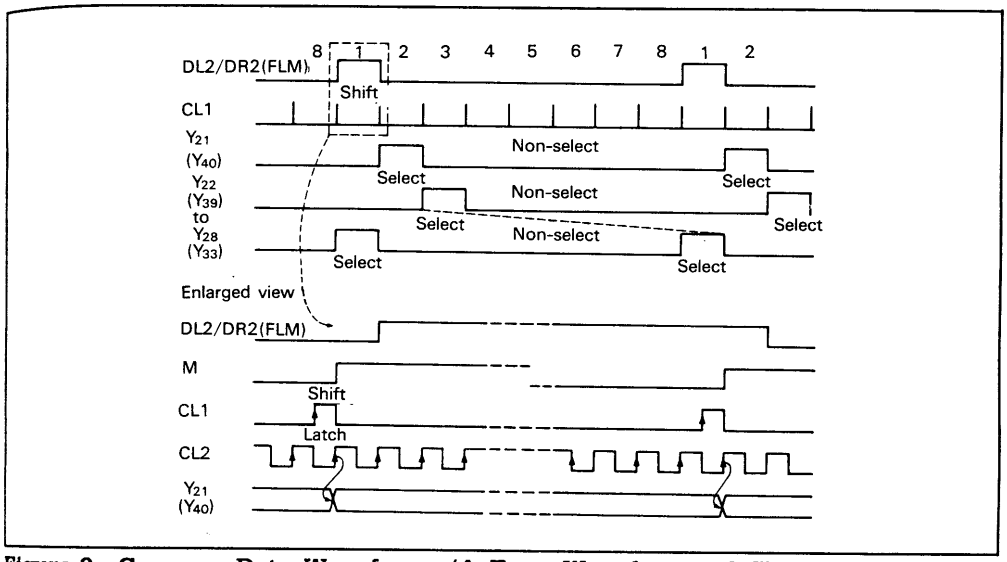


Figure 3 Common Data Waveforms (A Type Waveforms of Channel 2, 1/8 Duty Cycle)

Both Channel 1 and Channel 2 Used as Common Drivers (FCS = GND)

When both of channel 1 and channel 2 of HD44100R are used common drivers, FCS is set to GND and the signals (CL1, CL2, FLM) from the controller are connected as shown in figure 4.
In this case, connection of the liquid crystal display driver power supply is different from that of segment driver, so refer to figure 4.

- V_1, V_2: Select level of segment and common
- V_3, V_4: Non-select level of segment
- V_5, V_6: Non-select level of common

Static Drive

When the HD44100R is used in the static drive method (figure 5), data is transferred at the fall of CL2 and latched at the fall of CL1. The frequency of CL1 becomes the frame frequency of the liquid crystal display driver. The signal applied terminal M must have twice the frequency of CL1 and be synchronized at the fall of CL1. The power supply for liquid crystal display driver is used by short-circuiting V_1, V_4 and V_6, and V_2, V_3, and V_5 respectively.
One of the liquid crystal display driver output terminals can be used for a common output. In this case, FCS is set to GND and data is transferred so that 0 can be always latched in the latch corresponding to the liquid crystal display driver output terminal used as the common output. If the latch signal corresponding to the segment output is 1, the segments of LCD light. They also light for common side = 1, and segment side 0.

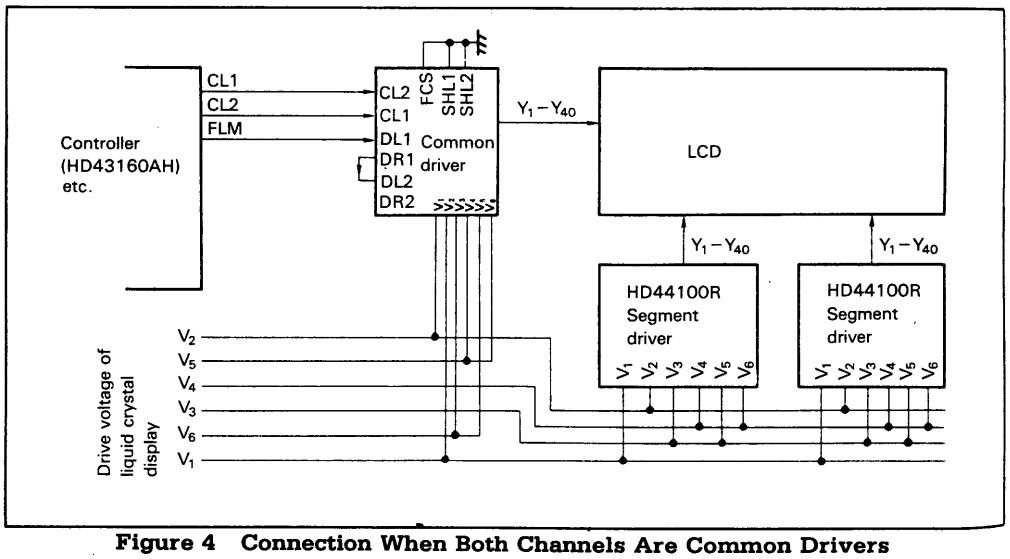


Figure 4 Connection When Both Channels Are Common Drivers

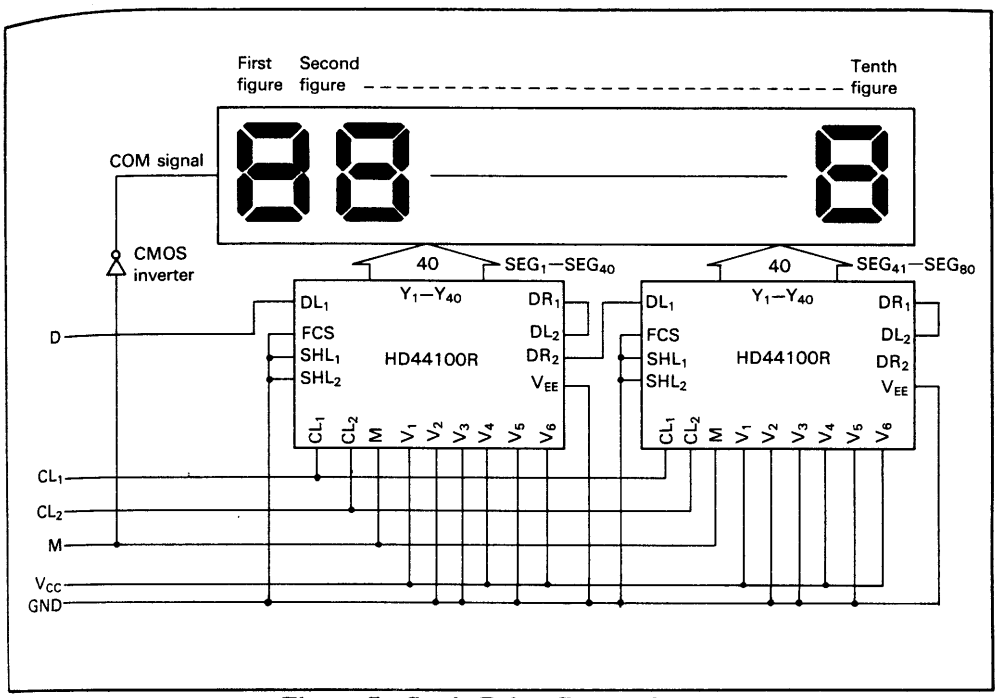
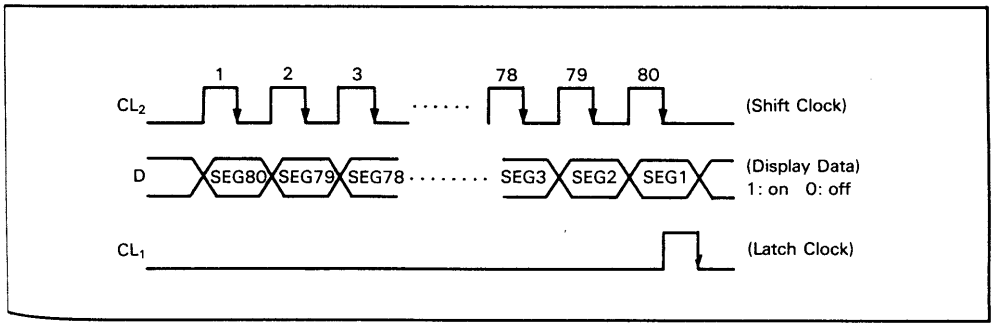


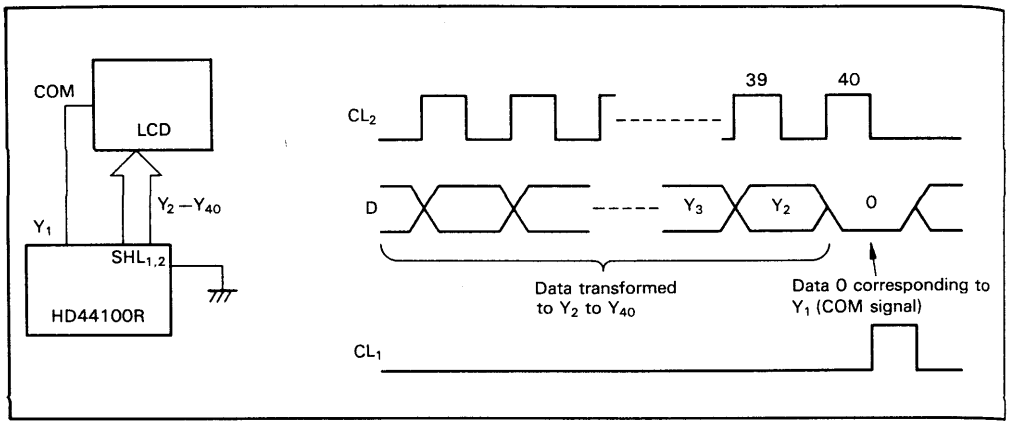
Figure 5 Static Drive Connection

Timing Chart of Input Waveforms



Notes:

1. Input square waves of 50% duty cycle (about 30—500 Hz) to M. The frequency depends on the specifications of LCD panels.
2. The drive waveforms corresponding to the new displayed data are output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid this, have CL1 fall synchronously with the one edge of M.
3. In this example, the CMOS inverter is used as a COM signal driver in consideration of the large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
   Usually, one of the HD44100R outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.


COM
LCD
Y_1
$Y_2 - Y_{40}$
$SHL_{1,2}$
HD44100R
CL_2
39
40
D
Y_3
Y_2
0
Data transformed to Y_2 to Y_{40}
Data 0 corresponding to Y_1 (COM signal)
CL_1