Dual 4-Input Multiplexer

HITACHI

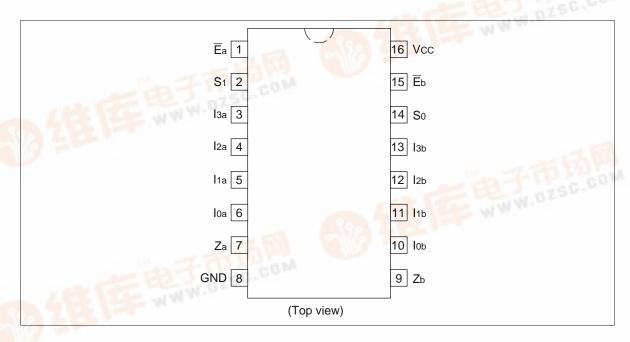
Description

The HD74AC153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (noninverted) form. In addition to multiplexer operation, the HD74AC153 can act as a function generator and generate any two functions of three variables.

Feature

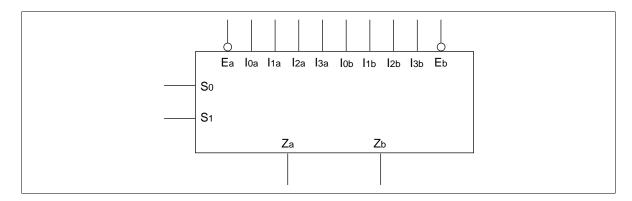
• Outputs Source/Sink 24 mA

Pin Arrangement





Logic Symbol



Pin Names

I_{0a} to I_{3a} Side A Data Inputs

 I_{0b} to $I_{3b}\,$ Side B Data Inputs

S₀, S₁ Common Select Inputs

 \overline{E}_{a} Side A Enable Input

 \overline{E}_b Side B Enable Input

Z_a Side A Output

Z_b Side B Output

Functional Description

The HD74AC153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1) . The two 4-input multiplexer circuits have individual active-Low Enables $(\overline{E}_a, \overline{E}_b)$ which can be used to strobe the outputs independently. When the Enables $(\overline{E}_a, \overline{E}_b)$ are High, the corresponding outputs (Z_a, Z_b) are forced Low. The HD74AC153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$\begin{split} Z_a &= \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0) \\ Z_b &= \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0) \end{split}$$

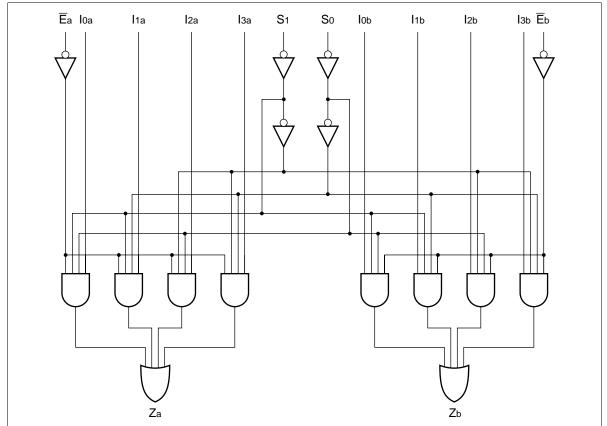
Truth Table

Select Inputs		Input (a	Input (a or b)							
S ₀	S ₁	Ē	I _o	I ₁	l ₂	I ₃	Z			
X	Х	Н	Х	Х	Х	Х	L			
L	L	L	L	Χ	Χ	Χ	L			
L	L	L	Н	Х	Х	Х	Н			
Н	L	L	Х	L	Х	Х	L			
Н	L	L	Х	Н	Х	Х	Н			
L	Н	L	Х	Х	L	Χ	L			
L	Н	L	Х	Х	Н	Х	Н			
Н	Н	L	Х	Х	Х	L	L			
Н	Н	L	Х	Х	Х	Н	Н			

H: High Voltage Level
L: Low Voltage Level

X : Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I _{cc}	80	μΑ	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, Ta = Worst case
Maximum quiescent supply current	I _{cc}	8.0	μΑ	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, $Ta = 25^{\circ}\text{C}$

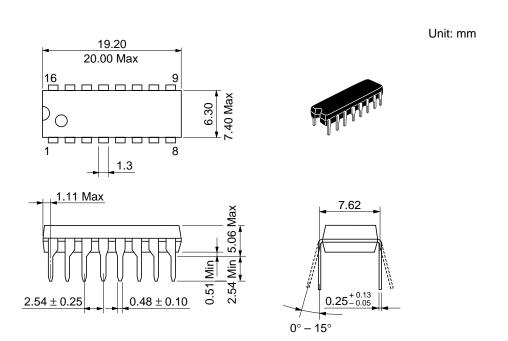
AC Characteristics: HD74AC153

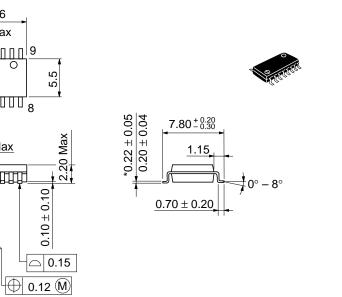
			Ta = + C _∟ = 50			Ta = −4 C _L = 50	0°C to +85°C pF	
Item	Symbol	V _{cc} (V)*1	Min	Тур	Max	Min	Max	Unit
Propagation delay	t _{PLH}	3.3	1.0	9.5	15.0	1.0	17.5	ns
S_n to Z_n		5.0	1.0	6.5	11.0	1.0	12.5	_
Propagation delay	t _{PHL}	3.3	1.0	8.5	14.5	1.0	16.5	ns
S_n to Z_n		5.0	1.0	6.5	11.0	1.0	12.0	
Propagation delay	t _{PLH}	3.3	1.0	8.0	13.5	1.0	16.0	ns
\overline{E}_{n} to Z_{n}		5.0	1.0	5.5	9.5	1.0	11.0	
Propagation delay	t _{PHL}	3.3	1.0	7.0	11.0	1.0	12.5	ns
\overline{E}_n to Z_n		5.0	1.0	5.0	8.0	1.0	9.0	
Propagation delay	t _{PLH}	3.3	1.0	7.5	12.5	1.0	14.5	ns
I_n to Z_n		5.0	1.0	5.5	9.0	1.0	10.5	_
Propagation delay	t _{PHL}	3.3	1.0	7.0	11.5	1.0	13.0	ns
I_n to Z_n		5.0	1.0	5.0	8.5	1.0	10.0	

Note: 1. Voltage Range 3.3 is 3.3 V \pm 0.3 V Voltage Range 5.0 is 5.0 V \pm 0.5 V

Capacitance

Item	Symbol	Тур	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	65.0	pF	$V_{CC} = 5.0 \text{ V}$





10.06 10.5 Max 16 7 7 9

1 00000008

0.80 Max

1.27

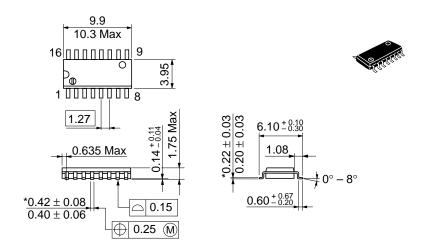
 $^{*}0.42 \pm 0.08$ 0.40 ± 0.06

5.5

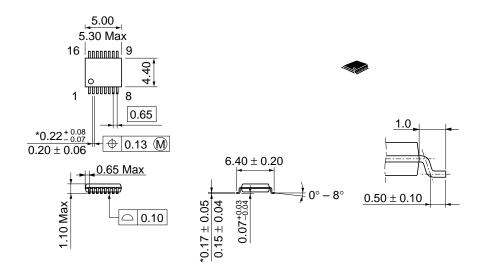
 $\boldsymbol{0.10\pm0.10}$

Unit: mm









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