

# HD74AC157

## Quad 2-Input Multiplexer

# HITACHI

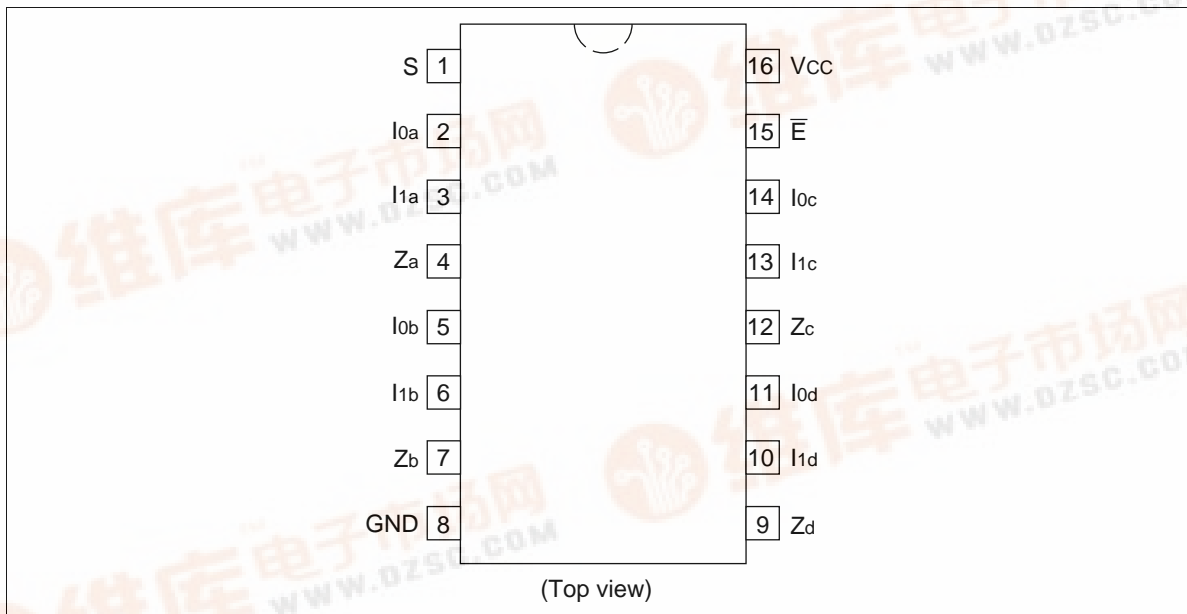
### Description

The HD74AC157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The HD74AC157 can also be used as a function generator.

### Feature

- Outputs Source/Sink 24 mA

### Pin Arrangement

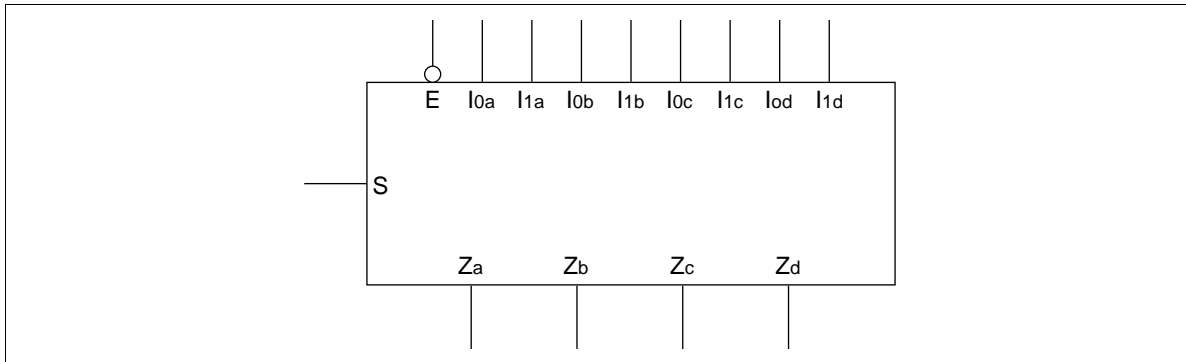


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## HD74AC157

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### Logic Symbol



### Pin Names

$I_{0a}$ to $I_{0d}$	Source 0 Data Inputs
$I_{1a}$ to $I_{1d}$	Source 1 Data Inputs
$\bar{E}$	Enable Input
S	Select Input
$\bar{Z}_a$ to $\bar{Z}_d$	Outputs

### Functional Description

The HD74AC157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ( $\bar{E}$ ) is active-Low. when  $\bar{E}$  is High, all of the outputs (Z) are forced Low regardless of all other inputs. The HD74AC157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\begin{aligned}Z_a &= \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\Z_b &= \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\Z_c &= \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\Z_d &= \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})\end{aligned}$$

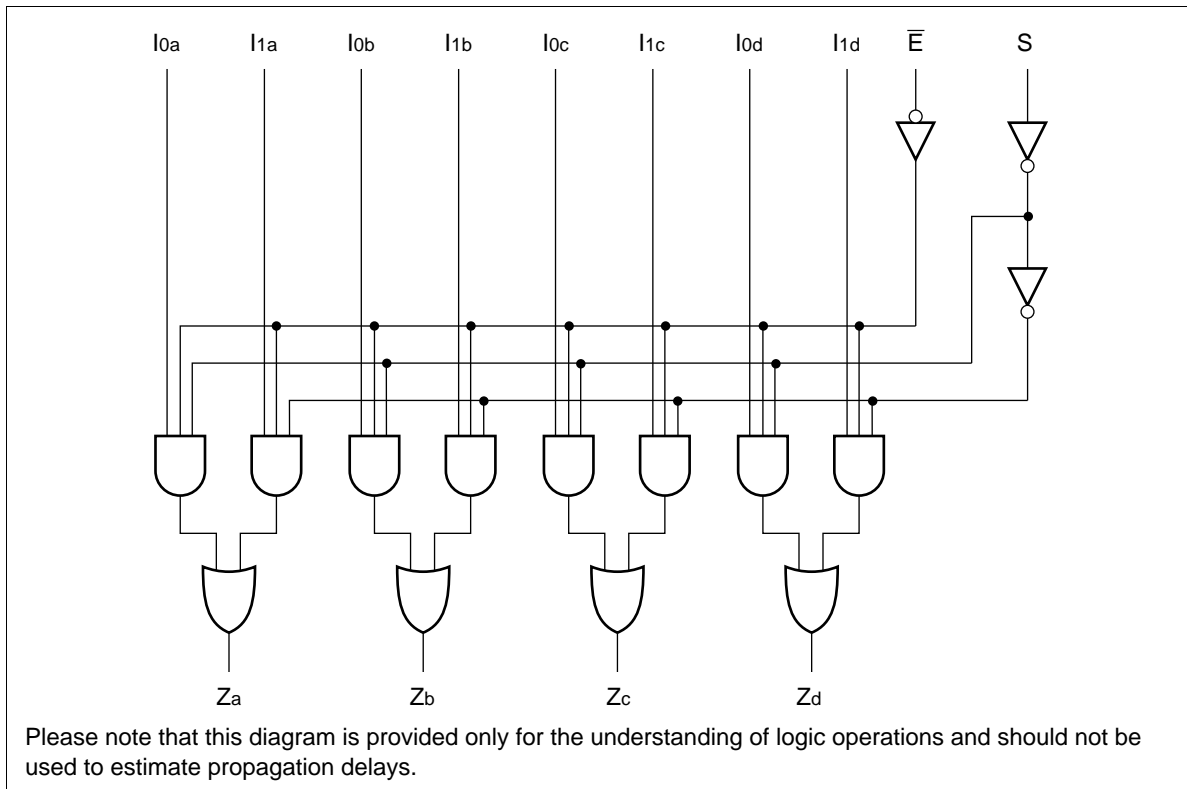
A common use of the HD74AC157 is the moving of data from two groups of register to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The HD74AC157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

**Truth Table**

Inputs				Output
<b>E</b>	<b>S</b>	<b>I<sub>0</sub></b>	<b>I<sub>1</sub></b>	<b>Z</b>
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H : High Voltage Level  
 L : Low Voltage Level  
 X : Immaterial

**Logic Diagram**



## HD74AC157

### DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	$I_{CC}$	80	$\mu\text{A}$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$ , $T_a = \text{Worst case}$
Maximum quiescent supply current	$I_{CC}$	8.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$ , $T_a = 25^\circ\text{C}$

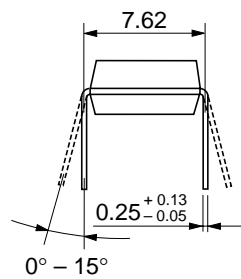
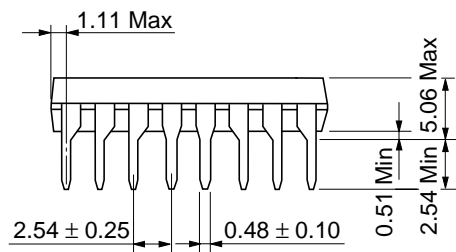
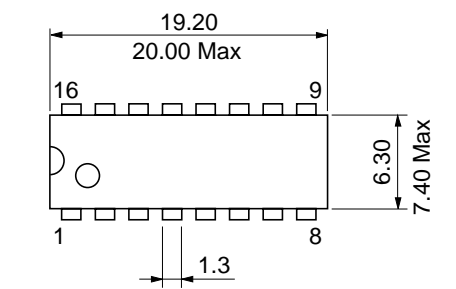
### AC Characteristics: HD74AC157

Item	Symbol	$V_{CC} (\text{V})^{*1}$	$T_a = +25^\circ\text{C}$ $C_L = 50\text{ pF}$			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$		Unit
			Min	Typ	Max	Min	Max	
Propagation delay S to $Z_n$	$t_{PLH}$	3.3	1.0	7.0	11.5	1.0	13.0	ns
		5.0	1.0	5.5	9.0	1.0	10.0	
Propagation delay S to $Z_n$	$t_{PHL}$	3.3	1.0	6.5	11.0	1.0	12.0	ns
		5.0	1.0	5.0	8.5	1.0	9.5	
Propagation delay $\bar{E}$ to $Z_n$	$t_{PLH}$	3.3	1.0	7.0	11.5	1.0	13.0	ns
		5.0	1.0	5.5	9.0	1.0	10.0	
Propagation delay $\bar{E}$ to $Z_n$	$t_{PHL}$	3.3	1.0	6.5	11.0	1.0	12.0	ns
		5.0	1.0	5.5	9.0	1.0	9.5	
Propagation delay $I_n$ to $Z_n$	$t_{PLH}$	3.3	1.0	5.0	8.5	1.0	9.0	ns
		5.0	1.0	4.0	6.5	1.0	7.0	
Propagation delay $I_n$ to $Z_n$	$t_{PHL}$	3.3	1.0	5.0	8.0	1.0	9.0	ns
		5.0	1.0	4.0	6.5	1.0	7.0	

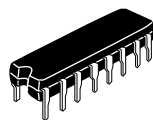
Note: 1. Voltage Range 3.3 is  $3.3\text{ V} \pm 0.3\text{ V}$   
Voltage Range 5.0 is  $5.0\text{ V} \pm 0.5\text{ V}$

### Capacitance

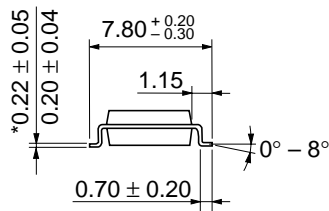
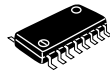
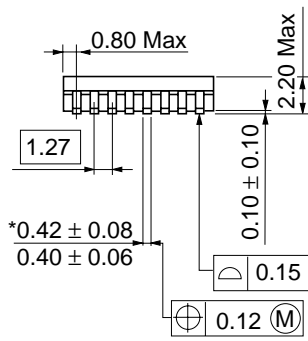
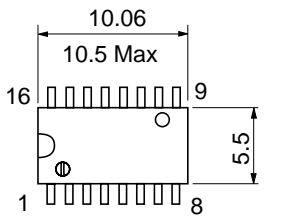
Item	Symbol	Typ	Unit	Condition
Input capacitance	$C_{IN}$	4.5	pF	$V_{CC} = 5.5\text{ V}$
Power dissipation capacitance	$C_{PD}$	50.0	pF	$V_{CC} = 5.0\text{ V}$



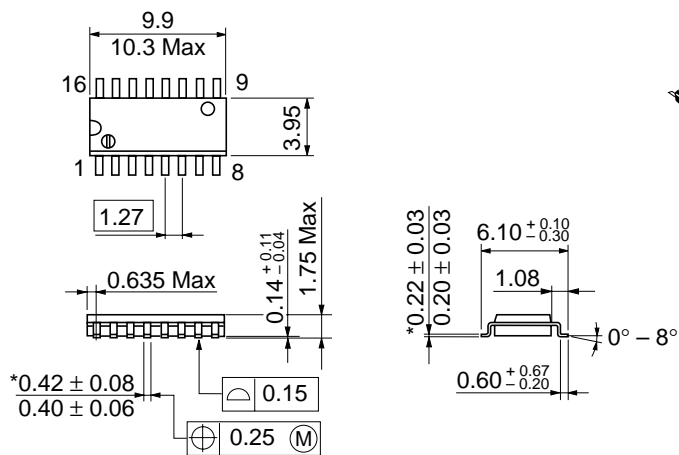
Unit: mm



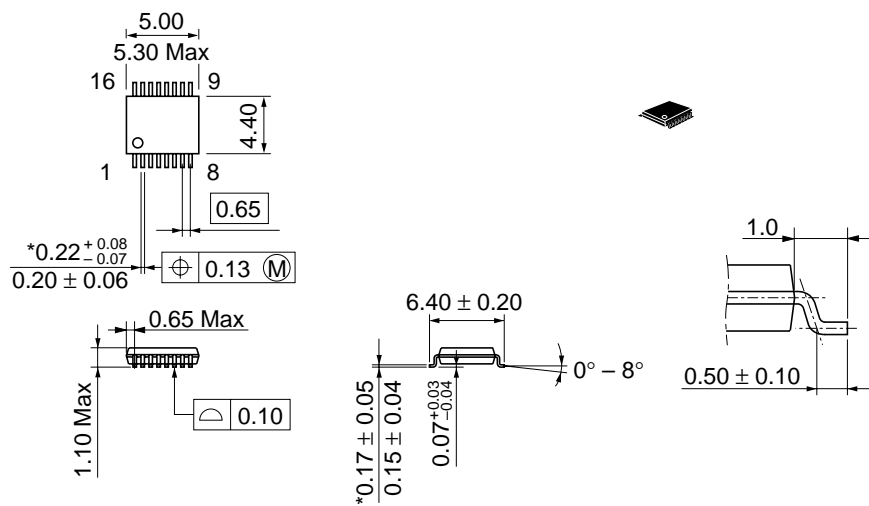
Unit: mm



Unit: mm



Unit: mm





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