
HD74AC195

4-bit Parallel-Access Shift Register

HITACHI

Description

This shift register features parallel inputs, parallel outputs, J- \bar{K} serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; Shift from Q_0 towards Q_3 .

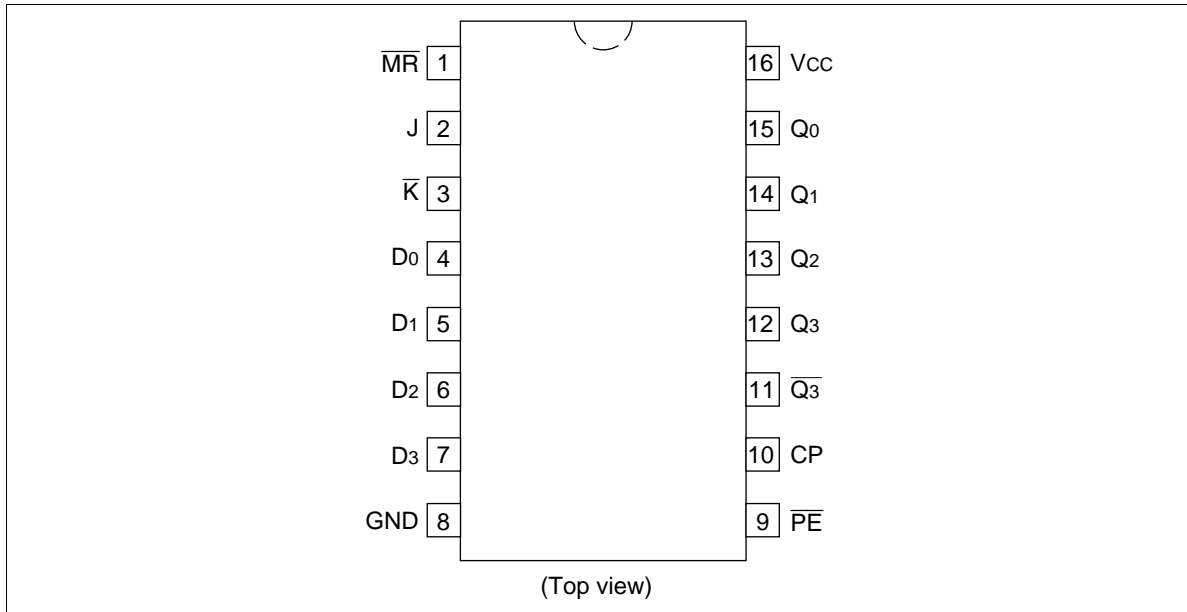
Parallel loading is accomplished by applying the four bits of data, and taking the \bar{PE} Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the CP input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the \bar{PE} input is high. Serial data for this mode is entered at the J- \bar{K} inputs. These inputs allow the first stage to perform as a J- \bar{K} or toggle flip-flop as shown in the function table.

Features

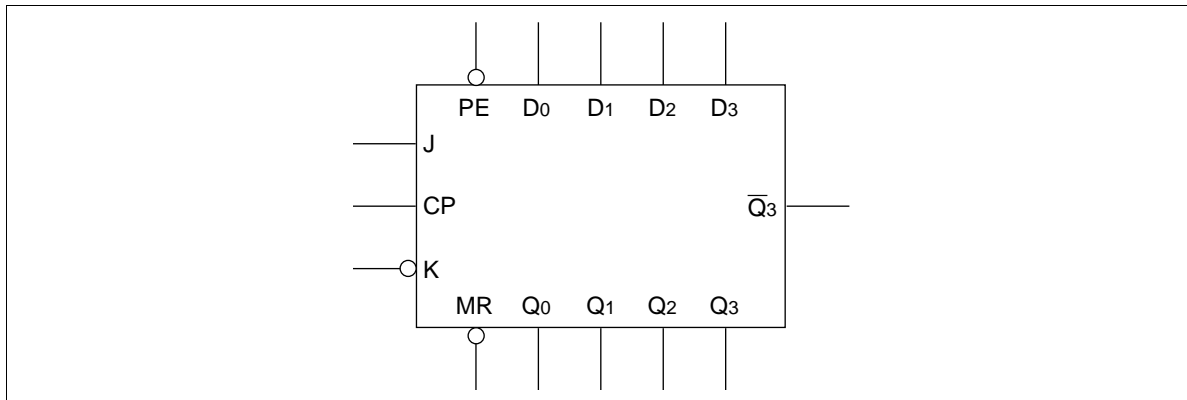
- Shift Right and Parallel Load Capability
- J- \bar{K} (D-Type) Inputs to First Stage
- Complement Output from Last Stage
- Asynchronous Master Reset
- Outputs Source/Sink 24 mA

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Pin Arrangement



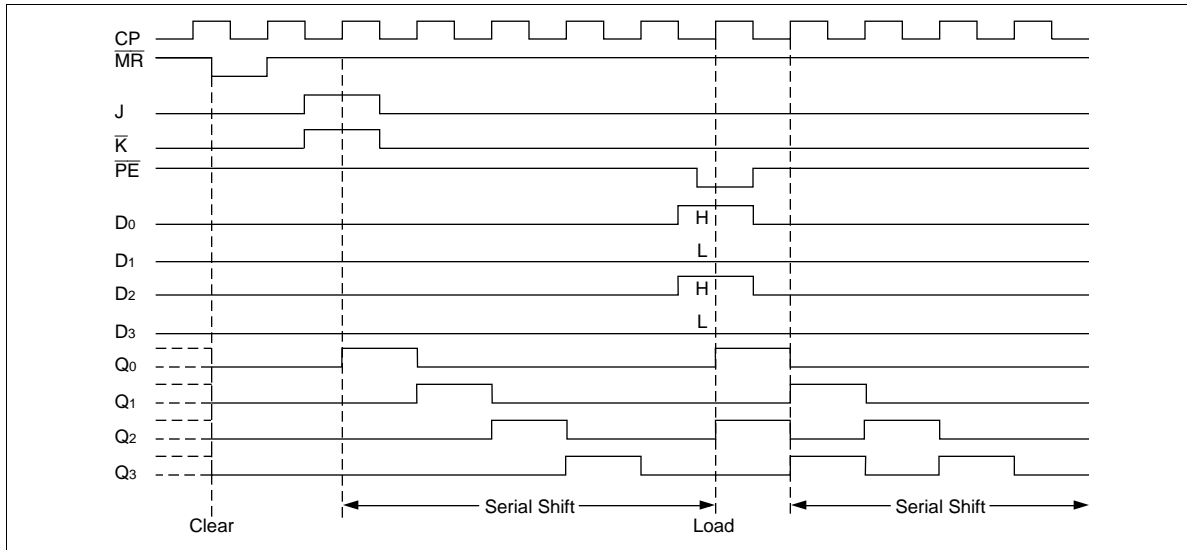
Logic Symbol



Pin Names

| | |
|---------------------------------------------------|----------------------------------------|
| CP | Clock Pulse Input (Active Rising Edge) |
| D ₀ to D ₃ | Parallel Data Inputs |
| PE | Parallel Enable Input |
| MR | Asynchronous Master Reset |
| J, K | J-K or D Type Serial Inputs |
| Q ₀ to Q ₃ , Q ₃ | Outputs |

Timing Diagram



Mode Select-Function Table

| Operating Modes | Inputs | | | | | | Outputs | | | | |
|---------------------------|--------|----|----|---|----|----------------|-----------------|----------------|----------------|----------------|-----------------|
| | MR | CP | PE | J | K̄ | D _n | Q ₀ | Q ₁ | Q ₂ | Q ₃ | Q̄ ₃ |
| Asynchronous Reset | L | X | X | X | X | X | L | L | L | L | H |
| Shift, Set First Stage | H | ⌋ | H | H | H | X | H | q ₀ | q ₁ | q ₂ | q̄ ₂ |
| Shift, Reset First Stage | H | ⌋ | H | L | L | X | L | q ₀ | q ₁ | q ₂ | q̄ ₂ |
| Shift, Toggle First Stage | H | ⌋ | H | H | L | X | q̄ ₀ | q ₀ | q ₁ | q ₂ | q̄ ₂ |
| Shift, Retain First Stage | H | ⌋ | H | L | H | X | q ₀ | q ₀ | q ₁ | q ₂ | q̄ ₂ |
| Parallel Load | H | ⌋ | L | X | X | d _n | d ₀ | d ₁ | d ₂ | d ₃ | d̄ ₃ |

H : HIGH Voltage Level

L : LOW Voltage Level

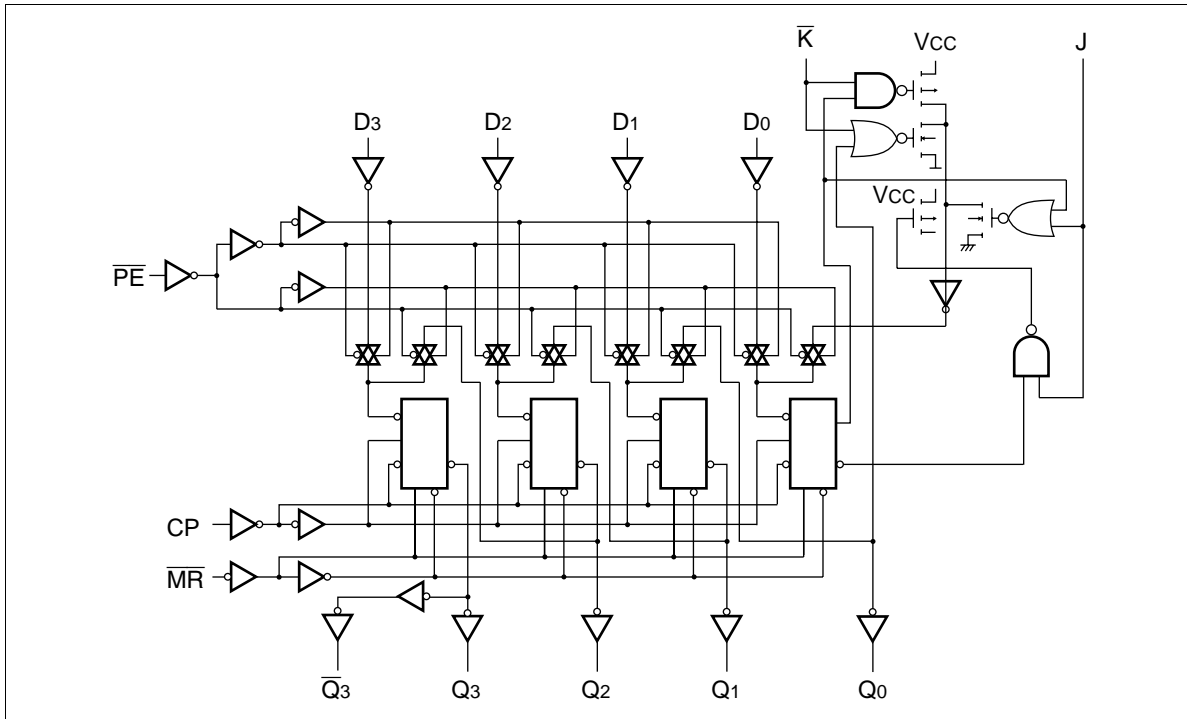
X : Immaterial

Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH transition.

⌋ : LOW-to-HIGH clock transition.

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Logic Diagram



DC Characteristics (unless otherwise specified)

| Item | Symbol | Max | Unit | Condition |
|----------------------------------|----------|-----|---------|------------------------------------------------------------------------------|
| Maximum quiescent supply current | I_{CC} | 80 | μA | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$ |
| Maximum quiescent supply current | I_{CC} | 8.0 | μA | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^\circ C$ |

AC Characteristics: HD74AC195

| Item | Symbol | V _{CC} (V)*1 | Ta = +25°C C _L = 50 pF | | | Ta = -40°C to +85°C C _L = 50 pF | | Unit |
|---------------------------------------------------------------|------------------|-----------------------|--------------------------------------|-----|------|-----------------------------------------------|------|------|
| | | | Min | Typ | Max | Min | Max | |
| Maximum clock frequency | f _{max} | 3.3 | 75 | — | — | 65 | — | MHz |
| | | 5.0 | 100 | — | — | 85 | — | |
| Propagation delay CP to Q _n or \overline{Q}_3 | t _{PLH} | 3.3 | 1.0 | 9.0 | 13.0 | 1.0 | 15.0 | ns |
| | | 5.0 | 1.0 | 5.5 | 10.0 | 1.0 | 11.5 | |
| Propagation delay CP to Q _n or \overline{Q}_2 | t _{PHL} | 3.3 | 1.0 | 9.0 | 13.0 | 1.0 | 15.0 | ns |
| | | 5.0 | 1.0 | 6.5 | 10.0 | 1.0 | 11.5 | |
| Propagation delay \overline{MR} to \overline{Q}_2 | t _{PLH} | 3.3 | 1.0 | 7.5 | 10.5 | 1.0 | 12.0 | ns |
| | | 5.0 | 1.0 | 5.5 | 8.0 | 1.0 | 9.5 | |
| Propagaion delay \overline{MR} to \overline{Q}_n | t _{PHL} | 3.3 | 1.0 | 6.0 | 9.0 | 1.0 | 10.5 | ns |
| | | 5.0 | 1.0 | 5.0 | 7.0 | 1.0 | 8.0 | |

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC195

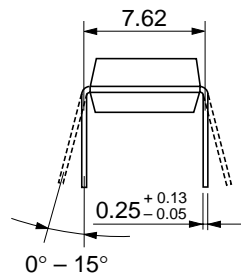
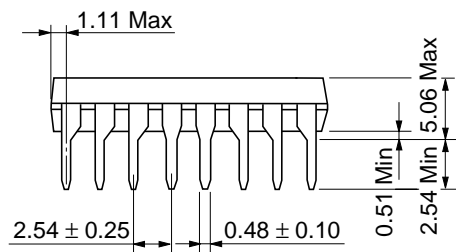
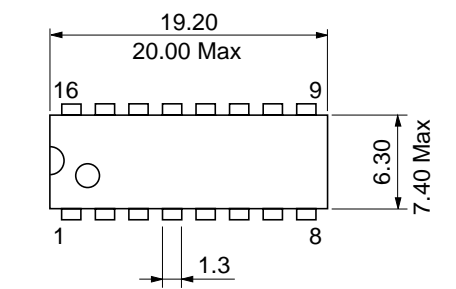
| Item | Symbol | V _{CC} (V)*1 | Ta = +25°C C _L = 50 pF | | Ta = -40°C to +85°C C _L = 50 pF | | Unit |
|------------------------------------------------------------------------|------------------|-----------------------|--------------------------------------|--------------------|--------------------------------------------------|--------------------|------|
| | | | Typ | Guaranteed Minimum | Guaranteed Minimum | Guaranteed Minimum | |
| Setup time, HIGH or LOW J, \overline{K} or \overline{D}_n to CP | t _{su} | 3.3 | 3.0 | 5.5 | 7.0 | ns | |
| | | 5.0 | 2.0 | 4.0 | 5.0 | | |
| Hold time, HIGH or LOW J, \overline{K} or \overline{D}_n to CP | t _h | 3.3 | -0.5 | 2.0 | 3.6 | ns | |
| | | 5.0 | 0.5 | 1.5 | 2.0 | | |
| Setup time, HIGH or LOW \overline{PE} to CP | t _{su} | 3.3 | 3.5 | 5.0 | 7.0 | ns | |
| | | 5.0 | 2.5 | 4.0 | 5.0 | | |
| Hold time, HIGH or LOW \overline{PE} to CP | t _h | 3.3 | -2.0 | 0.0 | 0.0 | ns | |
| | | 5.0 | -1.5 | 0.0 | 0.0 | | |
| Recovery time \overline{MR} to CP | t _{rec} | 3.3 | -1.5 | 0.5 | 0.5 | ns | |
| | | 5.0 | -1.0 | 0.5 | 0.5 | | |
| Pulse width | t _w | 3.3 | -3.0 | 5.5 | 7.0 | ns | |
| | | 5.0 | -3.0 | 4.5 | 5.0 | | |

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

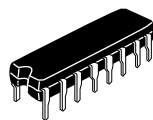
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Capacitance

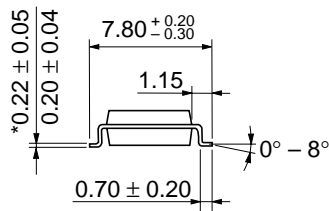
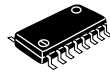
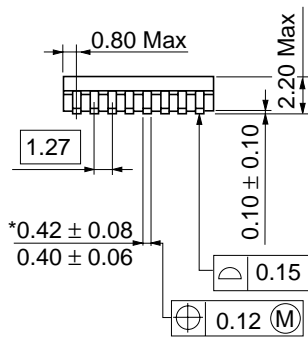
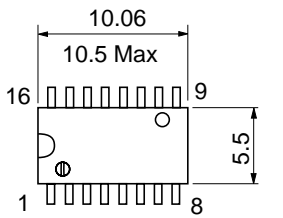
| Item | Symbol | Typ | Unit | Condition |
|-------------------------------|----------|-----|------|--------------------------|
| Input capacitance | C_{IN} | 4.5 | pF | $V_{CC} = 5.5 \text{ V}$ |
| Power dissipation capacitance | C_{PD} | 125 | pF | $V_{CC} = 5.0 \text{ V}$ |



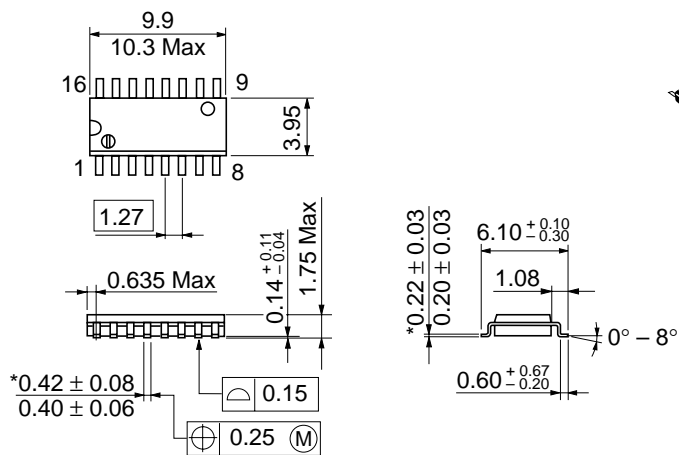
Unit: mm



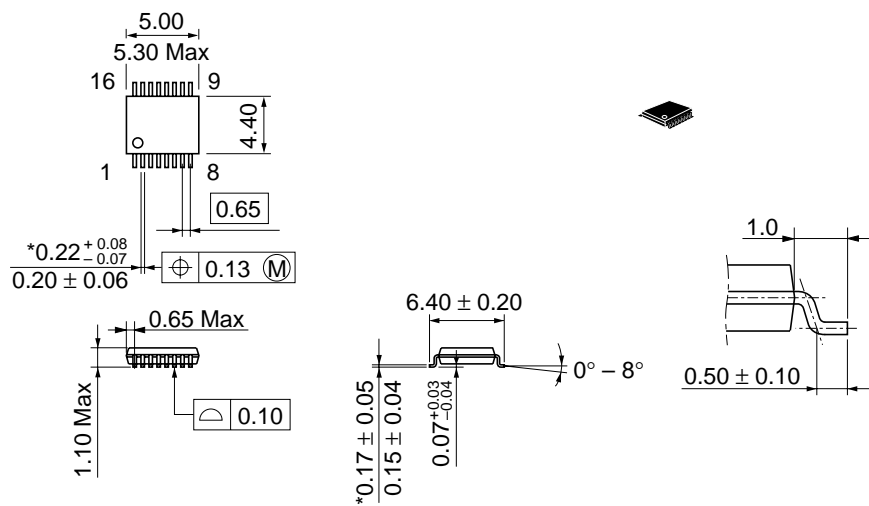
Unit: mm



Unit: mm



Unit: mm



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