

# HD74ALVCH16500

18-bit Universal Bus Transceivers with 3-state Outputs

# HITACHI

ADE-205-167A (Z)

2nd. Edition

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## Description

Data flow in each direction is controlled by output enable ( $\text{OEAB}$  and  $\overline{\text{OEBA}}$ ), latch enable ( $\text{LEAB}$  and  $\text{LEBA}$ ), and clock ( $\overline{\text{CLKAB}}$  and  $\overline{\text{CLKBA}}$ ) inputs. For A to B data flow, the device operates in the transparent mode when  $\text{LEAB}$  is high. When  $\text{LEAB}$  is low, the A data is latched if  $\overline{\text{CLKAB}}$  is held at a high or low logic level. If  $\text{LEAB}$  is low, the A bus data is stored in the latch flip flop on the high to low transition of  $\overline{\text{CLKAB}}$ . Output enable  $\text{OEAB}$  is active high. When  $\text{OEAB}$  is high, the B port outputs are active. When  $\text{OEAB}$  is low, the B port outputs are in the high impedance state. Data flow for B to A is similar to that of A to B but uses  $\overline{\text{OEBA}}$ ,  $\text{LEBA}$ , and  $\overline{\text{CLKBA}}$ . The output enables are complementary ( $\text{OEAB}$  is active high, and  $\overline{\text{OEBA}}$  is active low). Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## Features

- $V_{CC} = 2.3 \text{ V}$  to  $3.6 \text{ V}$
- Typical  $V_{OL}$  ground bounce  $< 0.8 \text{ V}$  ( $@V_{CC} = 3.3 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.0 \text{ V}$  ( $@V_{CC} = 3.3 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- High output current  $\pm 24 \text{ mA}$  ( $@V_{CC} = 3.0 \text{ V}$ )
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors

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## HD74ALVCH16500

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**Function Table** <sup>\*3</sup>

Inputs				Output B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B <sub>0</sub> <sup>'1</sup>
H	L	L	X	B <sub>0</sub> <sup>'2</sup>

H : High level

L : Low level

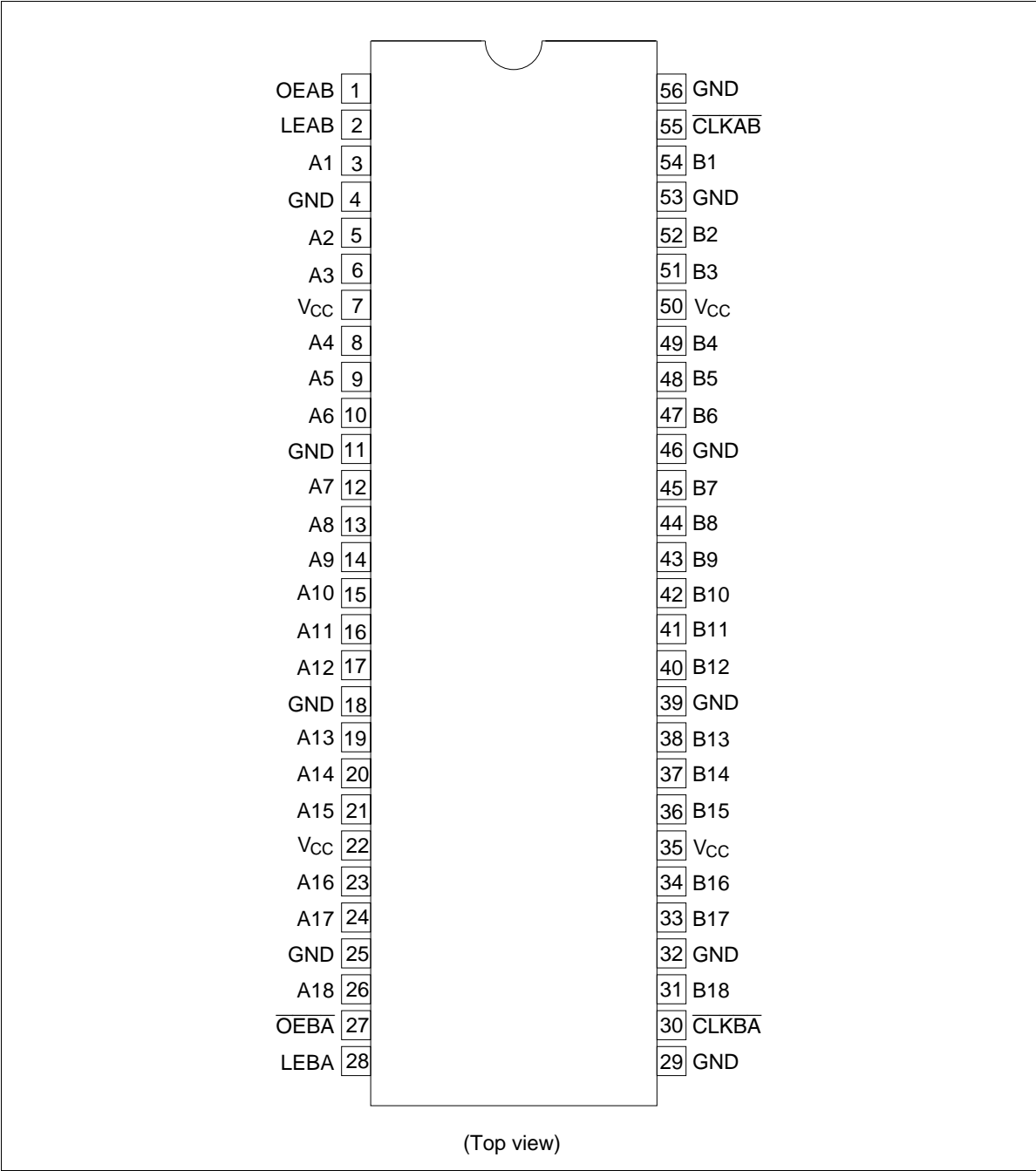
X : Immaterial

Z : High impedance

↓ : High to low transition

- Notes:
1. Output level before the indicated steady state input conditions were established.
  2. Output level before the indicated steady state input conditions were established, provided that  $\overline{\text{CLKAB}}$  was low before LEAB went low.
  3. A to B data flow is show; B to A flow is similar but uses  $\overline{\text{OEBA}}$ , LEBA, and  $\overline{\text{CLKBA}}$ .

Pin Arrangement



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### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	−0.5 to 4.6	V	
Input voltage <sup>*1,2</sup>	$V_I$	−0.5 to 4.6	V	Except I/O ports
		−0.5 to $V_{CC} + 0.5$		I/O ports
Output voltage <sup>*1,2</sup>	$V_O$	−0.5 to $V_{CC} + 0.5$	V	
Input clamp current	$I_{IK}$	−50	mA	
Output clamp current	$I_{OK}$	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	±50	mA	$V_O = 0$ to $V_{CC}$
		±100		
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	1	W	TSSOP
Storage temperature	$T_{stg}$	−65 to 150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

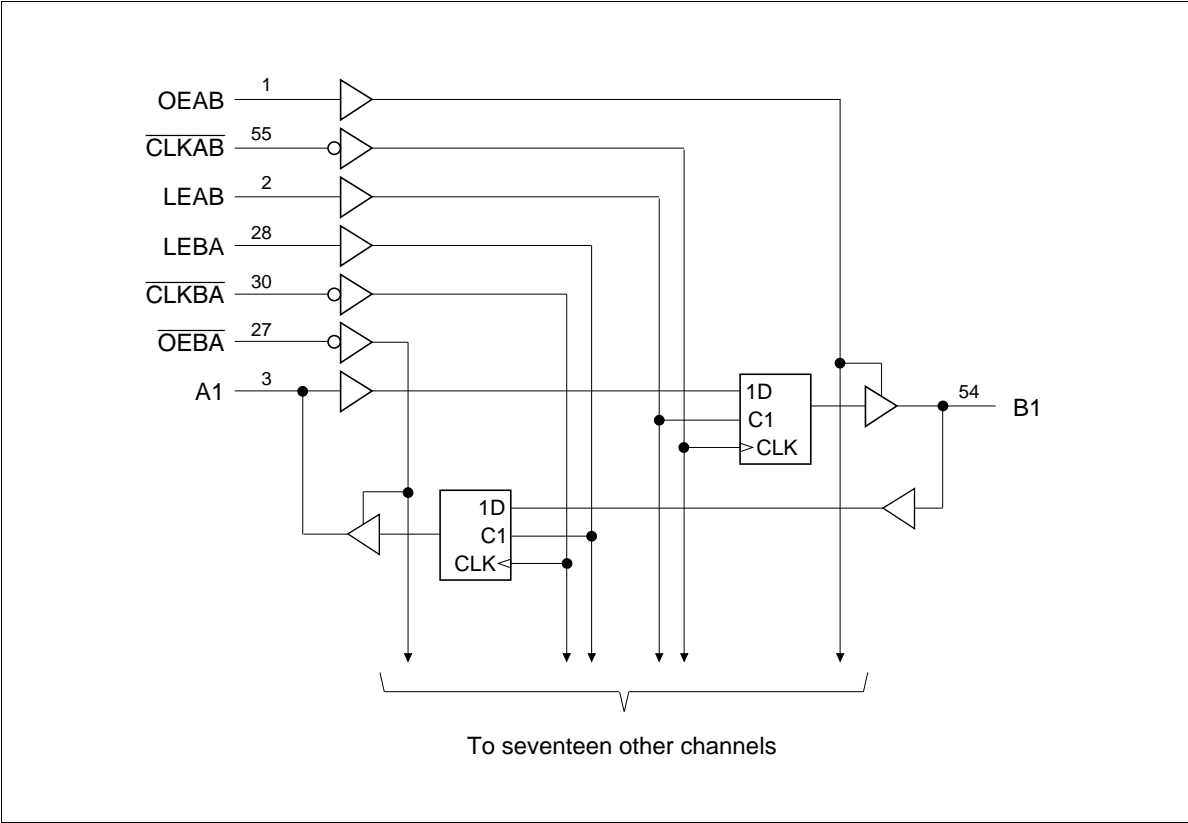
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

### Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	$V_{CC}$	2.3	3.6	V	
Input voltage	$V_I$	0	$V_{CC}$	V	
Output voltage	$V_O$	0	$V_{CC}$	V	
High level output current	$I_{OH}$	—	−12	mA	$V_{CC} = 2.3\text{ V}$
		—	−12		$V_{CC} = 2.7\text{ V}$
		—	−24		$V_{CC} = 3.0\text{ V}$
Low level output current	$I_{OL}$	—	12	mA	$V_{CC} = 2.3\text{ V}$
		—	12		$V_{CC} = 2.7\text{ V}$
		—	24		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	$T_a$	−40	85	$^\circ\text{C}$	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



## HD74ALVCH16500

### Electrical Characteristics (Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V) <sup>*1</sup>	Min	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V <sub>IL</sub>	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA
		2.3	2.0	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 1.7 V
		2.3	1.7	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 1.7 V
		2.7	2.2	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V
		3.0	2.4	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V
		3.0	2.0	—		I <sub>OH</sub> = -24 mA, V <sub>IH</sub> = 2.0 V
	V <sub>OL</sub>	Min to Max	—	0.2		I <sub>OL</sub> = 100 μA
		2.3	—	0.4		I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V
		2.3	—	0.7		I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.7 V
		2.7	—	0.4		I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V
		3.0	—	0.55		I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V
Input current	I <sub>IN</sub>	3.6	—	±5	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	I <sub>IN (hold)</sub>	2.3	45	—		V <sub>IN</sub> = 0.7 V
		2.3	-45	—		V <sub>IN</sub> = 1.7 V
		3.0	75	—		V <sub>IN</sub> = 0.8 V
		3.0	-75	—		V <sub>IN</sub> = 2.0 V
		3.6	—	±500		V <sub>IN</sub> = 0 to 3.6 V
Off state output current <sup>*2</sup>	I <sub>OZ</sub>	3.6	—	±10	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND
Quiescent supply current	I <sub>CC</sub>	3.6	—	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	3.0 to 3.6	—	750	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6) V, other inputs at V <sub>CC</sub> or GND

Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

2. For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

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### Switching Characteristics (Ta = -40 to 85°C)

Item	Symbol	V <sub>cc</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency f <sub>max</sub>		2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t <sub>PLH</sub>	2.5±0.2	1.0	—	5.1	ns	A or B	B or A
	t <sub>PHL</sub>	2.7	—	—	4.7			
		3.3±0.3	1.0	—	3.9			
		2.5±0.2	1.0	—	5.9	LEAB or LEBA	A or B	
		2.7	—	—	5.5			
		3.3±0.3	1.0	—	4.7			
		2.5±0.2	1.0	—	6.1	$\overline{\text{CLKAB}}$ or $\overline{\text{CLKBA}}$	A or B	
	2.7	—	—	6.6				
	3.3±0.3	1.1	—	5.5				
Output enable time	t <sub>ZH</sub>	2.5±0.2	1.0	—	5.7	ns	$\overline{\text{OEAB}}$	B
	t <sub>ZL</sub>	2.7	—	—	5.4			
		3.3±0.3	1.0	—	4.6			
		2.5±0.2	1.0	—	6.1	$\overline{\text{OEBA}}$	A	
	2.7	—	—	6.2				
	3.3±0.3	1.0	—	5.2				
Output disable time	t <sub>HZ</sub>	2.5±0.2	1.7	—	6.2	ns	$\overline{\text{OEAB}}$	B
	t <sub>LZ</sub>	2.7	—	—	5.7			
		3.3±0.3	1.5	—	5.0			
		2.5±0.2	1.0	—	5.4	$\overline{\text{OEBA}}$	A	
	2.7	—	—	4.6				
	3.3±0.3	1.0	—	4.3				
Input capacitance	C <sub>IN</sub>	3.3	—	4.0	—	pF	Control inputs	
Output capacitance	C <sub>IN/O</sub>	3.3	—	8.0	—	pF	A or B ports	

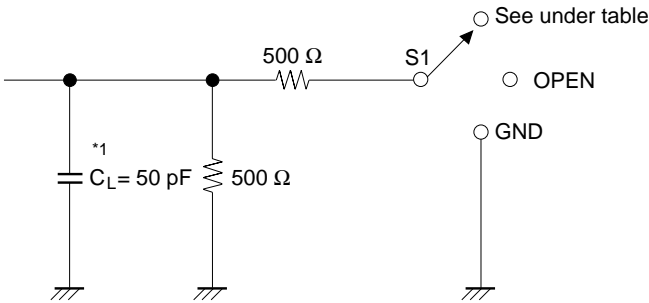
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### Switching Characteristics (Ta = -40 to 85°C) (Cont)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t <sub>su</sub>	2.5±0.2	1.7	—	—	ns	Data before CLK↓
		2.7	1.4	—	—		
		3.3±0.3	1.3	—	—		
		2.5±0.2	1.1	—	—		Data before LE↓
		2.7	1.0	—	—		CLK "H"
		3.3±0.3	1.0	—	—		
		2.5±0.2	1.9	—	—		Data before LE↓
		2.7	1.6	—	—		CLK "L"
		3.3±0.3	1.4	—	—		
Hold time	t <sub>h</sub>	2.5±0.2	1.7	—	—	ns	Data after CLK↓
		2.7	1.6	—	—		
		3.3±0.3	1.3	—	—		
		2.5±0.2	2.0	—	—		Data after LE↓
		2.7	1.8	—	—		CLK "H"
		3.3±0.3	1.5	—	—		
		2.5±0.2	1.6	—	—		Data after LE↓
		2.7	1.5	—	—		CLK "L"
		3.3±0.3	1.2	—	—		
Pulse width	t <sub>w</sub>	2.5±0.2	3.3	—	—	ns	LE "H"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		
		2.5±0.2	3.3	—	—		CLK "H" or "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		



• Test Circuit



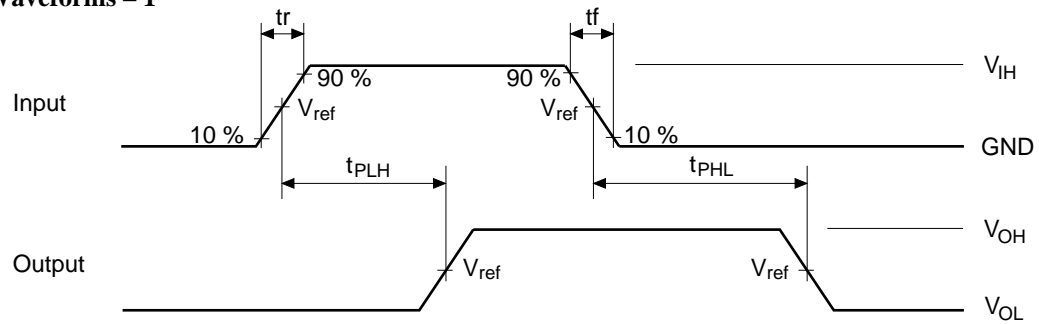
Load Circuit for Outputs

Symbol	$V_{CC}=2.5\pm0.2\text{V}$	$V_{CC}=2.7\text{V}, 3.3\pm0.3\text{V}$
$t_{PLH}/t_{PHL}$	OPEN	OPEN
$t_{su}/t_h/t_w$	OPEN	OPEN
$t_{ZH}/t_{HZ}$	GND	GND
$t_{ZL}/t_{LZ}$	4.6 V	6.0 V

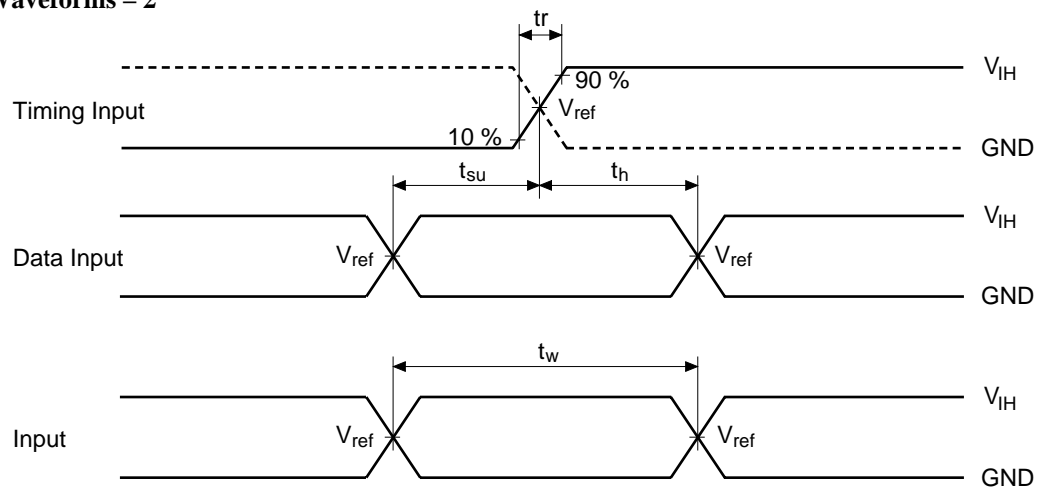
Note: 1.  $C_L$  includes probe and jig capacitance.

## HD74ALVCH16500

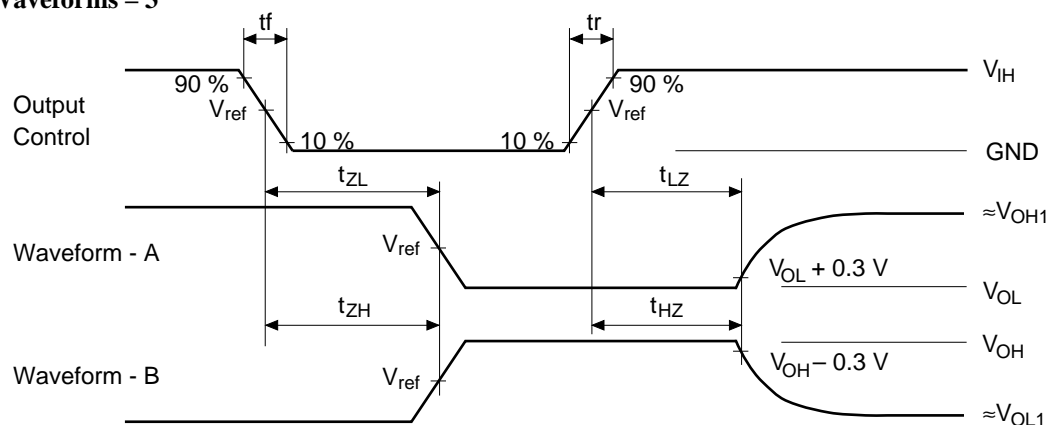
### • Waveforms – 1



### • Waveforms – 2



- **Waveforms – 3**



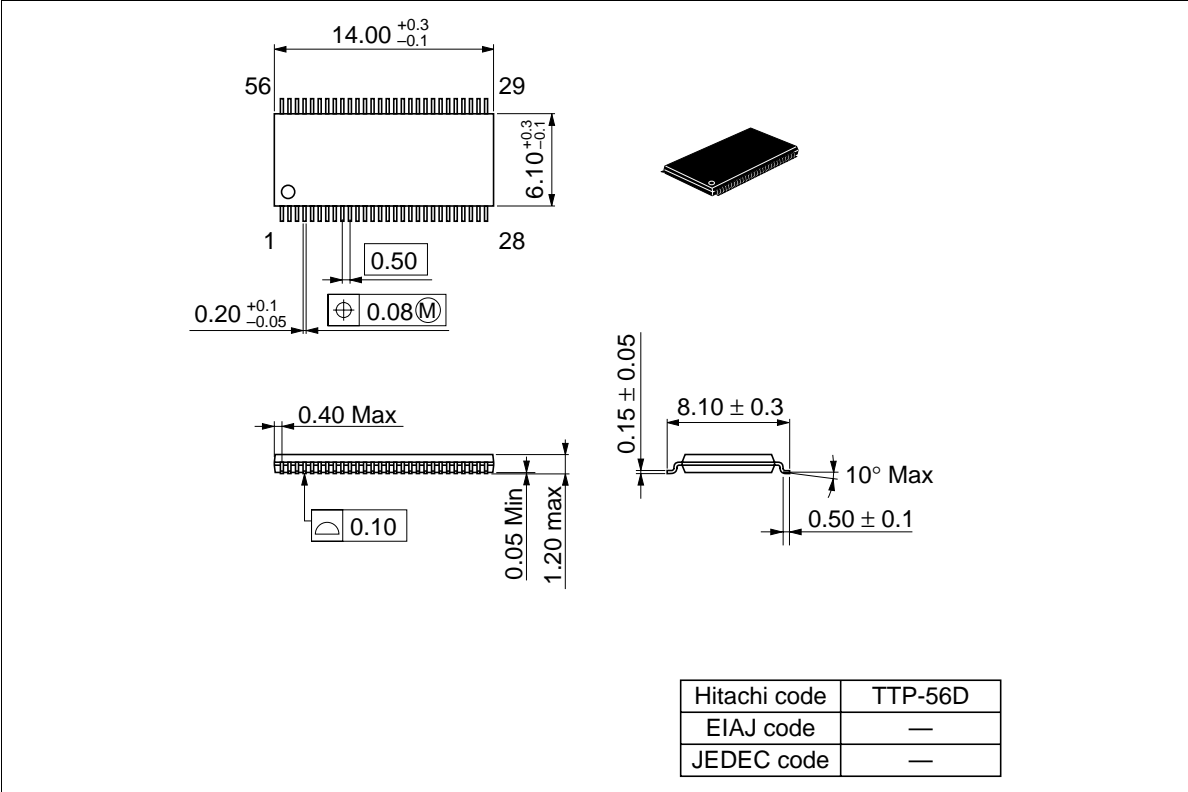
TEST	V <sub>CC</sub> =2.5±0.2V	V <sub>CC</sub> =2.7V, 3.3±0.3V
V <sub>IH</sub>	2.3 V	2.7 V
V <sub>ref</sub>	1.2 V	1.5 V
V <sub>OH1</sub>	2.3 V	3.0 V
V <sub>OL1</sub>	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics:  
 $\text{PRR} \leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
  4. The output are measured one at a time with one transition per measurement.

**HD74ALVCH16500**

**Package Dimensions**

**Unit : mm**



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