
HD74BC564A

Octal D Type Flip Flops With 3 State Outputs

HITACHI

ADE-205-041 (Z)

Rev. 0

June 1993

Description

The HD74BC564A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC, when the frequency is 10 MHZ. The device has eight edge trigger D type flip flops with three state outputs in a 20 pin package. Data at the D inputs meeting set up requirements, are transferred to the $\bar{Q}$ outputs on positive going transitions of the clock input. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- Input/Output are at high impedance state when power supply is off.
- Built in input pull up circuit can make input pins be open, when not used.
- TTL level input
- Wide operating temperature range
 $T_a = -40$ to $+85^{\circ}\text{C}$

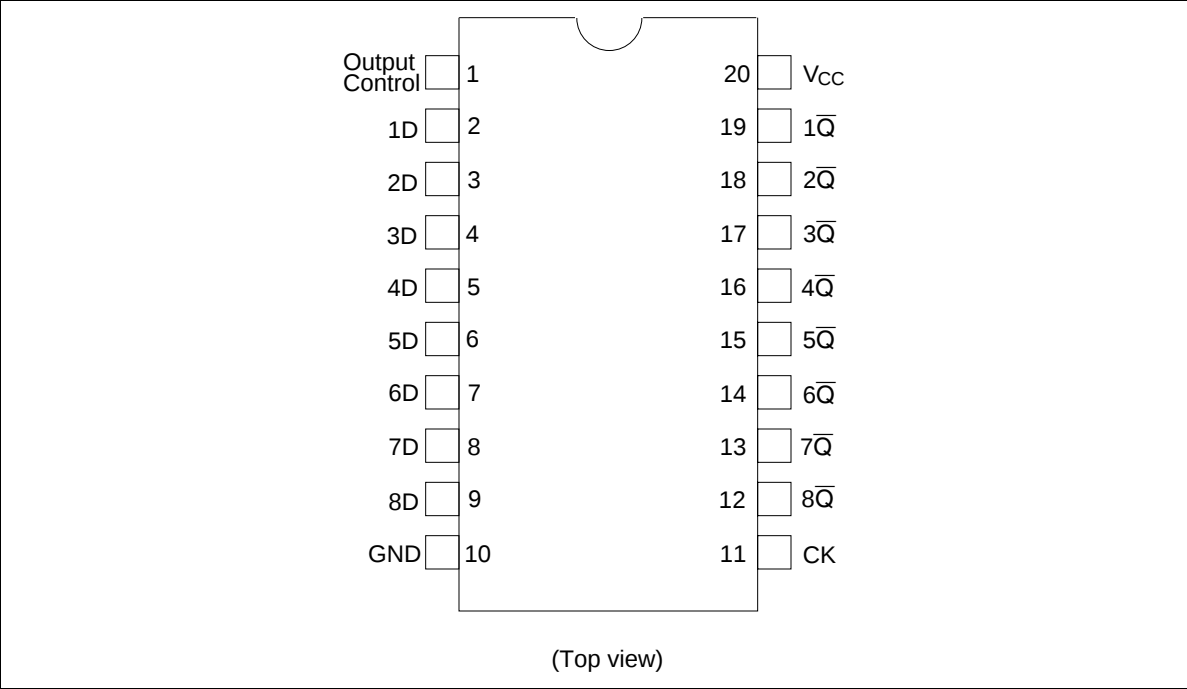
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Function Table

Inputs			
Output Control	CK	D	Output $\overline{Q}$
L		H	L
L		L	H
L	L	X	Q_0
H	X	X	Z

H : High level
L : Low level
X : Immaterial
Z : High impedance
 : Low to high transition
 Q_0 : Level of $\overline{Q}$ before the indicated steady state input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 to +7.0	V
Input diode current	I_{IK}	±30	mA
Input voltage	V_{IN}	−0.5 to +7.5	V
Output voltage	V_{OUT}	−0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	−0.5 to +5.5	V
Storage temperature	Tstg	−65 to +150	°C

Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

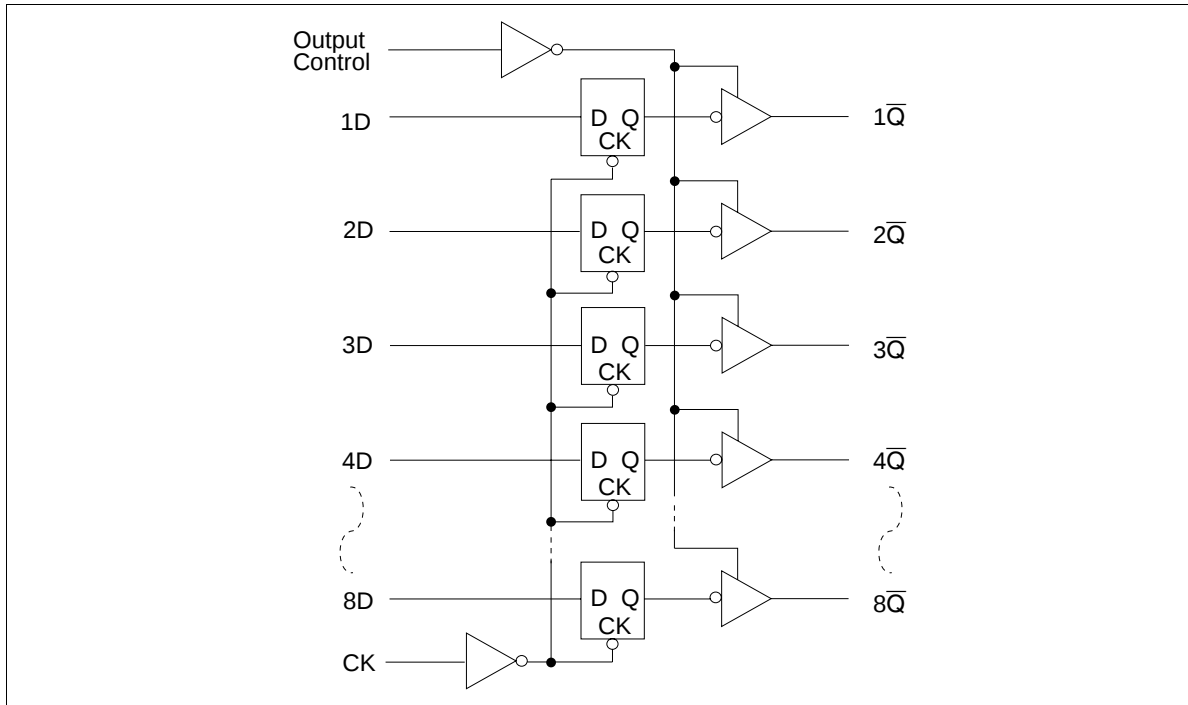
Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IN}	0	—	V_{CC}	V
Output voltage	V_{OUT}	0	—	V_{CC}	V
Operating temperature	Topr	−40	—	85	°C
Input rise/fall time*1	t_r, t_f	0	—	8	ns/V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

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Logic Diagram



Electrical Characteristics (Ta = -40°C to +85°C)

Item	Symbol	VCC(V)	Min	Max	Unit	Test Conditions
Input voltage	V _{IH}		2.0	—	V	
	V _{IL}		—	0.8	V	
Output voltage	V _{OH}	4.5	2.4	—	V	I _{OH} = -3 mA
		4.5	2.0	—	V	I _{OH} = -15 mA
	V _{OL}	4.5	—	0.4	V	I _{OL} = 24 mA
		4.5	—	0.5	V	I _{OL} = 48 mA
Input diode voltage	V _{IK}	4.5	—	-1.2	V	I _{IN} = -18 mA
Input current	I _I	5.5	—	-250	μA	V _{IN} = 0 V
		5.5	—	1.0	μA	V _{IN} = 5.5 V
		5.5	—	100	μA	V _{IN} = 7.0 V
Short circuit output current*1	I _{OS}	5.5	-100	-225	mA	V _{IN} = 0 or 5.5 V
Off state output current	I _{OZH}	5.5	—	50	μA	V _O = 2.7 V
	I _{OZL}	5.5	—	-50	μA	V _O = 0.5 V
Supply current	I _{CCL}	5.5	—	29.5	mA	V _{IN} = 0 or 5.5 V All outputs is "L"
	I _{CCH}	5.5	—	2.5	mA	V _{IN} = 0 or 5.5 V All outputs is "H"
	I _{CCZ}	5.5	—	2.5	mA	V _{IN} = 0 or 5.5 V All outputs is "Z"
	I _{CCT} *2	5.5	—	1.5	mA	V _{IN} = 3.4 or 0.5 V

Notes : 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

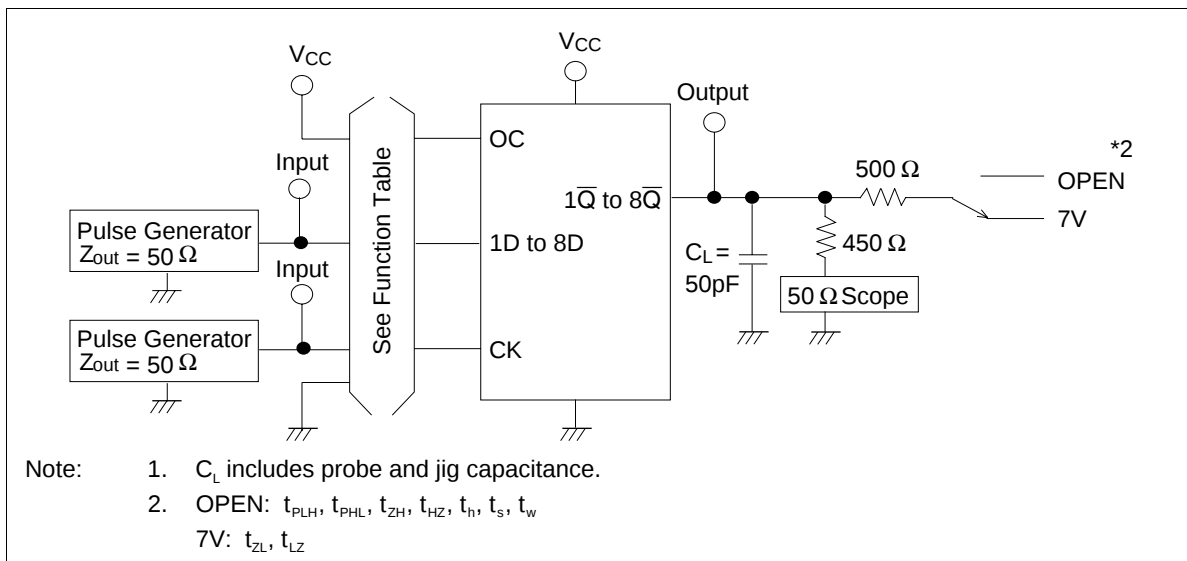
2. When input by the TTL level, it shows I_{CC} increase at per one input pin.

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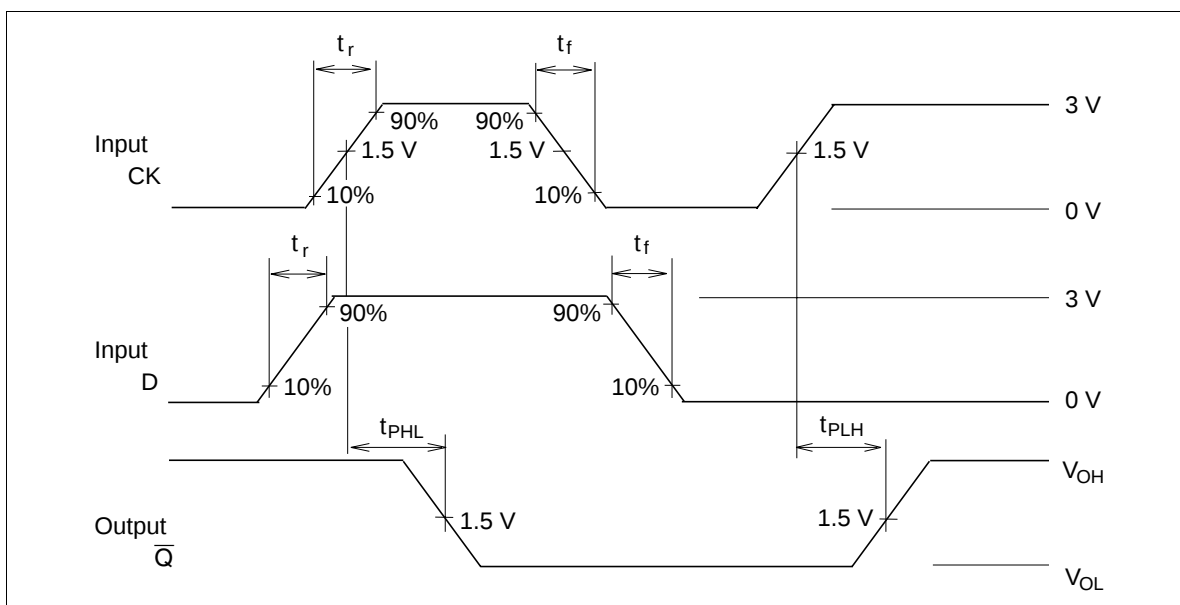
Switching Test Method ($C_L = 50 \text{ pF}$)

Item	Symbol	Ta = 25°C V _{CC} = 5.0 V		Ta = -40 to 85°C V _{CC} = 5.0V ±10%		Unit	Test Conditions
		Min	Max	Min	Max		
Propagation delay time	CK → $\overline{Q}$ t_{PLH}	3.0	8.0	3.0	10.0	ns	See under figure
	t_{PHL}	3.0	8.0	3.0	10.0		
Output enable time	t_{ZH}	3.0	9.0	3.0	11.0	ns	
	t_{ZL}	3.0	9.0	3.0	11.0		
Output disable time	t_{HZ}	3.0	8.0	3.0	10.0	ns	
	t_{LZ}	3.0	8.0	3.0	10.0		
Setup time	$t_s(H)$	2.0	—	2.0	—	ns	
	$t_s(L)$	2.0	—	2.0	—		
Hold time	$t_h(H)$	2.0	—	2.0	—	ns	
	$t_h(L)$	2.0	—	2.0	—		
Pulse width	$t_w(H)$	6.0	—	6.0	—	ns	
	$t_w(L)$	6.0	—	6.0	—		
Input capacitance	C _{IN}	3.0(Typ)		—		pF	V _{IN} = V _{CC} or GND
Output capacitance	C _O	15.0(Typ)		—		pF	V _O = V _{CC} or GND

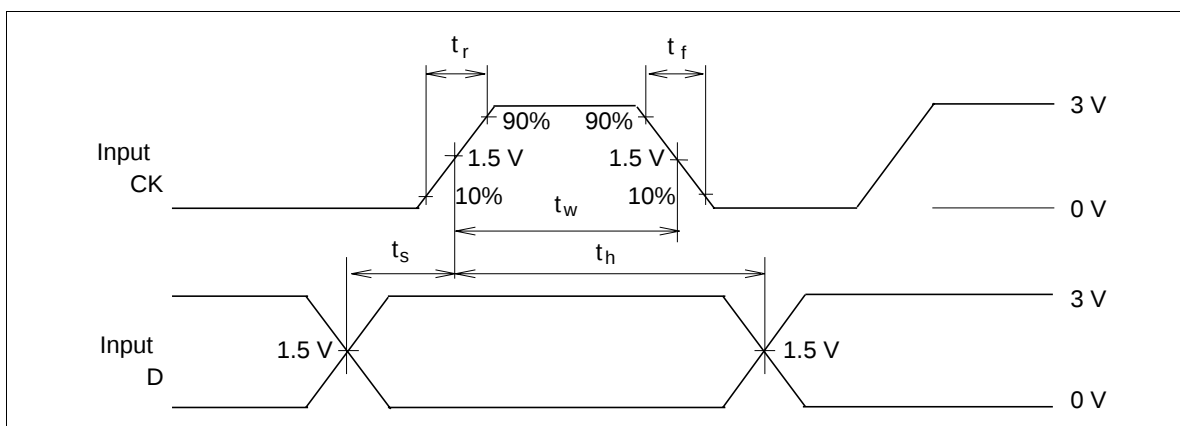
Test Circuit



Waveforms-1

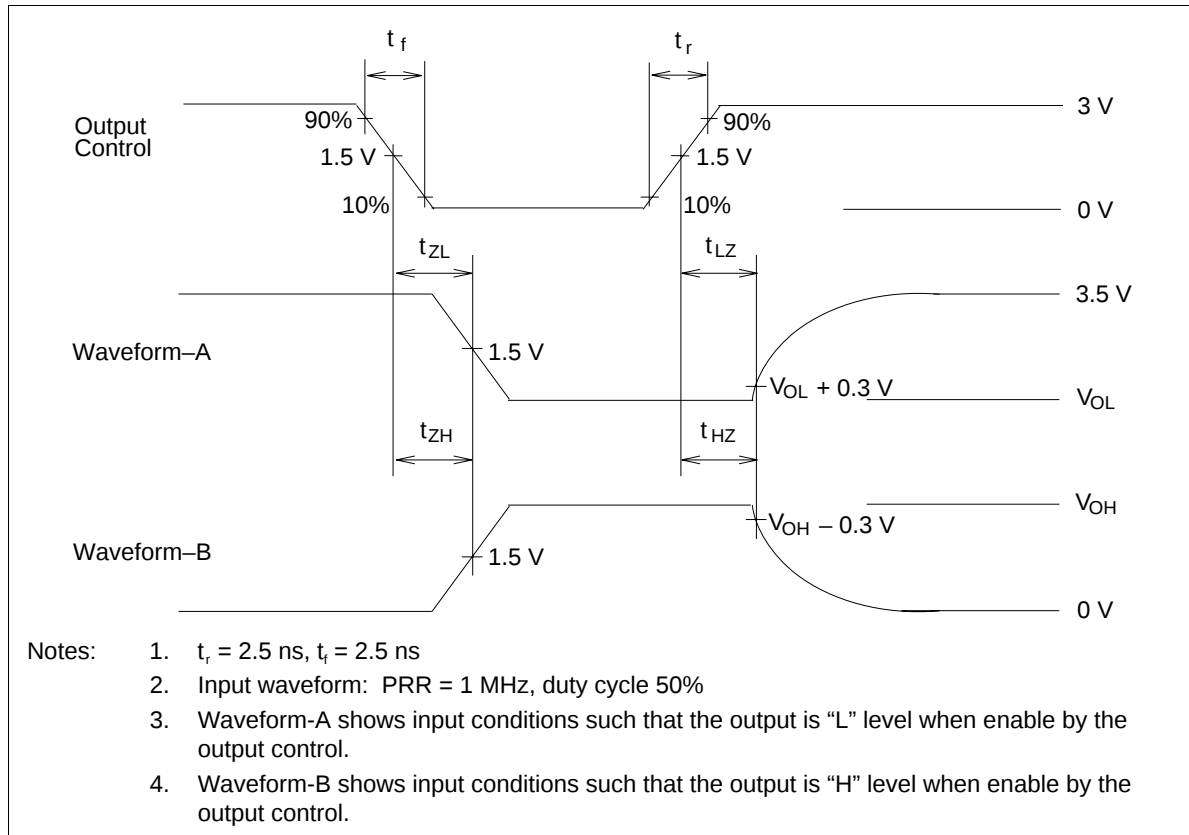


Waveforms-2



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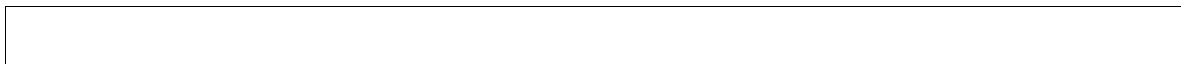
Waveforms-3



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Package Dimensions

Unit: mm



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