HD74CDC2509B

3.3-V Phase-lock Loop Clock Driver

HITACHI

ADE-205-218F (Z)
7th. Edition
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Description

The HD74CDC2509B is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The HD74CDC2509B operates at 3.3 V V_{CC} and is designed to drive up to five clock loads per output.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of the input clock. Output signal duty cycles are adjusted to 50 percent independent of the duty cycle at the input clock. Each bank of outputs can be enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the HD74CDC2509B does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, HD74CDC2509B requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.

Features

- Meets “PC SDRAM registered DIMM design support document, Rev. 1.2”
- Phase-lock loop clock distribution for synchronous DRAM applications
- External feedback (FBIN) pin is used to synchronize the outputs to the clock input
- No external RC network required
- Support spread spectrum clock (SSC) synthesizers

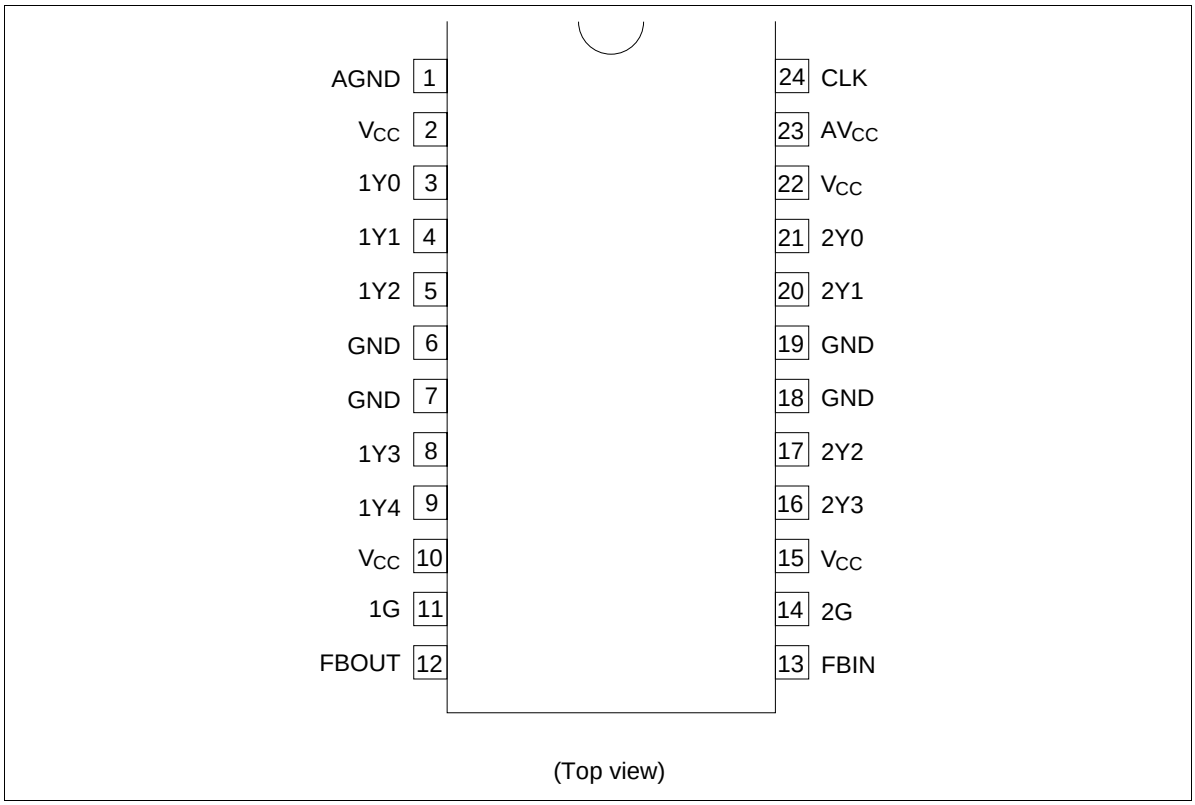
Note: Only by a change of a suffix (A to B) for standardization, there isn’t any change of the product.

Function Table

Inputs			Outputs		
1G	**2G**	**CLK**	**1Y (0:4)**	**2Y (0:3)**	**FBOUT**
X	X	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

H : High level
L : Low level
X : Immaterial

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 4.6	V	
Input voltage [*1]	V_I	–0.5 to 6.5	V	
Output voltage [*1, 2]	V_O	–0.5 to V_{CC} +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{CC}
Supply current	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) [*3]	P_T	0.7	W	
Storage temperature	T_{stg}	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

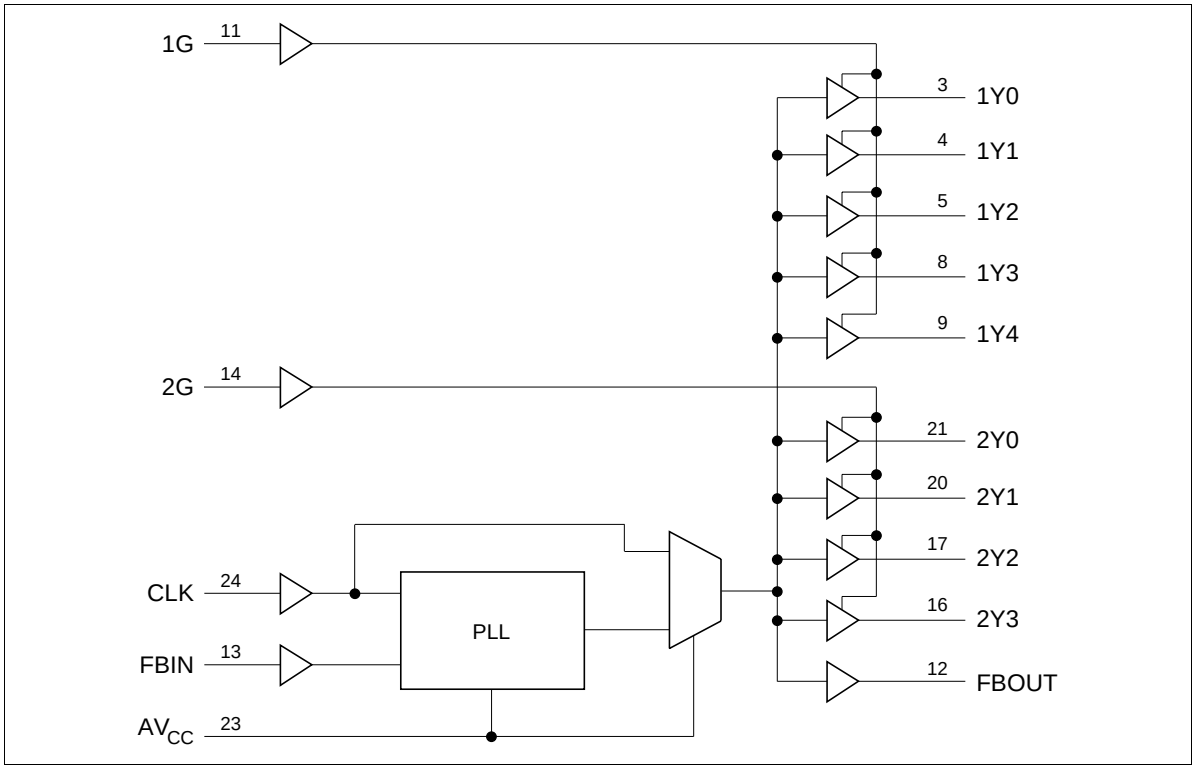
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	3.0	—	3.6	V	
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8		
	V_I	0	—	V_{CC}		
Output current	I_{OH}	—	—	–12	mA	
	I_{OL}	—	—	12		
Operating temperature	T_a	0	—	85	°C	

Note: Unused inputs must be held high or low to prevent them from floating.

Logic Diagram



Pin Function

Pin name	No.	Type	Description
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the HD74CDC2509B clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	I	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4)are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.
2G	14	I	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3)are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
1Y(0:4)	3, 4, 5, 8, 9	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic low state by deasserting the 1G control input.
2Y(0:3)	16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic low state by deasserting the 2G control input.
AV_{CC}	23	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2, 10, 15, 22	Power	Power supply
GND	6, 7, 18,19	Ground	Ground

Electrical Characteristics

Item	Symbol	Min	Typ [*1]	Max	Unit	Test Conditions
Input clamp voltage	V_{IK}	—	—	–1.2	V	V_{CC} = 3 V, I_I = –18 mA
Output voltage	V_{OH}	V_{CC}–0.2	—	—	V	V_{CC} = Min to Max, I_{OH} = –100 µA
		2.1	—	—		V_{CC} = 3 V, I_{OH} = –12 mA
		2.4	—	—		V_{CC} = 3 V, I_{OH} = –6 mA
	V_{OL}	—	—	0.2		V_{CC} = Min to Max, I_{OL} = 100 µA
		—	—	0.8		V_{CC} = 3 V, I_{OL} = 12 mA
		—	—	0.55		V_{CC} = 3 V, I_{OL} = 6 mA
Input current	I_{IN}	—	—	±5	µA	V_{CC} = 3.6 V, V_{IN} = V_{CC} or GND
Quiescent supply current	I_{CC}	—	—	10	µA	AV_{CC} = GND, V_{CC} = 3.6 V, V_I = V_{CC} or GND, I_O = 0
	ΔI_{CC}	—	—	500	µA	AV_{CC} = GND, V_{CC} = 3.3 to 3.6 V One input at V_{CC}–0.6 V, Other inputs at V_{CC} or GND
Input capacitance	C_{IN}	—	4	—	pF	V_{CC} = 3.3 V, V_I = V_{CC} or GND
Output capacitance	C_O	—	6	—	pF	V_{CC} = 3.3 V, V_O = V_{CC} or GND

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Switching Characteristics (C_L = 30 pF, Ta = 0 to 85°C)

Item	Symbol	V_{CC} = 3.3 V±0.3 V			Unit	From (Input)	To (Output)
		Min	Typ	Max			
Phase error time	t_{pe}	–150	—	150	ps	66 MHz < CLKIN↑ ≤ 100 MHz	FBIN↑
Between output pins skew [*1]	$t_{sk\ (O)}$	—	—	200	ps	Any Y or FBOUT	Any Y or FBOUT
Cycle to cycle jitter		–100	—	100	ps	F (clkin = 100 MHz)	Any Y or FBOUT
Duty cycle		45	—	55	%	F (clkin = 66 to 100 MHz)	Any Y or FBOUT
Output rise / fall time	t_{TLH}	5.0	—	1.0	volts/ns		Any Y or FBOUT
	t_{THL}	5.0	—	1.0			Any Y or FBOUT
Analog power supply rejection (DC to 10 MHz)	Vapsr [*2]	100	—	—	mV_{P-P}		AV_{CC}

Notes: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

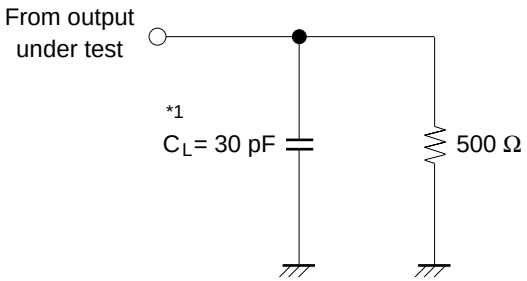
1. The $t_{sk(O)}$ specification is only valid for equal loading of all outputs.
2. This parameter is characterized but not tested.

Timing requirements

Item	Symbol	Min	Max	Unit	Test Conditions
Input clock frequency	f_{clock}	50	125	MHz	
Input clock duty cycle		40	60	%	
Stabilization time [*1]		—	1	ms	After power up

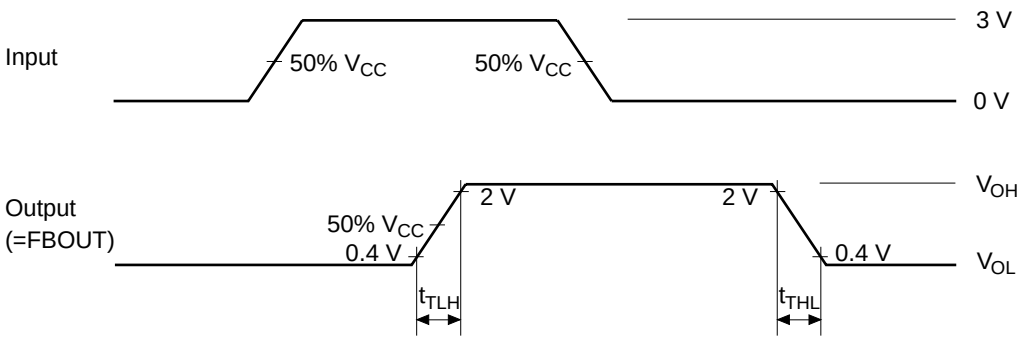
Note: 1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

Test Circuit



Note: 1. C_L includes probe and jig capacitance.

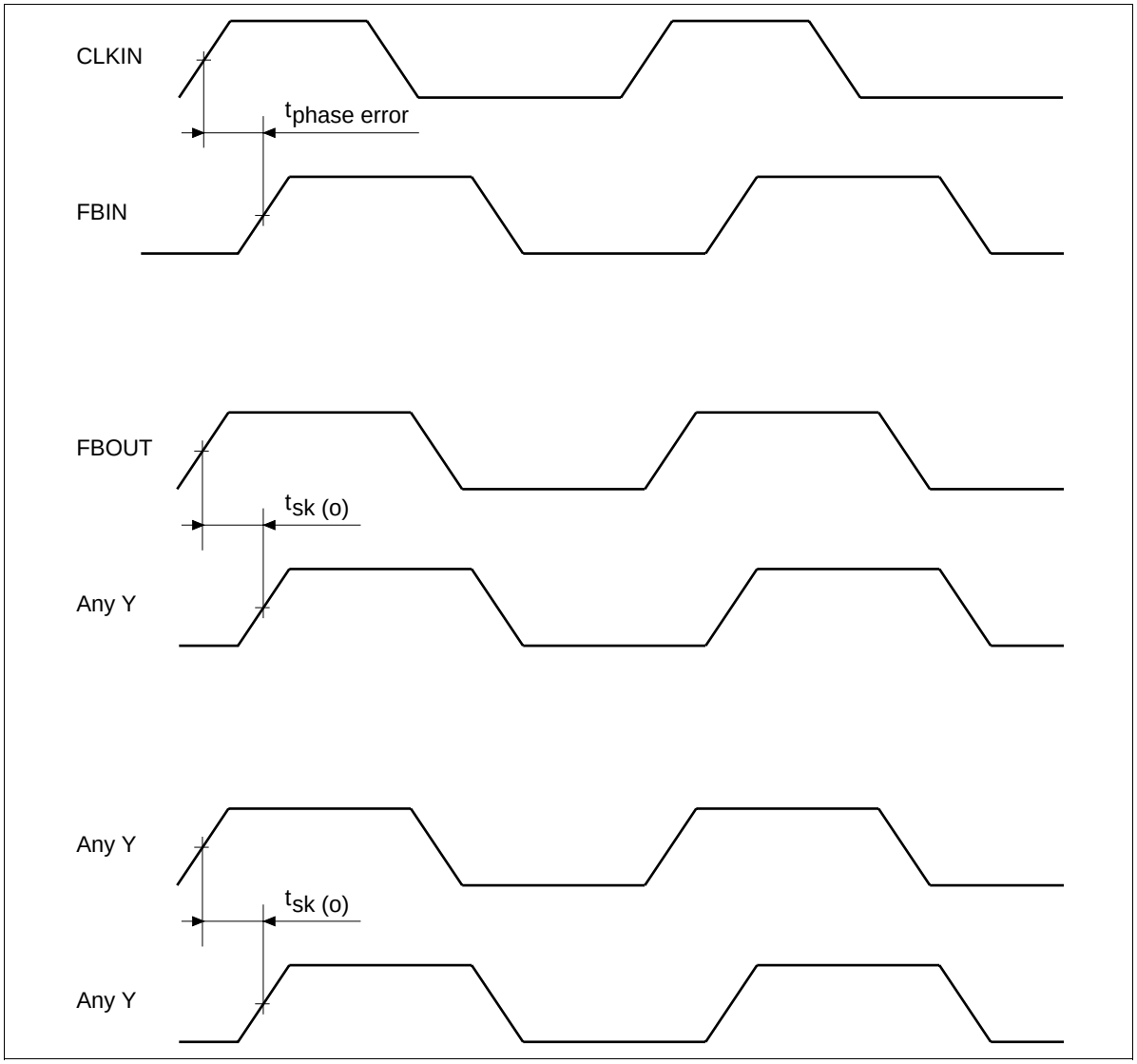
Waveforms – 1



Notes: 1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r = 1.2 ns, t_f = 1.2 ns.

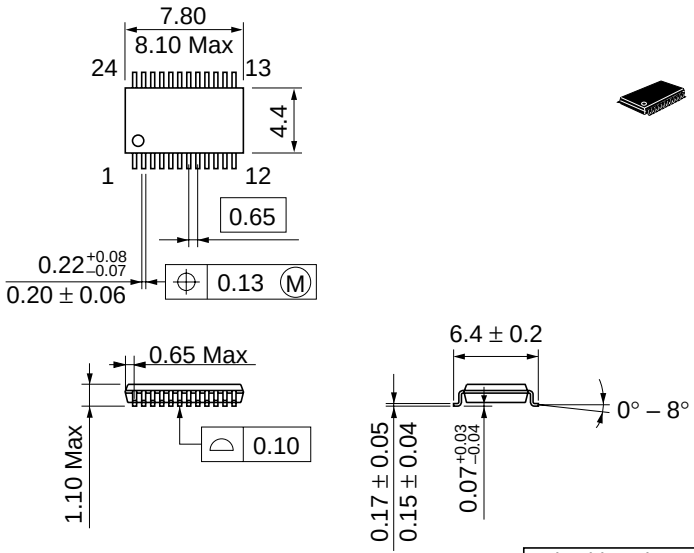
2. The outputs are measured one at a time with one transition per measurement.

Waveforms – 2



Package Dimensions

Unit : mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-24DB
JEDEC	—
EIAJ	—
Weight (reference value)	0.08 g

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