HD74CDC857

3.3/2.5-V Phase-lock Loop Clock Driver

HITACHI

ADE-205-222E (Z)
6th. Edition
July 1999

Description

The HD74CDC857 is a high-performance, low-skew, low-jitter, phase locked loop clock driver. It is specifically designed for use with DDR (Double Data Rate) synchronous DRAMs.

Features

- Supports 100 MHz to 150 MHz operation range [*1]
- Distributes one differential clock input pair to ten differential clock outputs pairs
- SSTL_2 (Stub Series Terminated Logic) differential inputs and LVCMOS reset (G) input
- Supports spread spectrum clock
- External feedback pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the outputs to the clock input
- Supports both 3.3 V/2.5V analog supply voltage (AV_{CC}), and 2.5 V V_{DDQ}
- No external RC network required
- Sleep mode detection
- 48pin TSSOP (Thin Shrink Small Outline Package)

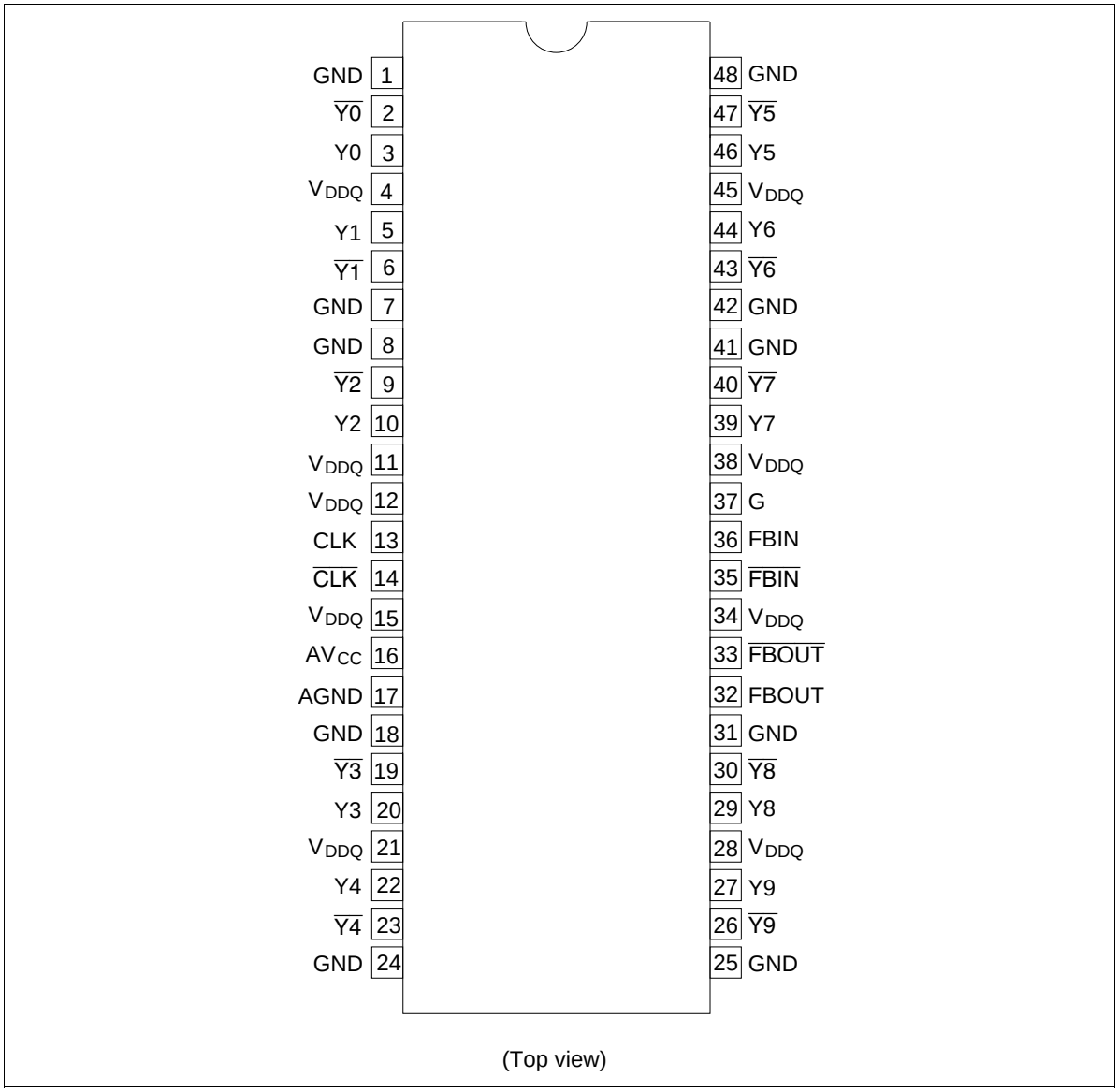
Note: 1. 200 MHz (Max) ver. will be available by 4Q/'99

Function Table

Inputs			:	Outputs				:	PLL
G	CLK	$\overline{\text{CLK}}$	:	Y	$\overline{\text{Y}}$	FBOUT	$\overline{\text{FBOUT}}$		
L	L	H	:	Z	Z	Z	Z	:	off
L	H	L	:	Z	Z	Z	Z	:	off
H	L	H	:	L	H	L	H	:	run
H	H	L	:	H	L	H	L	:	run
X	0 MHz	0 MHz	:	Z	Z	Z	Z	:	off

H : High level
L : Low level
Z : High impedance
X : Don't care

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{DDQ}	–0.5 to 4.6	V	
Input voltage	V_I	–0.5 to 4.6	V	
Output voltage [*1]	V_O	–0.5 to V_{DDO} +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	–50	mA	$V_O < 0$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{DDQ}
Supply current through each V_{DDQ} or GND	I_{VDDQ} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air)		0.7	W	
Storage temperature	T_{stg}	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	AV_{CC} (1)	2.3	—	2.7	V	f_{CLK} = 100 to 150 MHz
	AV_{CC} (2)	3.0	—	3.6		f_{CLK} = 130 to 150 MHz
Output supply voltage	V_{DDQ}	2.3	—	2.7	V	
DC input signal voltage *1		–0.3	—	V_{DDQ}+0.3	V	All pins
High level input voltage	V_{IHD}	1.7	—	—	V	
Low level input voltage	V_{ILD}	—	—	0.8	V	
High level input voltage	V_{IHG}	1.7	—	V_{DDQ}+0.3	V	G input pin
Low level input voltage	V_{ILG}	–0.3	—	0.7	V	G input pin
Differential input signal voltage *2	V_{ID}	0.36	—	V_{DDQ}+0.6	V	DC
		0.7	—	V_{DDQ}+0.6		AC
Differential cross point voltage *3		$0.5 \times V_{DDO}$ –0.35	—	$0.5 \times V_{DDO}$ +0.35	V	
Reference voltage *4	V_{ref}	1.15	1.25	1.35	V	Vref = $0.5 \times V_{DDQ}$
Output current	I_{OH}	–7	—	–30	mA	
	I_{OL}	7	—	30		
Input slew rate	SR	1	—	—	V/ns	
Operating temperature	T_a	0	—	70	°C	

Notes: Unused inputs must be held high or low to prevent them from floating.

Feedback inputs (FBIN, $\overline{\text{FBIN}}$) may float when the device is in low power mode.

1. DC input signal voltage specifies the allowable dc execution of differential input.
2. Differential input signal voltage specifies the differential voltage |VTR–VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
3. Differential cross point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing. (See figure1-1)
4. V_{ref} is the reference DC level, when using single clock input. When CLK (pin#13) is single ended input, $\overline{\text{CLK}}$ (pin#14) must be set V_{ref} . (See figure1-2)

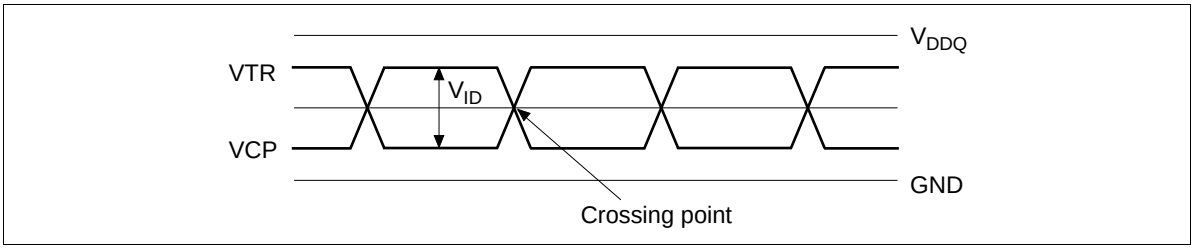


Figure 1-1 Differential input levels

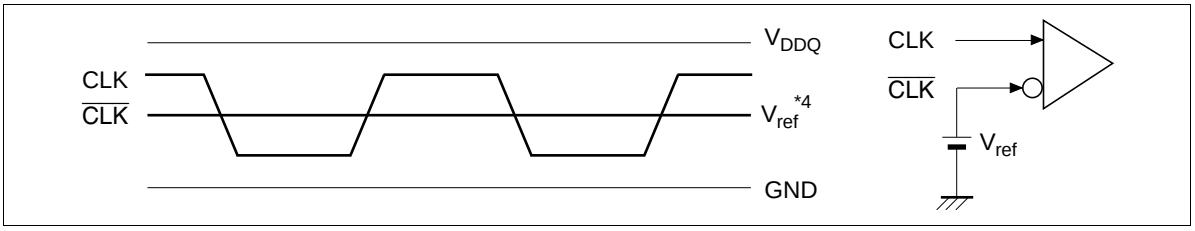
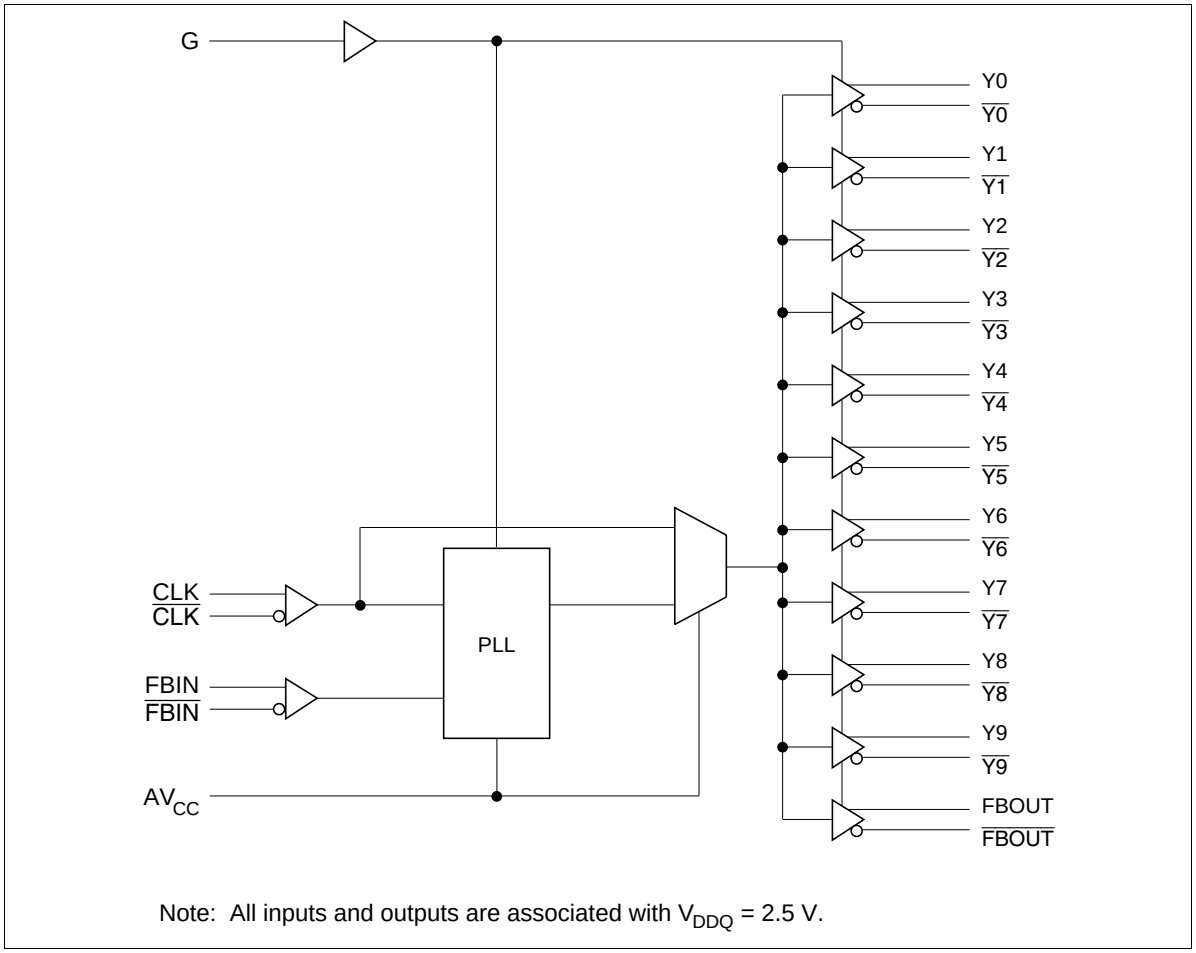


Figure 1-2 Single input levels

Logic Diagram



Note: All inputs and outputs are associated with V_{DDQ} = 2.5 V.

Pin Function

Pin name	No.	Type	Description
AGND	17	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
AV_{CC}	16	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
CLK, $\overline{CLK}$	13, 14	I	Clock input. CLK provides the clock signal to be distributed by the HD74CDC857 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{FBIN}$, FBIN	35, 36	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
FBOUT, $\overline{FBOUT}$	32, 33	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
G	37	I	Output bank enable. G is the output enable for all outputs. When G is low, VCO will stop and all outputs are disabled to a high impedance state. When G will be returned high, PLL will re-synchroniz to CLK frequency and all outputs are enabled.
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	Ground	Ground
V_{DDQ}	4, 11, 12, 15, 21, 28, 34, 38, 45	Power	Power supply
Y	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	O	Clock outputs. These outputs provide low-skew copies of CLK.
$\overline{Y}$	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	O	Clock outputs. These outputs provide low-skew copies of $\overline{CLK}$.

Electrical Characteristics

Item		Symbol	Min	Typ [*1]	Max	Unit	Test Conditions
Input clamp voltage	CLK, $\overline{CLK}$ FBIN, $\overline{FBIN}$, G	V_{IK}	—	—	–1.2	V	I_I = –18 mA, V_{DDQ} = 2.3 V
Output voltage		V_{OH}	V_{CC}–0.2	—	—	V	I_{OH} = –100 µA, V_{CC} = 2.3 to 2.7 V
			1.95	—	—		I_{OH} = –8 mA, V_{CC} = 2.3 V
			1.70	—	—		I_{OH} = –16 mA, V_{CC} = 2.3 V
		V_{OL}	—	—	0.2		I_{OL} = 100 µA, V_{CC} = 2.3 to 2.7 V
			—	—	0.35		I_{OL} = 8 mA, V_{CC} = 2.3 V
			—	—	0.55		I_{OL} = 16 mA, V_{CC} = 2.3 V
Input current		I_I	—	—	±10	µA	V_I = 0 V to 2.7 V, V_{DDQ} = 2.7 V
Input capacitance		C_I	—	—	4	pF	

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Switching Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Cycle to cycle jitter		–100	—	100	ps	See figure 2
Phase error time	$t_{(phase\ error)}$	–150	—	150	ps	See figure 2, 3, 4
Output skew	$t_{sk\ (o)}$	—	—	200	ps	See figure 2
Differential clock skew	$t_{sk\ (diff)}$	–100	—	100	ps	See figure 2
Duty cycle		45	—	55	%	See figure 2
Output impedance	Z_O	—	25	—	Ω	See figure 2
Clock frequency	f_{CLK}	100	—	150 [*1]	MHz	See figure 2, AV_{CC} = 2.5±0.2 V
		130	—	150 [*1]		See figure 2, AV_{CC} = 2.5±0.2 V or AV_{CC} = 3.3±0.3 V
Slew rate		1.2	—	—	V/ns	See figure 2
Stabilization time		—	—	0.1	ms	See figure 2, 3

Note: 1. 200 MHz (Max) ver. will be available by 4Q/'99.

Differential clock outputs are directly terminated by a 120 Ω resistor. Figure 2 is typical usage conditions of outputs load.

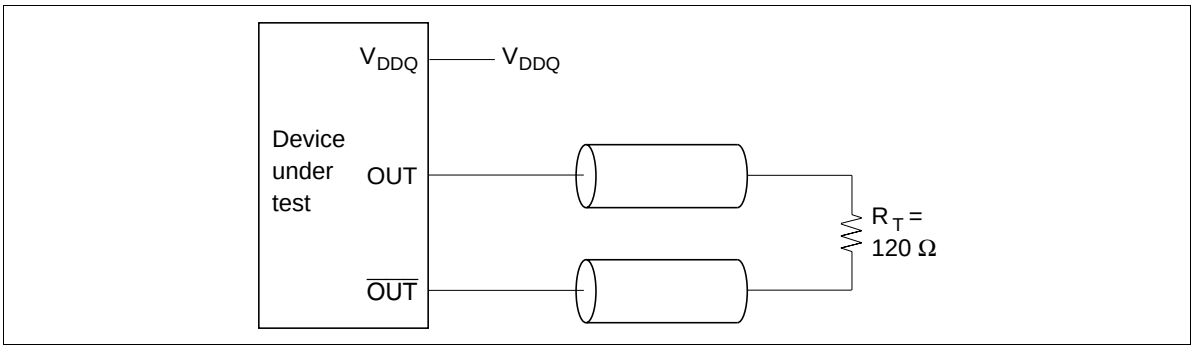
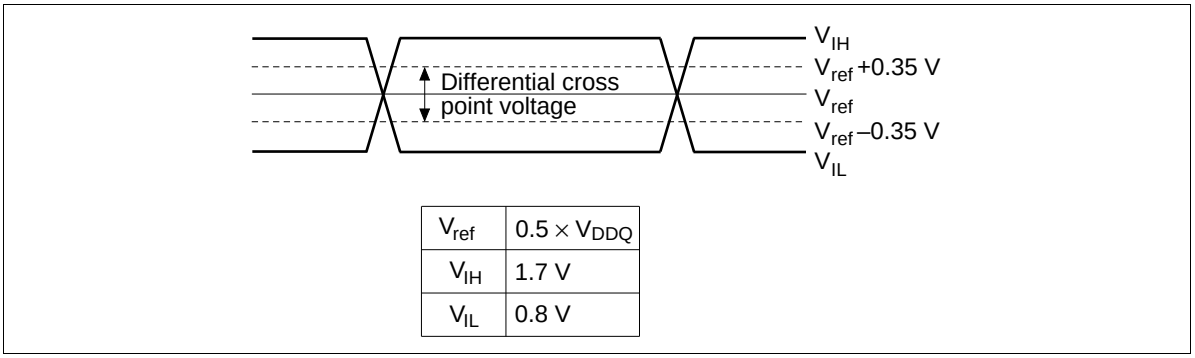


Figure 2 Differential signal using direct termination resistor



V_{ref}	$0.5 \times V_{DDQ}$
V_{IH}	1.7 V
V_{IL}	0.8 V

Figure 3 CLKIN waveforms

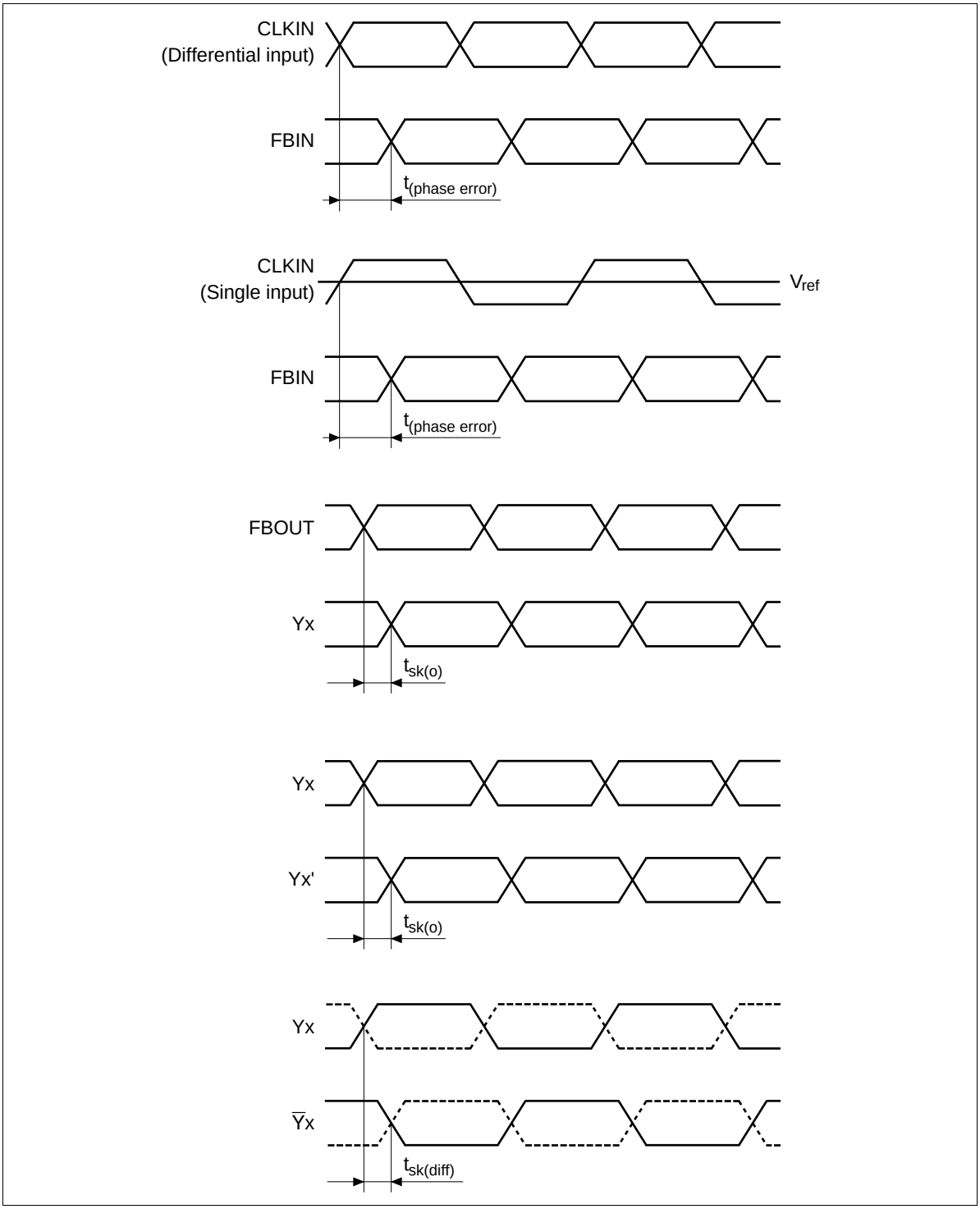
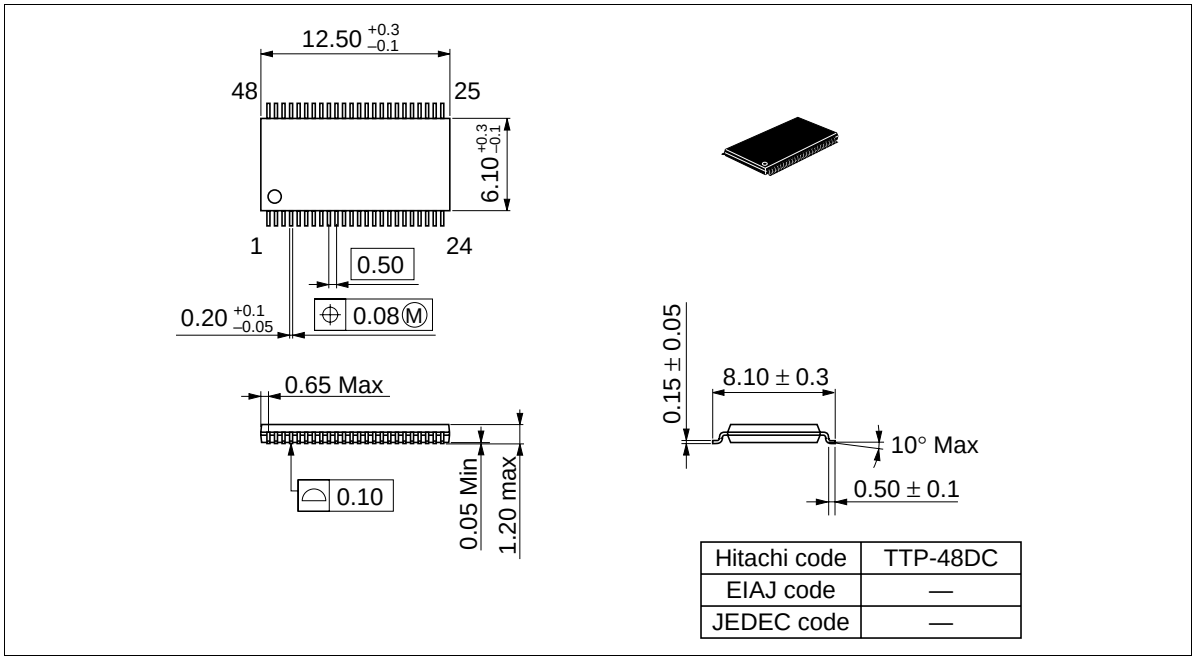


Figure 4 Timings

Package Dimensions

Unit : mm



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